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Impulse-Based Asynchronous Serial Communication Protocol on Optical Fiber Link for AER Systems

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***Abstract* — We developed an Impulse-Based Asynchronous Serial Address-Event Representation (IB-AS-AER) protocol. It allows for full-duplex communication and explicit flow control, does not require any clock data recovery or accurate clock relationship between the transmitter and receiver. Moreover, the optical fiber communication link, that galvanically isolates the communicating devices, highly improves the robustness to electromagnetic disturbances, reduces the power consumption and allows for high data rate transmissions. In addition, the proposed implementation does not require any specific hardware and can be developed on low-cost FPGAs as well as on full-custom ASICs. Preliminary tests performed at 100 Mbps raw bit transfer rate confirm a 32 bit maximum event rate of 2.9 Meps.**

Keywords* — *Asynchronous Systems, Optical Fiber Links, Event-Driven Communications, AER Protocol.

I. Introduction

The Address-Event Representation (AER) is the standard communication protocol adopted by the neuromorphic community [1]. It is used to send asynchronous "events" across neuromorphic (or event-driven) devices such as sensors and computation platforms. In AER, the broadcasted data is a digital pulse with a payload describing the identifier (or address) of the emitting source. Information is encoded in the timing of the digital pulses (or events) themselves. The most common implementation of the AER protocol employs parallel lines for the payload with a request/acknowledge handshake. However, embedded applications would strongly benefit from serial implementations of the protocol, as the increasing capacity of neuromorphic chips requires an increasing number of bits (and wires) for encoding the address [2-5]. Even though a standard serial AER protocol is not yet defined and commonly accepted, a list of requirements and constraints has been defined within the neuromorphic community [6], to which all reported solutions try to comply as much as possible, even if all of them introduce constraints on their implementation relying on some specific components [3-5], or on full custom solutions [2].

In this paper, we propose an evolution of the serial protocol proposed in [7], where the data is encoded now in pulse-to-pulse time intervals. The Impulse-Based Asynchronous Serial AER (IB-AS-AER) protocol is based on an optical fiber link as the physical layer (according to the ISO/OSI interconnection model), that satisfies the requirements defined for the neuromorphic systems, together with a specific implementation to prove its feasibility. This protocol shares almost all the features of those relying on LVDS communication. Specifically, it does not require any clock recovery, nor any assumption on the relationship between the transmitter and receiver clock for a given communication speed. In contrast with LVDS communication channels, where the galvanic isolation between devices is implemented through AC-coupling capacitors, thereby imposing the constraint of a DC-balanced protocol, here the same feature is implicitly provided by the use of an optical fiber link, thereby allowing to trade the DC-balancing for an impulse-based encoding.

The system implementation is based on an FPGA parametrized soft-core that does not need any vendor- nor model-specific features. This solution achieves high portability across devices and can be implemented on ASICs. The proposed architecture has been tested both on Xilinx Artix-7 and Virtex-6, spanning a range of different trade-offs between performances and costs. The second major contribution of this paper is the use of an optical communication substrate for the IB-AS-AER based on an optoelectronic platform composed by a semiconductor laser, a Si photodiode, an optical fiber, and the related electronic circuits allowing for the communication link. This solution highly increases the overall system electromagnetic compatibility and signal integrity. Our measurements show that the implemented system reduces signal interferences and disturbances, hence improving data rate, BER and power consumption [8,9]. Eventually, the optical communication exploits the inherent galvanic isolation between the transmitter and the receiver, typically achieved through capacitive coupling that requires a DC-balanced protocol. The full system, shown in Fig. 1, is composed by a transmitter module (TX) that encodes the signal into digital voltage pulses and sends them to the optical fiber through an optical driver. An optical detector module is then connected to the receiver module (RX) that decodes the pulses. Both TX and RX modules communicate to other subsystems of the FPGA by means of a Synchronous Parallel AER (SPAER) interface. The system is equipped with error and debug signals that provide information about the status of the communication.

In this paper, we provide the characterization of the full system first presented at [7], where the communication system was demonstrated live in our target application, that is the communication of events generated by an event-driven skin patch of the iCub humanoid robot [10-14]. In this application, remote sensors embedded in the skin that covers the body of the robot send events to a main processing unit.

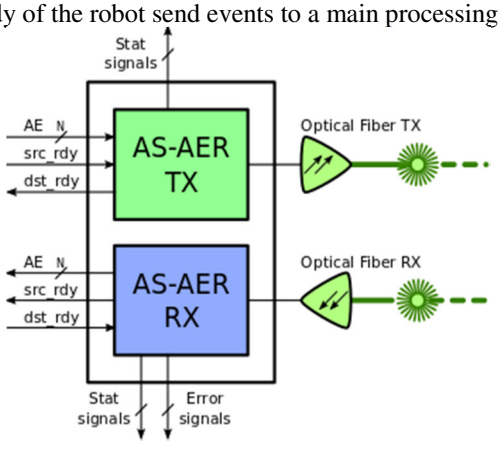

Fig. 1. Overall block diagram of the reference implementation of the transceiver for the proposed IB-AS-AER protocol (adapted from [7]).

The event-driven encoding ensures that skin data are sent only during a contact with the robot, but at the same time has constraints on the number of wires that can be integrated on the platform. As technical specification, the specific application set the maximum raw bit rate at 100 Mbps. The validation in a full pipeline comprising also the sensors and the robot is a strong feasibility proof, on the other hand, it is general enough, as the protocol here discussed defines only the physical and datalink layer and does not impose any constraint on the upper layers of the ISO/OSI interconnection model.

II. System Implementation

A. Transmitter

Fig. 2 shows the building blocks and data flow of the transmitter. It is largely based on the architecture previously used in [7], comprising a SPAER interface, a modified Non-Return Zero Mark (NRZM) sequencer and the corresponding delayed modulator needed to run the module at full-speed with back-to-back transmitted packets, eventually, a Double Data Rate (DDR) output stage (running at twice the base clock, i.e., 200 MHz for a 100 Mbps transfer rate) generates the voltage pulses for the laser driver circuit. The full transmitter is parametrized (at synthesis time) on the number of bits per packet to be transmitted, and it is designed to be scalable w.r.t. the clock/data rate: by multiplying by N the clocks, the raw data rate will be increased of the same factor.

B. Optical fiber communication link

Fig. 3 shows the block diagram of the optical communication link. A driver circuit converts the input voltage pulses from the transmitter module into current pulses that drive a Vertical Cavity Surface Emitting Laser (VCSEL, OPV314AT by TT Electronics) with response time lower than 100 ps, 2.2 mA threshold current, and maximum emitting power at λ=850nm. The VCSEL is coupled to a 1 m length 50/125 µm multi-mode optical fiber. The light pulses are detected and transformed back into current pulses by a high-speed Si-based photodiode (PD, DET025AFC/M by Thorlabs) with rise/fall times of about 150 ps, coupled to the optical fibre. Eventually, a conditioning circuit converts the current into voltage pulses that are sent as input to the receiver module. Fig. 4 and 5 show the schematic of the driver and conditioning circuits of Fig. 3, respectively. The former regulates both the current amplitude and DC level through two resistive trimmers Rvar1 and Rvar2. The latter provides the reverse biasing to the photodiode and amplifies the pulsed signal to reach the amplitude values matching the logic threshold levels of the standard I/O LVCMOS25 of the receiver modules [8,9]. The circuits of Fig. 4 and 5 had been simulated (AWR Microwave Office) and implemented with discrete off-the-shelf components on prototype Printed Circuit Boards. The chosen components are wide bandwidth low noise Si-Ge bipolar RF transistors BFP720 operating at 3.3V single supply voltage.

C. Receiver

Fig. 6 shows the architecture of the receiver. As for the transmitter, the overall structure is derived from the proof-of-concept implementation presented in [7], partitioned into two halves belonging to two different clock domains. The major improvement is the introduction of an asynchronous input toggle Flip-Flop (FF): even if actually implemented by standard and not vendor specific resources, its input clock is the received stream of pulses generated by the photodiode and the relative signal conditioning circuit. The resulting signal is then sampled by a DDR module and the corresponding Inter-Edge-Interval (IEI) computed by a LFSR counter. Through a LFSR-based FIFO and a Pulse-to-Toggle-to-Pulse re-synchronization block, the IEI values are transferred to the low-speed clock domain, converted into binary numbers and then interpreted by the AS-AER decoder Finite State Machine (FSM). Finally, a standard SPAER interface communicates with the following modules through a common parallel protocol. Similarly to the transmitter, the receiver is parametrized (at synthesis time) on the number of bits per packet to be received and is scalable w.r.t. the clock/data rate: by multiplying by *N* the clocks and retaining a high/low speed clocks frequency ratio of three, the raw input data/output event rate will be increased by N.

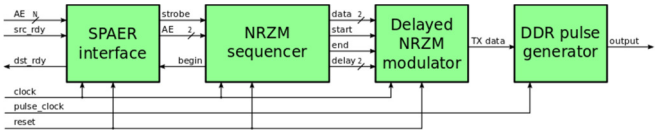

Fig. 2. Block diagram of the proposed IB-AS-AER transmitter (adapted from [7]).

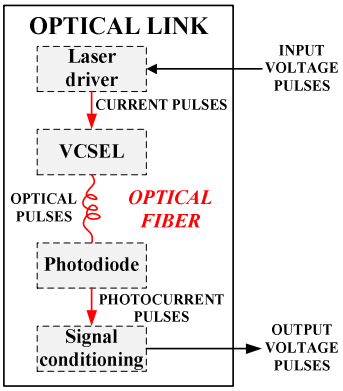

Fig. 3. Block diagram of the optical fiber communication link including all the optoelectronic devices and circuits.

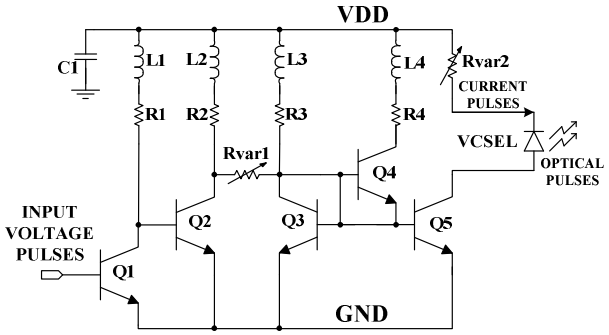

Fig. 4. Schematic circuit of the implemented laser driver block.

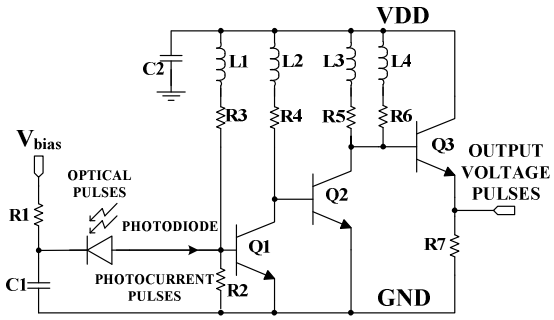

Fig. 5. Schematic circuit of the implemented signal conditioning block.

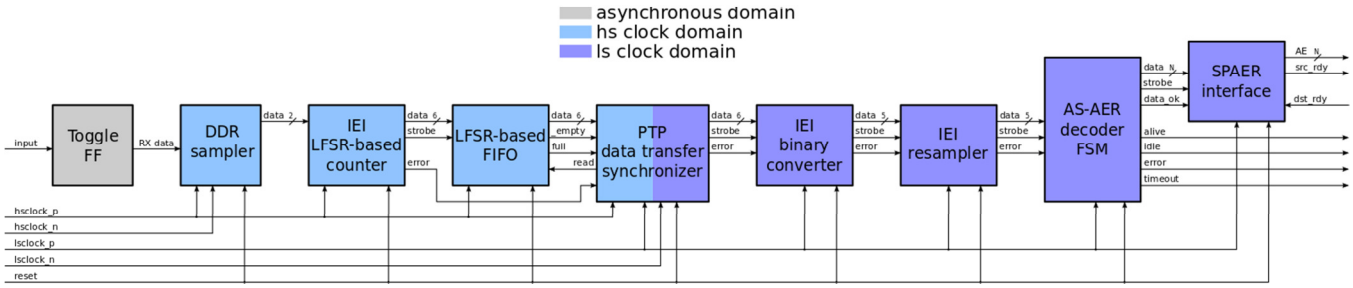

Fig. 6. Block diagram of the proposed IB-AS-AER receiver (adapted from [7]).

III. Experimental Results

The characterisation of the asynchronous AER protocol is reported in [7], here we report a summary of the results for completeness. We developed two demonstrators based on the Xilinx Virtex-6 (XC6VLX240T) and Artix-7 (XC7A50T), respectively, with the goal of assessing basic performance and protocol validation on FPGA devices with different performance. In all experiments, the TX and RX clocks were always separated and independent, using different external clock sources. TX and RX were connected through an external loop-back (with decoupling capacitors) or via an Ethernet cable for test purposes.

In the Virtex-6 implementation the resource utilisation (16 bit AER events, as configured in the following tests) is 31 (TX) and 76 (RX), while on the Artix-7 the same amount to 29 (TX) and 90 (RX). With a payload of 32 bits (plus the protocol overhead of start and end parity bits), the maximum measured transfer rate without errors is 2.9 Meps at raw bit rate of 100 Mbps; with 16 bits of payload it increases up to 5.5 Meps.

The Virtex-6 implementation was characterised more thoroughly, using a testbench with a pseudo-random AER events generator controlled by a trigger with run-time configurable rate and jitter. For the sake of simplicity and completeness (to fully test the allowed payload space for each transmitted event for a significant number of test cycles) the 16 bit per event implementation was tested. The TX clock was controlled by a Keithley 3390 arbitrary waveform generator for maximum precision, while the RX clock is generated on board. The transmitted and received events are then compared for error detection while changing the TX/RX clock ratio.

Fig. 7 shows an example of the main signals, taken from an oscilloscope in the time domain, related to the developed event-based serial communication protocol operating at 100 Mbps. In particular, it reports the signal AS-AER coded by the edge-to-edge intervals approach representing a 16 bit AER event. Simultaneously, the corresponding IB-AS-AER signal is also reported showing the pulse-to-pulse intervals coding technique that provides a train of 2.5 ns voltage pulses always related to a 16 bit AER event. These pulses are then used as the input pulsed signal for the laser driver block of the optical fiber communication link.

Moreover, in Fig. 8 is reported a photo of the experimental set-up implemented to test the overall optical fiber communication link composed by the laser driver, the VCSEL, the optical fiber, the photodiode and its signal conditioning circuit. In this regard, a further proper *ad-hoc* test-bench has been developed on a Virtex-6 FPGA board so to test and validate the event-driven serial communication protocol on the optical fiber link by performing a data transmission corresponding to 16 bit AER events with $2^{32} \approx 4 \cdot 10^9$ transmissions of events for each conducted test. More in detail, measurements have been conducted for the evaluation of the number of coded AER events that have not been correctly received by the receiver with respect to the 2^{32} transmitted events. Different errors have been achieved as a function of the different settings of the laser driver and of the photodiode signal conditioning circuit. In particular, referring to Fig. 4 and 5, by changing the maximum pulsed current amplitude through the resistive trimmer Rvar1 and adjusting the reverse bias voltage of the photodiode through the Vbias terminal, the following errors have been achieved for three different optoelectronic circuit setups: 8.8×10^{-4} for the minimum VCSEL current and the minimum photodiode reverse bias voltage; 1.53×10^{-6} for the maximum VCSEL current and the minimum photodiode reverse bias voltage; 0 for the maximum VCSEL current and the maximum photodiode reverse bias voltage. In this last operating condition, no error occurred and so no event was not correctly received with respect to the 2^{32} transmitted events.

Finally, several tests of the overall system, including the optical fiber communication link, have been also performed considering 16 bit AER events, with $2^{32} \approx 4 \cdot 10^9$ transmissions per test at a nominal TX/RX clock equal to 100 MHz (i.e., a raw bit rate of 100 Mbps). Starting from these operating conditions, the TX clock have been spanned in the range 93–107 MHz with different variation steps resulting into a maximum TX/RX clock ratio of ± 7%. Figure 9 reports the achieved results demonstrating that at a bit rate of 100 Mbps, by changing the TX/RX clock ratio of ±2%, the error rate, measured as the number of AER events not correctly received, is equal to zero. This result relaxes the constraints on the synchronisation of clock sources for transmitter and receiver, as opposed to those solutions requiring a clock precision of the order of 100 ppm (e.g., the standard/common Ethernet applications).

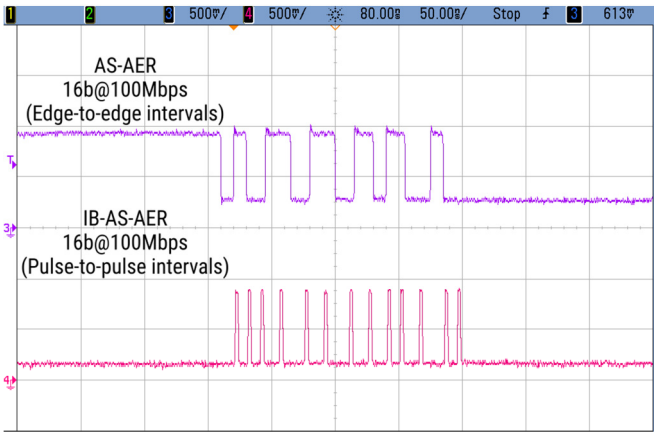

Fig. 7. Example of the main signals related to the implemented IB-AS-AER serial protocol operating with 16 bit per event at 100Mbps.

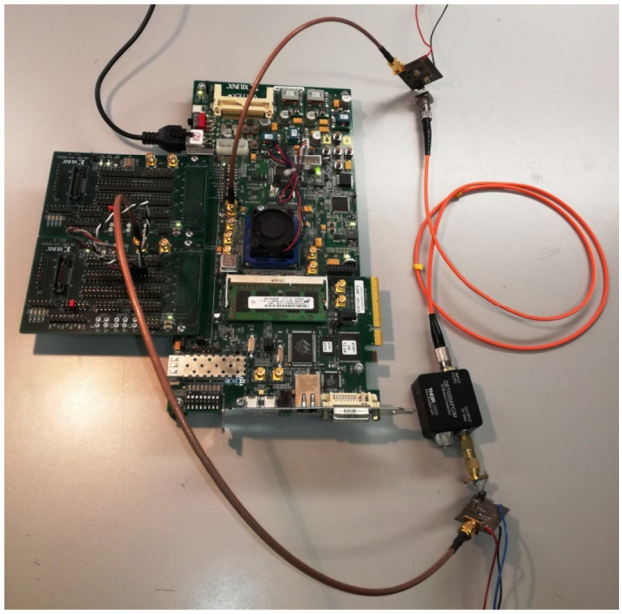

Fig. 8. Photo of the experimental set-up implemented for testing the optical fiber communication link.

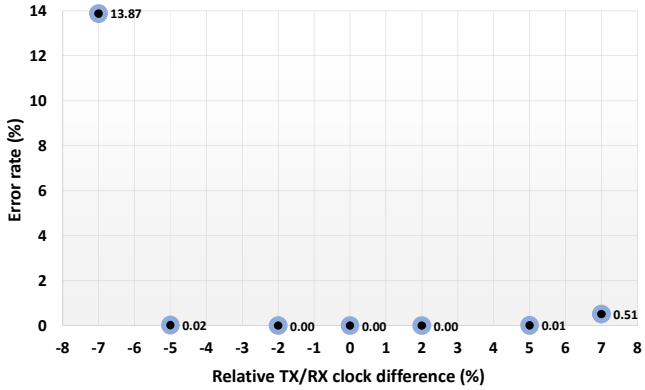

Fig. 9.Error rate as a function of the relative difference between TX and RX clocks. No error occurred for a clock difference in the range ±2%.

IV. Conclusions and Future Perspectives

In this work, we integrated an asynchronous serial communication protocol for AER, AS-AER, that sends information in the form of digital voltage pulses, with an optical communication link that transfers information in form of light pulses. This highly enhances the system electromagnetic compatibility and signal integrity, decreases the power consumption and allows for high data rate transmissions. The achieved experimental results are in a very good agreement with the expectations showing negligible values of the transmission errors.

The paper reports preliminary characterization of the full system, with quantitative measurements using controlled inputs as well as qualitative behaviour when the system is integrated in our target application. In this case, the events to be communicated are generated by tactile sensors, and the maximum measured transfer rate is 2.9Meps (for 32 bits addresses).

After this prototype proof of concept, the path to a full integration on a robotic platform involves the miniaturisation of all the components, going towards the implementation of the transmitter and driver modules on a single ASIC, also integrating the emitting laser onto the device [15].

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