Three-phase SiC inverter with active limitation of all MOSFETs junction temperature

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Review paper

# Three-phase SiC inverter with active limitation of all MOSFETs junction temperature

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ABSTRACT

Estimating the junction temperature of power electronic devices is of paramount importance for assuring the reliable operation of power converters. Wide bandgap devices, that allow extremely high-power density levels, make thermal management even more critical than before. Despite the efforts of the scientific community, this problem is far from being solved. Techniques based on thermo-sensitive electrical parameters are gaining momentum in the scientific literature, although their application to real case scenarios is slowed down by many unsolved challenges. The aim of this paper is to present a three-phase SiC inverter capable of accurate junction temperature estimation for all the SiC power MOSFETs and of active limitation of the maximum junction temperature. The temperature estimate is based on the well-known correlation between the conduction resistance and the junction temperature of a semiconductor. It is implemented here on a 3-phase SiC inverter for racing cars used in formula SAE electric student competitions. The experimental results show the effectiveness of the proposed technique in terms of augmented reliability and augmented performance of the power converter.

## 1. Introduction

Wide-bandgap power semiconductors such as SiC MOSFETs represent a step ahead respect to silicon MOSFETs and IGBTs. They have better conductivity, lower switching losses and higher power density. In addition, SiC devices are characterized by better thermal stability and can operate at higher temperature. All of this permits to realize systems capable of operating at higher environmental temperature (e.g. for geothermal exploration, oil and gas, power systems etc.) and to minimize the volume of the heatsink and thus of the converter [1–3].

To put this advantage in practice, it is then important that the junction temperature of the SiC devices is exploited as close as possible to the recommended limit without exceeding it. Operating the device at a higher junction temperature leads to the immediate destruction of the device or at least to a reduced life [4].

One way to avoid temperature dependent failures is to estimate the junction temperature so to provide accurate thermal management. Different solutions were developed over the years to measure or to estimate the junction temperature of power semiconductors. The goal of this paper is to present a technique and a hardware configuration capable of monitoring and actively limiting the junction temperature of the SiC power MOSFETs of a power converter, in realistic operating conditions.

## 2. Review of temperature estimate

In the literature of junction temperature measurement, direct measurement techniques use either a thermal camera [5,6] or a thermistor in direct contact with the chip. None of the two is viable for industrial applications. The first one for cost and practical reasons: the thermal camera cost and volume exceeding the ones of most converters. The second one is in use in a limited number of custom power modules [7], although it was proven critical due to related insulation problems. In fact, the higher reliability obtained due to the knowledge of the junction temperature does not compensate for the loss of reliability due to the presence of the sensor.

State of the art industrial converters make use of an electro-thermal model of the devices. The temperature of the heatsink or of the Direct Bonded Copper (DBC) substrate of the power module is directly measured with a temperature sensor [8,9]. Based on this measurement the junction temperature is calculated combining the estimated losses of the component and a lumped parameter thermal model. The disadvantage of this method is that both the loss and thermal models are known very roughly. This results in a rough estimate of the junction temperature, which still obliges to retain large safety margins. In turn, heatsink and semiconductors are inevitably oversized. Despite the effort of the scientific community, the problem is far from being solved.

Finally, techniques based on Thermo Sensitive Electrical Parameters (TSEPs) have gained of importance in recent times the most promising approach to junction temperature estimation in power semiconductors. However, most of these solutions can only be used in a laboratory environment under controlled testing conditions and with dedicated testing equipment.

## 3. Review of TSEP methods

Depending on the type of power semiconductor, different TSEPs can be used [10,11]. The main TSEPs for MOSFETs are:

1. Gate threshold voltage measurement. The gate threshold voltage decreases linearly while the junction temperature increases [10,12–14].
2. Saturation current (transconductance) measurement. This lowers with temperature [15–17].
3. di/dt measurement. The drain current switching rate during the turn-ON transition increases with the temperature [17–19].
4. Body diode voltage. A calibrated low current in injected in the device between the source and drain when the device is commanded OFF (usually with a negative $V_{GS}$ [20]). The voltage drop of the body diode is measured and used as a TSEP [11,17].
5. $R_{ON}$ at low calibrated current. A low calibrated current in injected between drain and source while the MOSFET is commanded close and the conduction resistance is used as a TSEP [17].
6. $R_{ON}$ at hight current. A high current in injected between drain and source while the MOSFET is commanded close and the conduction resistance ($R_{ON}$) is used as a TSEP [1,19,21].

The first three techniques require to measure voltages and currents in a very short timescale. This is feasible in laboratory where dedicated equipment like oscilloscopes can be used. In a real converter, these measurements are not realistically implementable especially for wide bandgap devices that are characterized by fast commutations. A possible work around is to slow down the commutations of the device, the drawback is the loss of efficiency that in most of the cases is unacceptable. In addition, the use of the threshold voltage as a TSEP is problematic, due to the $V_{th}$ instability that is particularly pronounced in SiC devices [13,14]. Techniques number four and five are not time critical however they cannot be implemented on a classical two-level converter. It is not possible to inject a calibrated current between drain and source or between source and drain during the normal operation of the converter. The last technique requires to measure the conduction resistance of the component during its working condition. This measurement is not critical and can be implemented on an industrial converter. However, despite being able to effectively measure the conduction resistance of the component it is necessary to find the correlation between the conduction resistance and its junction temperature. The datasheet of the component usually provides the curve $R_{ON}(\theta_J)$, however this does not consider the parametric dispersion of the components, furthermore this value is usually provided for the worst case scenario (the real $R_{ON}$ is usually lower). The datasheet information cannot be used directly for estimating the junction temperature, in turn every component must be individually characterized.

The characterization is usually performed in laboratory using dedicated equipment like a curve tracer. Once that the $R_{ON}(\theta_J)$ curve is known, the junction temperature of the component can be estimated by measuring its conduction resistance with dedicated laboratory equipment. If the same component is then mounted on a power converter with $R_{ON}$ measurement system on board, it is likely that the system will not be able to correctly estimate the junction temperature. This is due to many factors like the variation of the contact resistance and the errors and nonlinearities of the measurement system. In this paper, starting from the well-known correlation $R_{ON}(\theta_J)$, innovative solutions are here proposed to perform the TSEP tuning directly on the converter without using dedicated laboratory equipment. This permits to obtain a reliable and robust estimation of the junction temperature.

## 4. Hardware description

The overview of the prototypal converter realized for the formula SAE electric student is shown in Fig. 1. The 3-phase inverter uses three

**Fig. 1.** Overview of the 3-phase SiC inverter for the formula SAE electric.

BSM180D12P3C007 SiC power modules by ROHM, with anti-parallel SiC diodes. The custom liquid cooling plate that will be used on the race car was preliminarily replaced by an aluminium hotplate as shown at the bottom Fig. 1. Fig. 2 shows the 3D model of the power converter, with the main parts in evidence. The DC bus board houses six polypropylene capacitors for a total capacitance of 120 μF. Three "Local Cap" boards each housing one 220 nF ceramic capacitor are placed as close as possible to the DC pins of the power module. The three driver boards, one per module, embed the gate driver and the measurement system for the conduction voltage of the MOSFETs.

The control board is placed on top of the inverter. It is based on a hybrid digital architecture with a STM32H7 microcontroller and a Xilinx Spartan 6 FPGA. This solution allows maximum control development flexibility. The control board houses also the current sensors and all the peripherals needed by the race car like CAN interface, two encoder interfaces, uSD for data logging and debugging interfaces. A total of four inverters are installed on the car, one per wheel. The four inverters are controlled via CAN using a dSPACE MicroAutoBox real-time system.

The schematic of the power section of the converter is shown in Fig. 3. The measured quantities are reported in red. Additional measurements with respect to a conventional 3-phase inverter are the ON-state voltage ($v_{ON}$) of the six power MOSFETs (Table 1).

## 5. $v_{ON}$ measurement system

The $v_{ON}$ measurement system samples the ON-state voltage of the component during PWM operation at high voltage. The schematic of the analog conditioning stage of the $v_{ON}$ measurement system is shown in Fig. 4. This consists of an operational amplifier in differential configuration connected between the drain and the source of the power

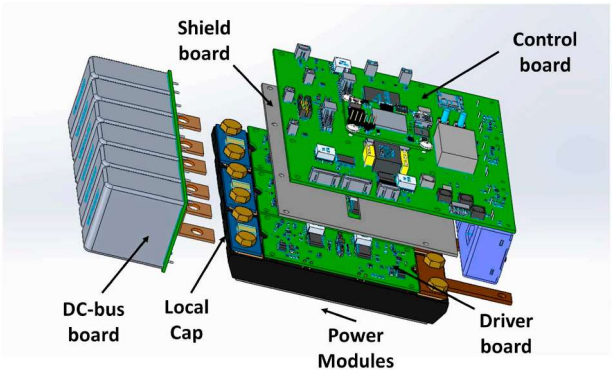


**Fig. 2.** 3D model of the power converter.

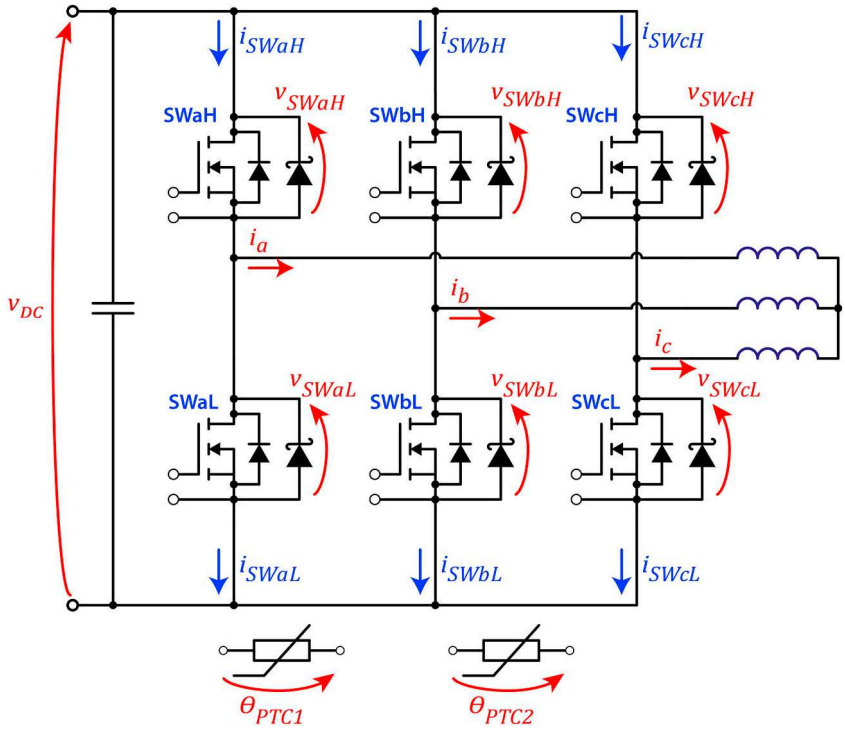


**Fig. 3.** Schematic of the power section of the 3-phase inverter.

**Table 1**
Ratings of the prototypal inverter.

| | |
|---|---|
| Peak output current | 240 A |
| Maximum DC voltage | 700 V |
| Maximum switching frequency | 200 kHz |
| Nominal switching frequency | 20 kHz |
| DC-link film capacitors | 5 × 20 μF |
| DC-link ceramic capacitors (SMD) | 3 × 220 nF |
| Microcontroller | STM32H743ZI |
| FPGA | Spartan6-XC6SLX75 |
| N° A/D channels of the MCU | 3 |
| N° 14-bit external A/D converters | 10 |
| CAN | CAN bus 2.0 |
| Encoder interface 1 | Absolute (EnDat 2.2) |
| Encoder interface 2 | Incremental |
| Power module, BSM180D12P3C007 | |
| Rated current (Tcase = 60 °C) | 180 A |
| Breakdown voltage | 1200 V |
| $R_{ON}$ @ 50 °C | 11 mΩ |
| Stray inductance | 25 nH |
| Max junction temperature | 175 °C |

MOSFET. The output of the analog conditioning system is connected to a 14-bit local ADC (not represented in the schematic) that communicate the sampled data to the control board through SPI communication. When the MOSFET is in conduction mode the voltage between drain and source is few volts however, when the MOSFET is in interdiction mode this voltage rises to the DC-link voltage. In turn, the diode D6 was added to protect the measurement system. When the MOSFET is in conduction state the diode D6 is forward biased using a constant current, thus allowing us to measure the voltage drop on the MOSFET. The transistor Q1 acts as a constant current source. The diode D4 is connected in series to the diode D6, so that in the first approximation is run by the same current. The voltage drop on D6 is used to compensate the voltage drop on D4, so that they cancel each other. Any small difference in the two voltage drops does not affect the temperature estimation provided that is constant over time. It is well known that the diodes forward voltage drop is temperature dependent, however the two diodes can be considered at the same temperature due to their physical proximity. Diodes D4 and D6 are type S1N-13-F (1.2 kV, 1 A @ 100 °C). The obtained bandwidth of the measurement system is circa 40 MHz. The MOSFET Q2 can be used to shorten the input of the operational amplifier when the power MOSFET is OFF, thus avoiding the saturation of the output of the operational amplifier. This improves the bandwidth of the measurement system. In fact, the operational amplifier needs an additional "recovery" time when going from the saturated state (power MOSFET OFF) to the linear state (power MOSFET ON). The diode D5 was inserted to avoid the conduction of the MOSFET Q2 when the voltage between Source and Drain of the power MOSFET is positive. In this paper we did not use this feature and we always kept the MOSFET Q2 in OFF state, as the switching frequency was limited to 20 kHz. For applications with higher switching frequency (e.g. 100 kHz) this feature can be useful.

This $V_{ON}$ measurement solution was selected for its simplicity and robustness. Alternative $V_{ON}$ measurement systems are available on the literature [1,21–25]. A performance comparison between the different solutions would be complex and it is out of the scope of this paper.

## 6. Power module characterization

The calibration test for the characterization of the power MOSFETs can be performed directly on the converter without the need of dedicated laboratory equipment others than an external heating source and an inductive load. The calibration test permits to obtain the look-up tables of the six MOSFETs used by the temperature estimator shown in Fig. 5. The converter is preliminary connected to an inductive load like an inductor, a transformer or a motor. In this case, a 3-phase star connected inductor with a phase inductance of 33 μH is used. The temperature of the heatsink is controlled using a hotplate.

The main steps of the calibration test are:

1. The aluminium plate is preliminarily heated to 150 °C, according to the two PTC thermistors on the aluminium plate. The hotplate is turned OFF and the aluminium plate starts cooling naturally.
2. At this temperature, short current pulses (< 100 μs) from 10 A to 240 A with step circa 10 A are commanded for each of the six

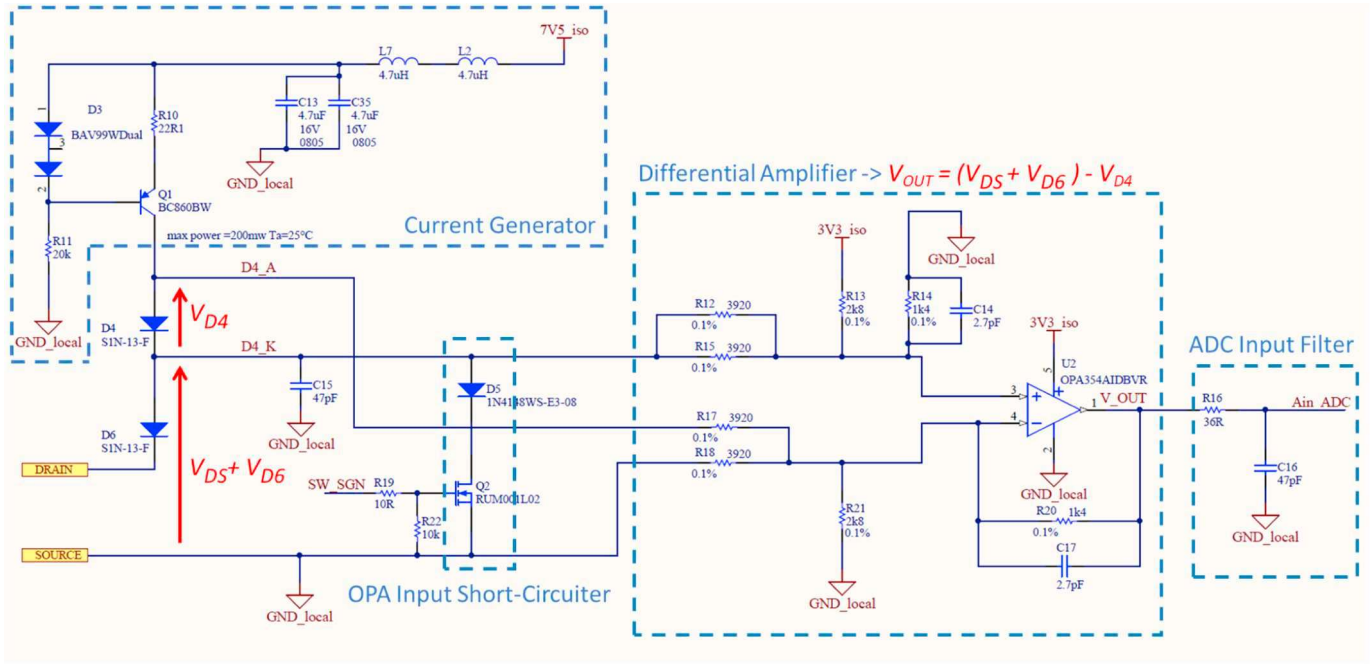


**Fig. 4.** Schematic of the $v_{ON}$ measurment system

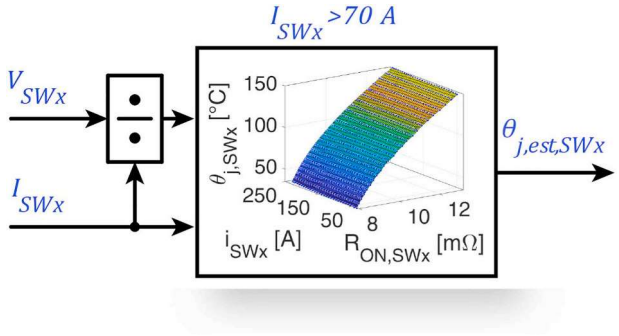


**Fig. 5.** Temperature estimator functional block.

inverter axes as shown in Fig. 6 and Fig. 7. Per each temperature, the currents pulses of growing amplitude are repeated along the six inverter axes. The data collected are shown in Fig. 8 and Fig. 9. Between each current pulse there is waiting time of 200 ms as shown in Fig. 7. This permits to map all the six switches within 240 A pk, for both positive and negative currents.

3. Every time the temperature drops by 5 °C (variable waiting time) a new set of current pulses is commanded along the six inverter axes as shown in Fig. 8.
4. The test stops when the hot plate reaches the room temperature. In this case the test was stopped at 35 °C.

Due to the short duration of the current pulses and to the slow cooling of the system, the temperature measured by the PTC equals the junction temperature of the MOSFETs. In addition, there is an idle time of 200 ms after each current pulse, so to eliminate any residual temperature perturbation. The total calibration time is 90 min, due to the slow natural cooling especially when the system is approaching the room temperature. This time can be significantly reduced by speeding up the cooling process at low temperatures.

### 6.1. Calibration test analysis

Fig. 10 shows a 240 A current pulse along the a+ axis. The bottom of the figure shows the triangular carrier at 20 kHz and reference duty cycles of the three legs. The top of the figure shows the state of the three inverter legs. The state of the inverter leg is "1" when the upper switch is ON and "0" when the lower switch in ON. E.g. "100" indicates that phase "a" is connected to the positive terminal of the DC-link and phase "b" and "c" are connected to the negative terminal. In Fig. 10 the current pulse is imposed along the a + axis and the state of the switches alternates between the active state "100" and the two inactive states "000" and "111" that are represented in Fig. 11. Fig. 10 shows that the total current pulse duration is two PWM periods, equivalent to 100 μs. During the first PWM period the current rises to the target value of 240 A. Conduction voltages, currents and temperatures are sampled during the second PWM period in correspondence of the positive and negative vertex of the triangle, labelled respectively as SP1 and SP2. At the sampling time SP1 the leg state is "111", and the current flowing in

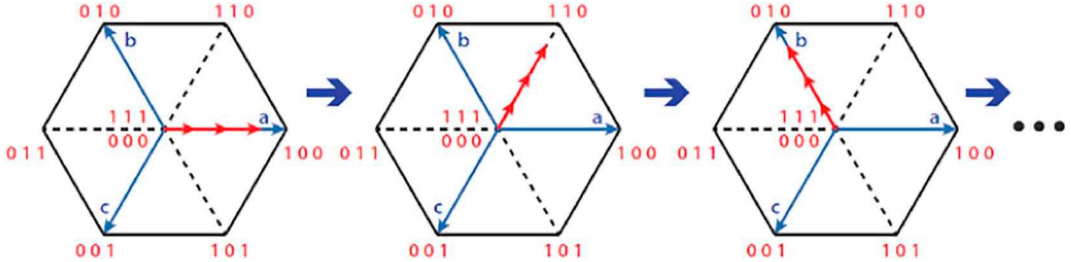


**Fig. 6.** Current pulses of growing amplitude on each of the six inverter axes.

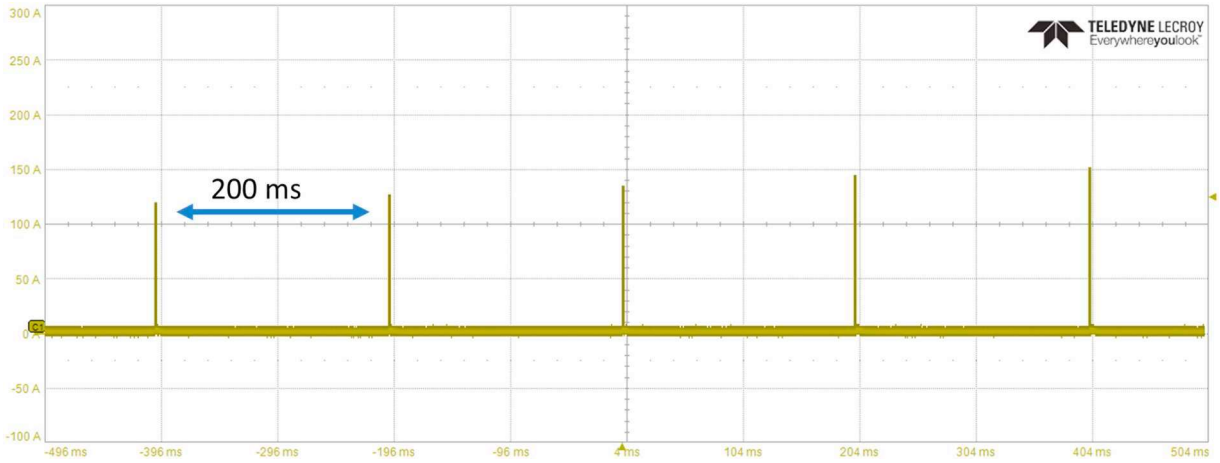


**Fig. 7.** Current pulses of growing amplitude along the "a" axis during the calibration test.

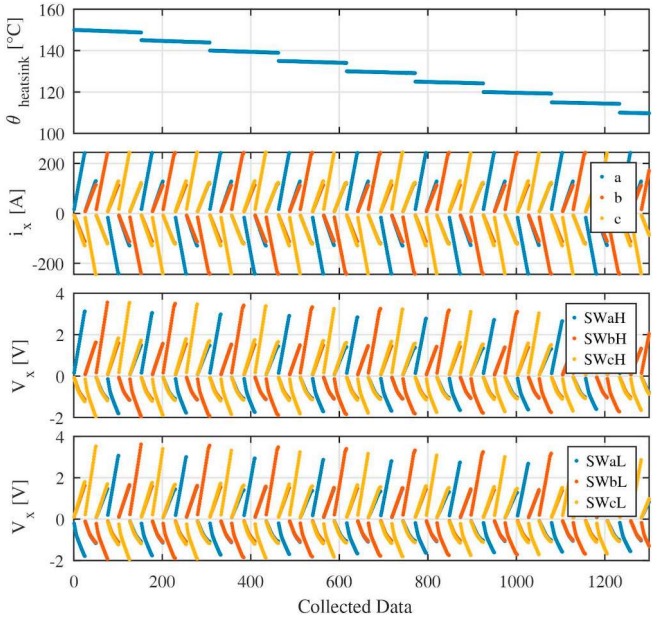


**Fig. 8.** Data collected during the calibration test. The waiting time between collected data is not represented.

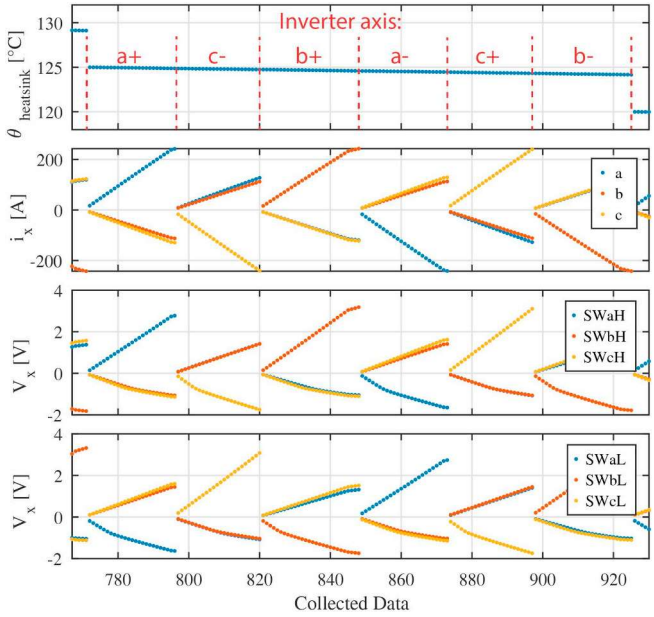


**Fig. 9.** Detail of the data collected during the calibration test highlighting the six inverter axes. The waiting time between collected data is not represented.

SWaH is $i_a$ while the currents flowing in SWbH and SWcH are $-i_a/2$ (Fig. 11). At sampling time SP2 the current flowing in SWaL is $-i_a$ while the currents flowing in SWbL and SWcL are $i_a/2$. In turn, imposing current pulses along the a+ axis makes it possible to map the MOSFET SWaH for positive currents and the MOSFET SWaL for negative currents. If the current pulse injection is repeated for all six axes, all the switches are mapped for positive and negative values of current. One of the main assumptions is that during the calibration test the junction temperature of the MOSFETs equals the temperature measured by the thermistors placed on the aluminium plate.

Indeed, due to the slow natural cooling of the aluminium plate, the system can be considered isothermal. Furthermore, the short duration of the current pulses ensures that during the test the temperatures of the MOSFETs do not vary significantly with respect to the temperature of the aluminium plate. The temperature rise of the MOSFET due to one current pulse in the worst case condition ($\theta_J = 150\,^{\circ}C$, $i_{DS} = 240A$) can be approximately computed. In Fig. 10 switch SWaH is characterized for a current of 240A with a heatsink temperature of 150 °C. The switch is in conduction only in the intervals indicated by a green area. The temperature rise due to the current pulse for switch SWaH is below 2 °C. To reduce the commutation losses the calibration test was performed at a reduced voltage of 340 V.

## 7. Experimental results

The data obtained from the calibration test can be represented in the form $\theta_{j,\ SWx}$ $(V_{SWx}, i_{SWx})$ or equivalently in the form $\theta_{j,\ SWx}$ $(R_{ON,\ SWx}, i_{SWx})$. Using the LUT in this second form is convenient because the obtained results can be interpolated using a polynomial function. As a tile of example, the LUT of the switch SWaH is shown in Fig. 12 for $i_{SWaH} > 30$ A and in Fig. 13 for $i_{SWaH} < -30$ A. The values obtained for currents below 30 A are discarded due to the difficulty of obtaining a reliable measurement of $R_{ON}$. The LUT for positive current can be used by the junction temperature estimator shown in Fig. 5. However, the LUT for negative current is useless for the temperature estimation, as the current sharing between the MOSFET and the antiparallel diode cannot be determined. The data shown in Fig. 12 can be further analysed and represented on a 2D plot. Fig. 14 display the relationship between the junction temperature and the normalized conduction resistance of the MOSFET SWaH at various drain current values. $R_{ON}$ has been normalized respect to $R_{ON,\ SWaH} = 7.88$ mΩ ($\theta_j = 30$ °C, $i_{DS} = 180$ A). This is the lowest $R_{ON}$ value measured experimentally for a current

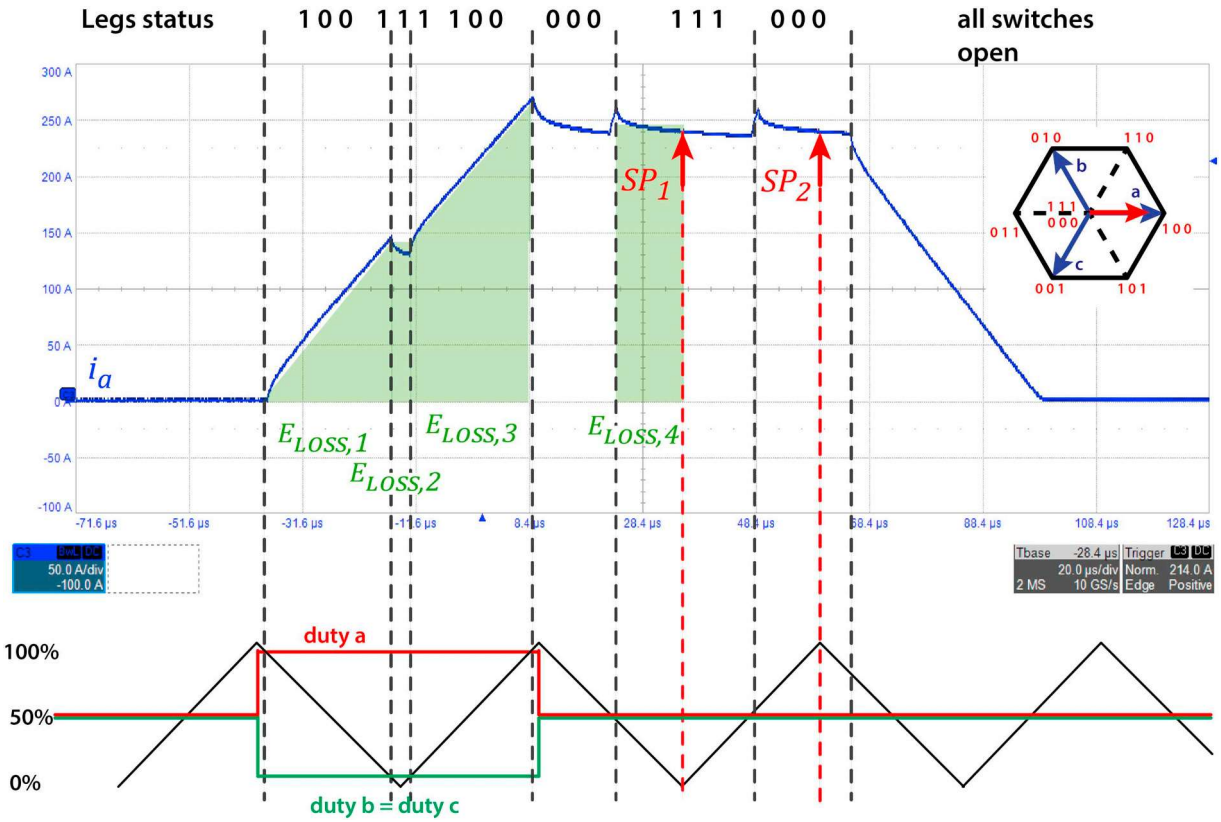


**Fig. 10.** Current pulse of 240 A on a+ axis during the calibration test. Phase current $i_a$ (50 A/div), $t$ = 20 µs/div.

of 180 A. The $R_{ON}$ increases by 62% when the junction temperature rises from 30 °C to 150 °C at a current of 240 A. Fig. 15 shows $R_{ON}$ as a function of the drain current for different values of junction temperature. In this case $R_{ON}$ increases only by 3% when the current varies from 30 to 240 A at a junction temperature of 150 °C. To obtain a good $\theta_j$ estimate, both dependencies must be considered.

It can be interesting to analyse the parametric dispersion between the six power MOSFETs. Fig. 16 shows $R_{ON}(\theta_j)$ at a drain current of 180 A of the six power MOSFETs. The measured $R_{ON}$ of the six MOSFETs is significantly different. SWaH and SWaL have a lower $R_{ON}$ compared to the other MOSFETs. For each inverter leg there is one power module, so SWaH and SWaL belong to the same power module. However, there is a small difference also between switches inside the same power module. The lower conduction resistance of the switches of the "leg A" was also verified with dedicated laboratory equipment and it is not due to errors of the measurement system. This lower resistance will also reflect in lower conduction losses and lower junction temperature as point out in the next paragraph. The $R_{ON}(\theta_j)$ curve provided in the datasheet is represented in Fig. 16 by a black dashed line. The real $R_{ON}$ obtained from the calibration test is sensibly lower than the

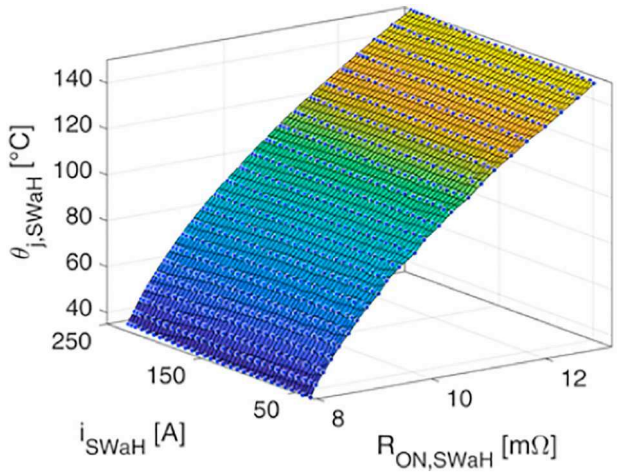


**Fig. 12.** Look-up table obtained from the current pulse test for the MOSFET SWaH for $i_{SWaH}$ > 30 A.

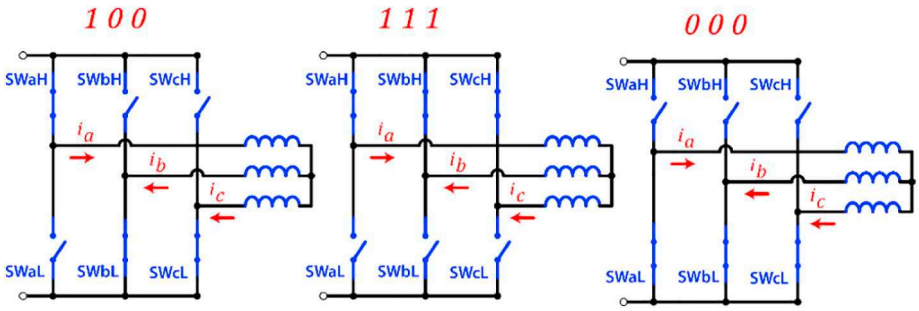


**Fig. 11.** Switches configurations during the pulses along a+ axis.

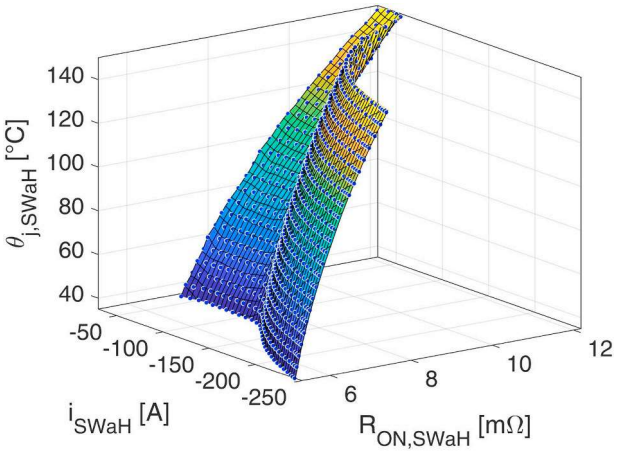


**Fig. 13.** Look-up table obtained from the current pulse test for the MOSFET SWaH for $i_{SWaH} < -30$ A.

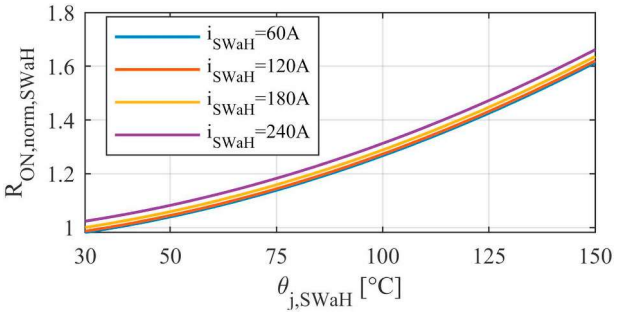


**Fig. 14.** Per-unit $R_{ON}$ as a function of the juntion temperature for positive drain currents. $R_{ON}$ is normalized respect to $R_{ON,\ SWaH}$ = 7.88 mΩ ($\theta_j$=30 °C, $i_{DS}$ = 180 A).

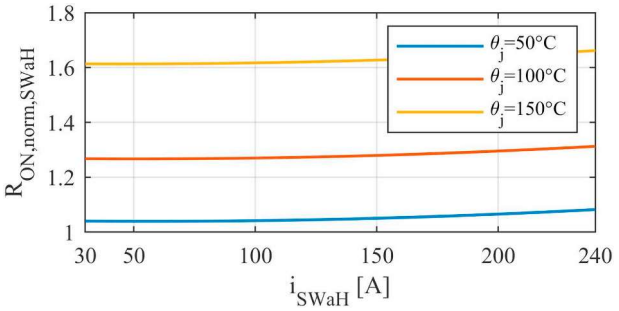


**Fig. 15.** Per-unit $R_{ON}$ as a function of the drain current at different juntion temperatures. $R_{ON}$ is normalized respect to $R_{ON,\ SWaH}$ = 7.88 mΩ ($\theta_j$ = 30 °C, $i_{DS}$ = 180 A).

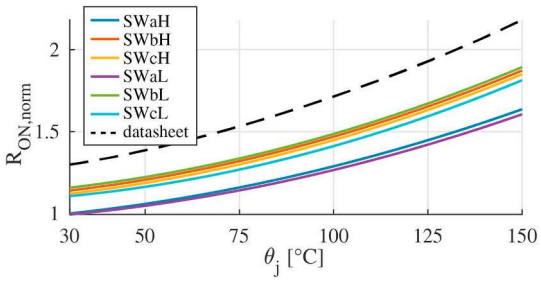


**Fig. 16.** Per-unit $R_{ON}$ as a function of $\theta_j$ for a drain current of 180 A. Comparison between the measured $R_{ON}$ of the six inverter MOSFETs and the datasheet reference value. $R_{ON}$ is normalized respect to $R_{ON,\ SWaH}$ = 7.88 mΩ ($\theta_j$ = 30 °C, $i_{DS}$ = 180 A).

**Table 2**
Coefficients of the polynomial function Eq. (1) computed by interpolating the MOSFETs LUTs (positive drain current) in the form $\theta_{j,\ SWx}$ ($i_{SWx}$,$R_{ON,\ SWx}$). x is the MOSFET current and y is the MOSFET conduction resistance.

| MOSFET | p00 | p10 | p01 | p11 | p02 |
|---|---|---|---|---|---|
| SWaH | −355.85 | −0.121 | 68,808 | 7.425 | −2,281,872 |
| SWbH | −349.40 | −0.164 | 60,432 | 8.508 | −1,783,226 |
| SWcH | −336.64 | −0.195 | 59,744 | 11.480 | −1,798,704 |
| SWaL | −376.30 | −0.201 | 75,766 | 12.614 | −2,671,784 |
| SWbL | −346.45 | −0.231 | 60,315 | 13.257 | −1,799,445 |
| SWcL | −361.72 | −0.232 | 66,504 | 13.608 | −2,129,471 |

one provided in the datasheet (30–35% lower for the switch SWaL). The datasheet must consider the components parametric dispersion and usually the data provided are representative of a worst case scenario. The value provided in the datasheet differs only of few $m\Omega$ compared to the measured one and for most application this is not critical. However, the datasheet data cannot be used to estimate $\theta_j$. As said the obtained results can be interpolated using a polynomial function Eq. (1), where x is the current of the MOSFET ($i_{DS}$) and y is its conduction resistance ($R_{ON}$). The coefficients of the polynomial function for the six MOSFETs are reported in Table 2.

$$\theta_{j,est,SWx} = p00 + p10 * x + p01 * y + p11 * x * y + p02 * y\text{^}2 \quad (1)$$

## 8. Online junction temperature estimation

The $\theta_j$ of all the six MOSFETs can be real-time estimated using the functional block diagram shown in Fig. 5. All the tests were performed at a switching frequency of 20 kHz and the $V_{ON}$ was measured once per period. Consequently, the temperature was estimated at each PWM period (50 µs). $\theta_j$ is estimated only for positive drain currents > 70 A, so to have reliable temperature estimations. At low values of drain currents, $\theta_{j,\ est}$ tends to be less accurate due to poor noise to signal ratio at low value of $v_{ON}$. The 70 A limit is a precautionary value so to obtain a reliable estimate of the junction temperature. Experimental results are shown in Fig. 17. The inverter imposes a 210 A pk current at 0.5 Hz to a 33 µH three phase load inductor. The top plot shows the measured output phase currents while the bottom plot shows the estimated junction temperature of the six MOSFETs and the measured heatsink temperature. During the test, the heatsink temperature measured using the two PTC thermistors is 50 °C and remains approximately constant. However, the $\theta_{j,\ est}$ of the MOSFETs is characterized by large thermal swings and $\theta_{j,\ est,\ max}$ reaches 153 °C. When the junction temperature

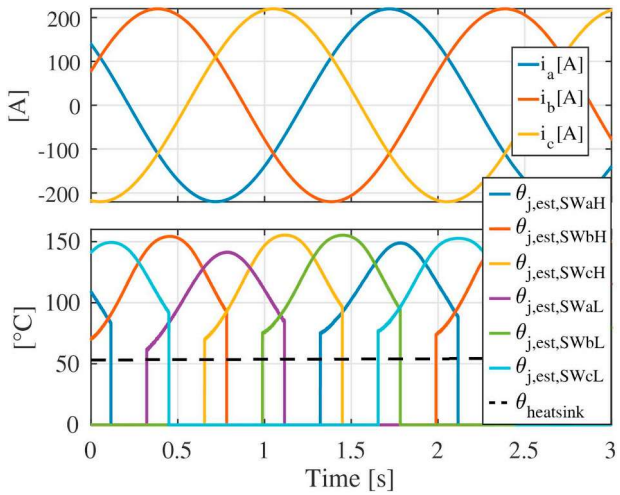


**Fig. 17.** Top: sinusoidal output phase currents at 0.5 Hz. Bottom: $\theta_{j,\ est}$ of the six MOSFETs and measured heatsink temperature.

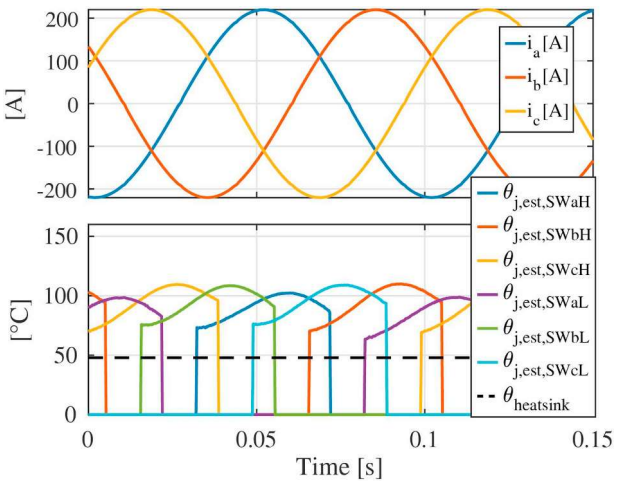


**Fig. 18.** Top: sinusoidal output phase currents at 10 Hz. Bottom: $\theta_{j,\ est}$ of the six MOSFETs and measured heatsink temperature.

cannot be determined is set to zero. In Fig. 18 the same test was performed increasing the fundamental frequency of the sinusoidal current to 10 Hz. The temperature swing of the MOSFETs is reduced due to the package thermal impedance that act as a "filter". In this case the maximum junction temperature value is "only" 115 °C.

## 9. Active junction temperature limitation

The maximum junction temperature of the power MOSFETs can be limited by reducing the converter output current. In a three-phase system without neutral wire, the output current can be represented by a rotating vector as shown in Fig. 19. $i_{ref}$ is the output reference current, while $i_{ref,\ lim}$ is the "limited" current obtained from the junction temperature limiter shown in Fig. 20. If $\theta_j$ of one of the six MOSFETs exceeds $\theta_{j,\ ref,\ max}$, $i_{ref}$ is reduced to $i_{ref,\ lim}$. If no overtemperature is detected $i_{ref}$ equals $i_{ref,\ lim}$. Depending on the final application, different solutions can be implemented to keep the maximum junction temperature of the semiconductors under control.

When a three-phase output current is imposed like in Fig. 17, the maximum junction temperature is the positive envelope of the junction temperatures of the six MOSFETs. This positive envelope is far from being constant. Consequently, if a simple PI regulator is used to limit the maximum current, the output current will be distorted.

To avoid excessive "distortions" of the output current, the temperature limiter shown in Fig. 20 was implemented. $\theta_{j,\ ref,\ max}$ is the maximum allowable junction temperature, this value can be set depending on the application and on the desired safety margin. $\theta_{j,\ est,\ max}$ is the maximum value of the six junction temperatures of the MOSFETs. $\theta_{j,\ ref,\ max}$ is filtered using a first order Low Pass Filter (5 Hz pole). The

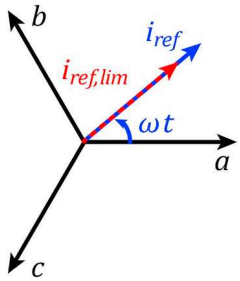


**Fig. 19.** Reference current vector (blue) rotating on 'abc' space and limited current vector (red) obtained from the temperature limitator shown in Fig. 20. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

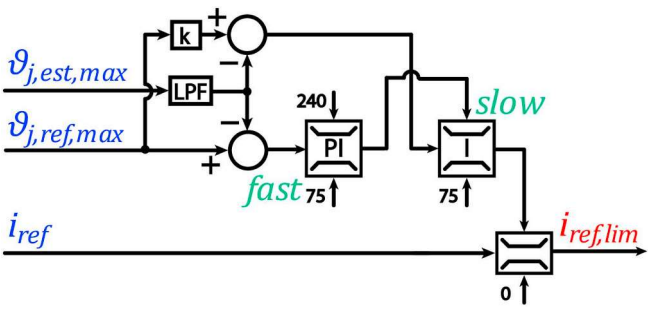


**Fig. 20.** Functional block of the online junction temperature limitator.

maximum allowable junction temperature $\theta_{j,\ ref,\ max}$ is limited using a "fast" PI (proportional-integral) regulator and a "slow" I (integral) regulator. When an over temperature is detected the fast PI regulator immediately reacts lowering the positive saturation limit of the slow I regulator, which in turn limits the maximum allowable output current. When the junction temperature drops under $\theta_{j,\ ref,\ max}$, the fast PI regulator immediately reacts increasing its output, while the slow I regulator starts increasing slowly. As a result, the output allowable current will slowly increase. In other words, the proposed regulator is very fast in reducing the maximum allowable current in case of over temperature, but it is slow in increasing the maximum allowable current when the temperature drops to a safe range. Furthermore a "k" coefficient was added. Its value varies between 0.96 and 1 depending on the reference of the reference output current. When the frequency is 0.5 Hz or lower, "k" is equal to 0.96 and it rises linearly to 1 when the frequency reaches 7 Hz. This coefficient is used to lower the reference of the slow I regulator, thus avoiding the intervention of the fast PI regulator when the converter is working in steady state. The bandwidth of the I regulator is also adjusted according to the reference frequency of the output current. At low frequency the bandwidth is lower than at high frequency.

An example of experimental result is provided in Fig. 21 where the output reference current represented by a blue dashed line is set to 220 A. During the converter start up the output current starts increasing. However, when $\theta_j$ of one of the six MOSFETs reaches $\theta_{j,\ ref,\ max}$, the fast PI immediately reduces the output current. This causes a distortion of the output current but avoids exceeding $\theta_{j,\ ref,\ max}$. Then the slow I regulator takes control maintaining a sinusoidal output current. After 3.2 s the output current frequency is increased from 1 Hz to 40 Hz, and again the thermal capacity of the component makes it

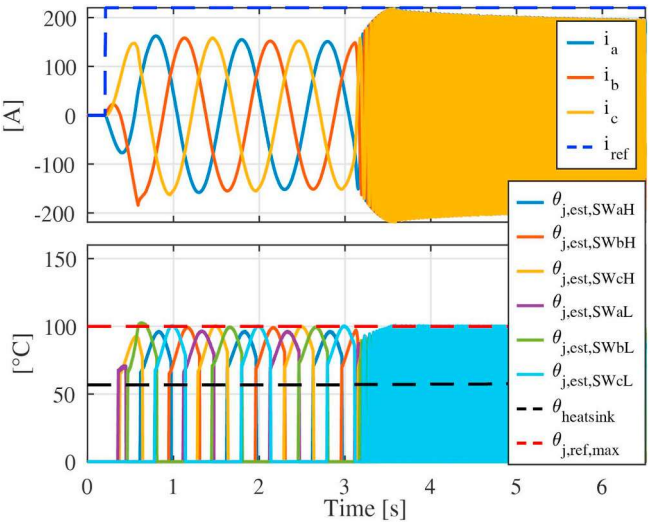


**Fig. 21.** Maximum junction temperature limitation. Output current frequency varied from 1 Hz to 40 Hz.

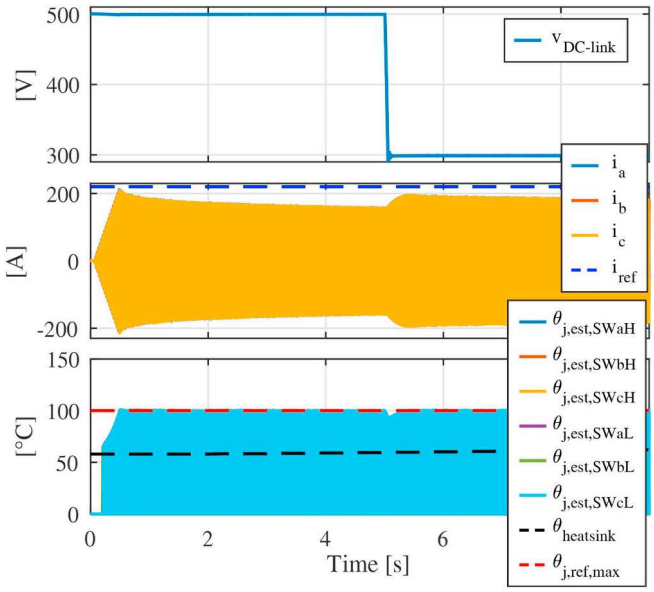


**Fig. 22.** Maximum junction temperature limitation. $v_{DC-link}$ step-varied from 500 to 300 V.

possible to increase the maximum allowable current.

A second example is provided in Fig. 22 where the converter supplies a 40 Hz sinusoidal current with $\theta_{j,\ ref,\ max}$ set to 100 °C. The top plot shows the DC-link voltage that is step varied from 500 V to 300 V. When the DC-link voltage decreases for the same value of $\theta_{j,\ ref,\ max}$ the maximum allowable output current increases. This is possible because of a reduction of the switching losses due to the lower DC-link voltage.

This paper shows that because of the junction temperature estimation, it is possible to actively limit the maximum allowable junction temperature of the power semiconductor of a three-phase inverter. The authors are aware that more sophisticated and performing control strategies can be implemented like in [26,32–34].

## 10. Conclusions

### 10.1. Strengths and limitations

The main strengths of the proposed methodology are:

- Temperature estimation has a high sampling rate and fast-dynamic response and does not affect the normal operations of the converter.
- The TSEP calibration can be performed directly on the converter without additional equipment. This is a very important point, because the same measurement system that is used to map the semiconductor is also used to estimate its temperature. Consequently, offsets and nonlinearities of the $v_{ON}$ measurement system that are constant over time do not introduce any error in the temperature estimation.
- The additional circuitry for the $v_{ON}$ measurement is rather standard and low cost. To furtherly reduced this cost, the $v_{ON}$ measurement circuitry can be embedded in the gate driver chip, like the implementation of the desaturation protection.
- The $v_{ON}$ measurement system does not require any tuning, provided that it is stable over time.
- No complex computation is involved.
- The temperature estimation can be implemented using a classical PWM modulator. The converter embeds an FPGA only for achieving better flexibility, however it is not necessary for the calibration and for the online temperature estimation. A classical microcontroller normally used for motor control is enough.

Current limitations of the methods are:

- The junction temperature of the MOSFET cannot be estimated for negative values of $i_{DS}$, however, this case tends not to be thermally critical, as the losses are shared between the antiparallel diode and the power MOSFET. Furthermore, when $i_{DS} < 0$ the commutation losses in the device are negligible compared to the case of $i_{DS} > 0$. If no antiparallel diode is present the temperature of the MOSFET can be estimated also for negative values of $i_{DS}$ due to the symmetrical behaviour of the MOSFET. The same power module is also available without the antiparallel diode and it will be tested in the future.
- If the current in the device is too small ($< 70$ A, absolute value for the evaluated power module), $\theta_{j,\ est}$ tends to be less accurate due to poor noise to signal ratio at low value of $v_{ON}$. However, also this case is not thermally critical.
- It is necessary to preheat the heatsink of the up to the maximum temperature that we want to estimate. This is a limitation, especially for liquid cooled heatsink that needs to be temporarily replaced or emptied from the cooling liquid. Further studies are underway to reduce the calibration temperature.

### 10.2. Aging

It is well known from the literature that the $R_{ON}$ increases with the aging of the component [28–30]. The $R_{ON}$ increase is due to the combined effects of the package and chip degradation ($V_{th}$ shift) [30]. This increase leads to overestimating the junction temperature. In one of our previous works [31] we used the same junction temperature estimation technique on a SiC power module subjected to accelerated aging. In this specific case, the junction temperature over estimation just before the failure of the component was between 4 and 6 °C. This temperature over estimation was modest, however we cannot generalize this result. As reported in [30], the $R_{ON}$ increment can also be higher depending on the specific device and on the failure mechanism.

If the temperature feedback is used to limit the maximum allowable current in the converter, this will lead to over limit the current and the converter will underperform. The user can perform a new calibration test or accept the derating of the converter.

### 10.3. Threshold voltage instability

The threshold voltage instability is an important phenomenon that is particularly pronounced in SiC MOSFETs [13]. The threshold voltage of SiC MOSFETs is subject to fluctuations, which depend on the previous gate bias state. According to [13] the threshold voltage variation goes in both directions, typically from $+1$ V to $-3$ V. This voltage variation is fully recoverable (not permanent) and is not harmful for most of applications. However, a variation of the threshold voltage means also a $R_{ON}$ variation. It is not trivial to evaluate the impact of this phenomenon on the temperature estimation. Many variables need to be considered, like the gate bias voltages, the delay between the commutation instant and the $V_{ON}$ sampling instant and the junction temperature. According to the data presented in [13], this phenomenon should not significantly affect the temperature estimate in our test bench, however further studies will be needed to investigate this aspect.

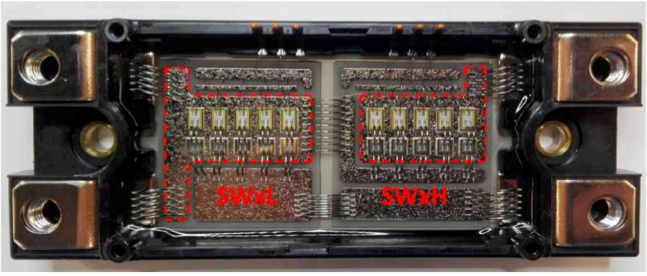


**Fig. 23.** Internal layout of the adopted power module.

### 10.4. Considerations

Each power MOSFET consists of five dies connected in parallel as shown in Fig. 23. Despite the good matching usually provided by the manufacturer, small differences in the temperature of the devices are likely. Furthermore, the temperature distribution across the single die is not uniform, and local hotspots are present [27]. For these reasons, an appropriate safety margin must be maintained.

It was not possible to provide a validation using a thermal camera, due to the lack of power modules without the filling gel and due to difficulty in providing visual access to the die while the module is mounted on the converter. However, in [27] the same technique was used for an H-bridge converter and a validation with a thermal camera was provided.

### 10.5. Applicability to different topologies and semiconductors

The same methodology can be virtually used with any type of switching converter, independently from the architecture. However, depending on the topology of the converter different calibration tests need to be elaborated. The same methodology applies also to Si MOSFETs and IGBTs.

### 10.6. Prospect applications

The applications that would most benefit in using the proposed methodology are:

- Applications with frequent transient overload like automotive.
- Safety critical applications where failure or malfunction may result in damage to people.
- Applications where the downtime is costly such as oil and gas.
- High power applications where the safety margins on the component size are costly.
- High power density applications where the cooling system and components must be fully exploited.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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