Digital-based analog processing in nanoscale CMOS ICs for IoT applications

Digital-based Analog Processing in Nanoscale CMOS ICs for IoT Applications

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Abstract

Over the past two decades, it is evident that there have been significant improvements (and it is expected to) in CMOS digital circuits when compared against analog building block performance. Digital circuits have been taking advantage of CMOS technology scaling in terms of speed, power consumption, and cost, while the techniques running behind the analog signal processing are still lagging. There has been an increasing trend in finding alternative IC design strategies to implement analog functions exploiting digital-in-concept design methodologies to decrease this historical gap. This idea of re-thinking analog functions in digital terms has shown that Analog ICs blocks can also avail of the feature-size shrinking and energy efficiency of new technologies. This poster shows the advanced of this field in the above scenario, proposing new digital-based analog blocks and proving their performance through silicon measurements.

Novel contributions

- Novel Ultra Low Voltage (ULV) Digital-Based (DB) analog blocks, such as Operational Transconductance Amplifier, are proposed.

Research Collaborations

UFRGS Universidade Federal do Rio Grande do Sul + Politecnico di Torino + NUS National University of Singapore

Joint Degree PhD

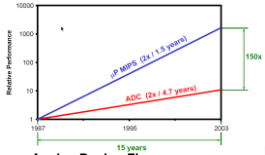
Research context and motivation

- **IoT Application and Low Power requirement:**

(Source: McKinsey Global Institute.)

- **Ultra Low Power (ULP)** systems disruptive IoT applications: logistics, navigation, health and fitness.
- Expected market share of **$2.5 trillion** at 2025.
- **CMOS** is **the IoT technology**.
- **ULP CMOS analog interfaces** always are needed.

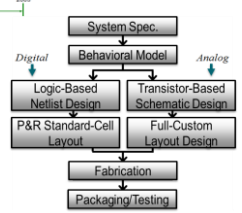
- **Analog versus Digital:**



(Comparison performance btw CMOS Digital and Analog system over time. - B. Murmann .: Digitally Assisted Analog Circuits, 2006)

Analog Design Flow:
- Longest design time
- Manual layout
- Labor intensive
- Highest performance

Digital Design Flow:
- Automatic
- Portability
- Time-to-market
- Reasonable performance

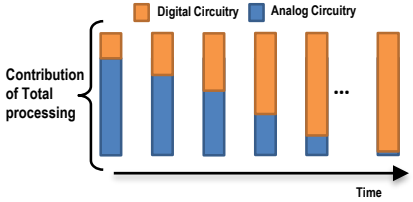


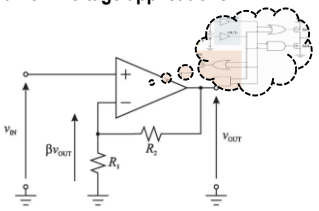
Submitted/published works and Awards

- [1] P. S. Crovetti, F. Musolino, O. Aiello, **P. Toledo** and R. Rubino, "breaking the boundaries between analogue and digital," Electronics Letters, vol. 55, no. 12, pp. 672-673, 13 6 2019.
- [2] **P. Toledo**, et all. , "A 300mV-Supply, 2nW-Power, 80pF-Load CMOS Digital-Based OTA for IoT Interfaces", International Conference on Electronics Circuits and Systems, 2019 **[best student paper]**
- [3] **P. Toledo**, O. Aiello, P. Crovetti "A 300mV-Supply Standard-Cell-Based OTA with Digital PWM Offset Calibration", IEEE Nordic Circuits and Systems Conference, 2019
- [4] **P. Toledo**, Crovetti, P.; Klimach, H.; Bampi, S. "Dynamic and Static Calibration of Ultra-Low-Voltage, Digital-Based Operational Transconductance Amplifiers". Electronics 2020
- [7] **P. Toledo**, Crovetti, P. Aielo, O. Alioto, M . "Fully-Digital Rail-to-Rail OTA with Sub-1,000 µm² Area, 250-mV Minimum Supply and nW Power at 150-pF Load in 180nm" Solid State Circuit Letters, 2020
- [8] Aielo, O. Crovetti, P. **P. Toledo**, Alioto, M. "Rail-to-Rail Dynamic Voltage Comparator Scalable down to pW-Range Power and 0.15V Supply" Transactions on Circuits and Systems II, 2020 (submitted)
- [11] Demo video link: https://www.dropbox.com/s/jr1kajrhparuwm6/s264711_PosterVideo.mp4?dl=0 and https://www.youtube.com/watch?v=unTmJKVgv4Y

Addressed research questions/problems

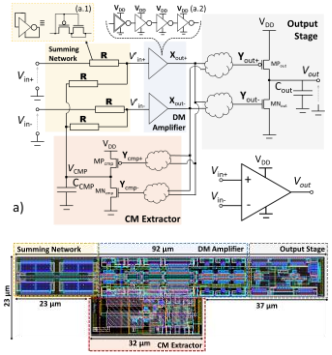
- There has been an **increasing trend** in finding alternative IC design strategies **to implement analog functions using digital-in-concept design.**
- **Can we design OTAs and Comparator using only digital logic gates targeting Ultra Low Voltage applications ?**

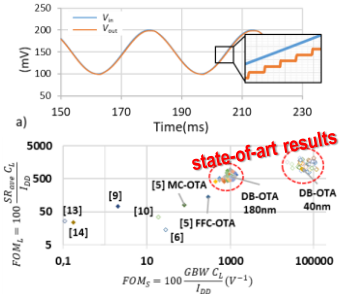




Adopted methodologies

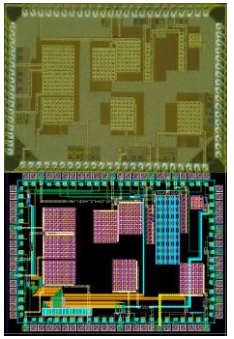
- In [2], an 180nm ULV DB-OTA has been proposed following digital design criteria





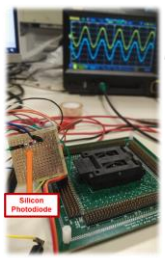
- [5] Lv, L., JSSC, 2019
- [6] Ferreira, L.,TCASI, 2014
- [9] Veldandi, H.,CSSP, 2018
- [10] Abdelfattah,O., TCASI, 2015
- [13] Chatterjee, S, JSSC, 2005
- [14] Ferreira, L. TCASII, 2007

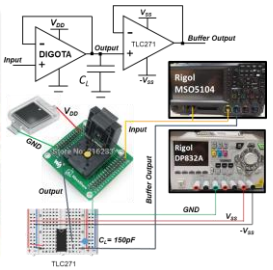
- Based on [2], several others ULV Digital-based analog blocks have been fabricated in TSMC 180nm

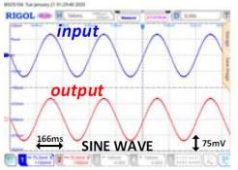


- Total Area: 1500 µm x 2000 µm
- TSMC 180 nm
- 82 PADS
- 2 New DB-OTA
- 2 New DB-Comparator
- 1 New DB-Oscillator
- 1 DB-Filter

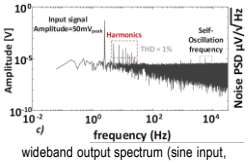
- In [7], a new DIGOTA is directly powered by a small energy harvester (7-mm2 solar cell) at dim light <100 lux (dark overcast day).



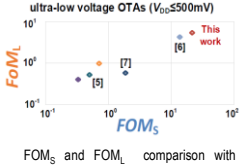




sine wave response in voltage follower configuration (3-Hz frequency, 75-mV ampl)



wideband output spectrum (sine input, 2.5-Hz, 75-mV amplitude)



FOM_S and FOM_L comparison with OTAs with V_{DD}≤500mV

Conclusion

- Several ULV digital-based analog building blocks have been proposed. • Development of a semi-automatic testbench is herein reported.
- A compact and energy-efficient digital OTA has been in 180 nm and its ability to operate at ultra-low voltage and power has been demonstrated in the context of energy-autonomous sensor nodes, as directly powered by a small energy harvester.