The first ASIC prototype of a 28 nm time-space front-end electronics for real-time tracking

PROCEEDINGS OF SCIENCE

The first ASIC prototype of a 28 nm time-space front-end electronics for real-time tracking

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A front-end ASIC for 4D tracking is presented. The prototype includes the block necessary to build a pixel front-end chain for timing measurement, as independent circuits. The architecture includes a charge-sensitive amplifier, a discriminator with programmable threshold, and a time-to-digital converter. The blocks were designed with target specifications in mind including: an area occupation of 55 µm × 55 µm, a power consumption tens of micro ampere per channel and timing a resolution of at least 100 ps. The prototype has been designed and integrated in 28 nm CMOS technology. The presented design is part of the TimeSpOT project which aims to reach a high-resolution particle tracking both in space and in time, in order to provide front-end circuitry suitable for next generation colliders.

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1. Introduction

The next-generation of colliders will will see an increase on the number of events per bunch crossing by at least factor 5. Future trackers should be able to perform a tight selection of events, even in case of high pile-up (150 to 200) and high background noise [1]. The problem of track recognition can be simplified by adding time information to spatial one, thus providing 4D data at the pixel output. The TimeSPOT project [2], funded by INFN, aims at the development of a complete processing chain for particle detection suitable for future HEP experiments. In the case of the High Luminosity phase of LHC (HL-LHC) the expected event rate per unit area observed by detectors will be $3\,\mathrm{GHzcm}^{-2}$, while the total dose which the instrumentation will sustain will be equivalent to $10^{14}\,\mathrm{cm}^{-2}$ 1 MeV neutrons. Hybrid pixel detectors with 3D sensors were selected due to their intrinsic radiation hardness, this approach defines the minimum pixel pitch on the base of minimum dimension of the bump-bond contacts used for sensor-electronics coupling. A pixel size of $55\,\mu\mathrm{m} \times 55\,\mu\mathrm{m}$ was selected and thus the 2D portion of the spatial resolution. Evaluation on 4D tracking algorithms suggests that, in order to be advantageous compared to standard 3D techniques, a time resolution less than 100 ps will be required, this value has been evaluated considering this area resolution and a LHCb velo-like geometry [3]. Considering the interest in only detecting the space-time position of the interaction point, the implemented Front-End (FE) architecture will be a binary one with a charge pre-amplification stage followed by a discriminator and a Time to Digital Converter (TDC) for the digitization of the timing information. Considering the chosen pixel geometry the average event rate will be 75 kHz per channel. This value has guided the design of the FE both in terms of analog circuits speed and on number of TDCs per channel. The power budget available to electronics is constrained by the power dissipation system employed in the experiments which ranges from $300\,\mathrm{mWcm}^{-2}$ to $1.1\,\mathrm{Wcm}^{-2}$, imposing a per-pixel power consumption in the range of tens of micro watt.

The project will exploit the potential of silicon [4] and diamond [5] 3D sensors, and will take advantage of the high speed and the radiation hardness performance provided by the 28 nm CMOS technology. The first prototype ASIC includes all the relevant blocks of the FE including the analog chain (section 2), three different TDC architectures (section 3) and output interface (section

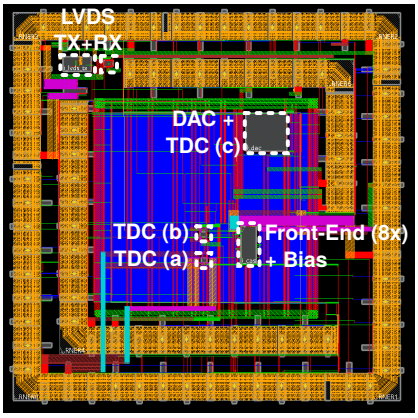


Figure 1: **Layout of the first prototype chip** ($1.4\,\mathrm{mm} \times 1.4\,\mathrm{mm}$)**.**

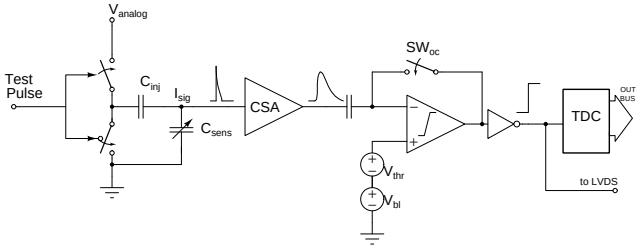


Figure 2: **Schematic of the Analog Front-End: the digital pulse coming from LVDS receiver is converted in a current signal by the means of C_{inj}, the charge is then integrated by the CSA and finally compared to an external voltage threshold by the discriminator. The digital output can than be sent either to an LVDS transmitter or to one of the three TDCs. Discriminator offset compensation can be performed my acting on the switch SW_{oc} .**

4). In the first prototype, circuit blocks can be characterized individually, or they can be connected together to form a processing chain. The layout of this first prototype is presented in Fig. 1.

2. Analog Front-End

The function of this block is to provide fast voltage signal transient which is fed to the TDC in order accurately measure its phase in relation to a reference clock. The total system jitter must be small compared to the target 100 ps resolution. Moreover, in order to leave a significant power headroom to the digital part of the design, the system is designed to consume a total power less than 5 µW per channel, with the possibility to set the circuit to a high power mode by increasing the core amplifier bias current.

The analog FE is formed by a charge injection circuit which emulates sensor signals and impedance. The charge preamplifier is a Charge Sensitive Amplifier (CSA) with DC leakage current compensation. The discriminator is Leading Edge Discriminator with offset correction circuit to provide both baseline setting and equalization of per-channel variations [6]. A schematic of the system and a description of its operation are presented in Fig. 2.

The circuit occupies an area of 50 µm×10 µm. It exhibits encouraging performance in simulation, and the simulated results are presented in Table 1 and in Fig. 3. In this prototype the circuit is replicated in 8 independent channels with settable power consumption, input charge and sensor capacitance. Analog references and control signals are provided externally.

Input Signal	**Delta**		**Sensor**	
Power [µW]	**4.1**	**7.2**	**4.1**	**7.2**
G [mV fC^{-1}]	190	168	150	124
σ_n [mV]	2.8	2.0	2.8	2.0
ENC [e]	94	77	120	103
t_{pk} [ns]	16.4	7.7	18.2	10.2
t_A [ns]	2.1	2.1	4.2	3.5
TOT [ns]	100	98	79	78
SR [mV ns^{-1}]	53	98	39	68
σ_j [ps]	54	21	74	30
σ_p [ps]	66	65	67	66
σ_{mm} [ps]	33	26	40	29

Table 1: **Front-End Parameters in two power consumption regimes. Simulations in response to a 2 fC signal, both a delta-like signal (triangular with a charge development under 1 ps) and a realistic signal extracted from sensor physics simulations are presented. G: CSA gain; σ_n: rms noise; ENC: equivalent noise charge; t_{pk} and t_A: peaking and threshold crossing time, TOT: time over threshold; SR: slew-rate; σ_j: jitter; σ_p and σ_{mm}: standard deviations of t_A variations due to process and mismatch.**

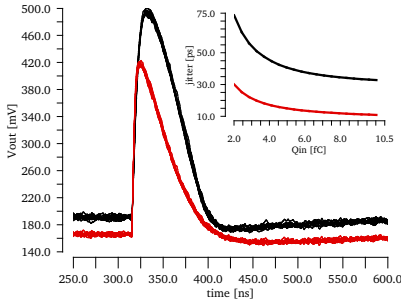
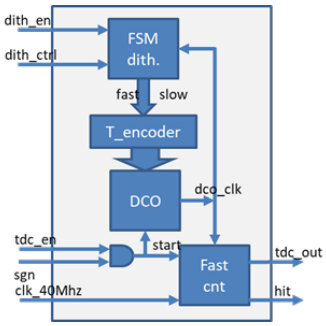


Figure 3: **Examples of CSA signals of 100 independent transient-noise simulation of CSA response to a 2 fC simulated sensor signal. Black curve: low-power (4.1 µW), red: high-power (7.2 µW). The inset is a plot of the jitter as a function of the input charge.**

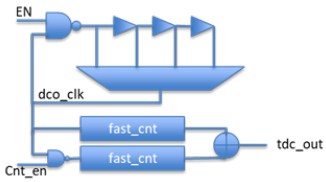
3. TDCs

On this chip we have tested three different TDC architectures that will process the output from the Front-End Discriminator. All the three TDCs are fully digital and they measure the phase of the incoming input signal with respect to a 40 MHz reference clock.

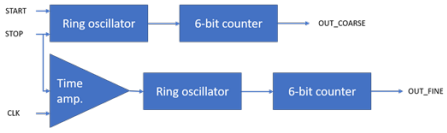
Architecture (a), shown in Fig. 4a, is based on a design realized in 130 nm technology for the LHCb muon detector upgrade [7]. The phase measurement is activated by the incoming signal that switches on the Digitally Controlled Oscillator (DCO). The DCO clock drives a fast counter, which "counts" the number of DCO clock periods. When the rise-edge master clock arrives, the fast counter (and the DCO) is stopped, the measurement



(a) **DCO**



(b) **Tapped delay**



(c) **Time Amplification**

Figure 4: **Implemented TDC architectures.**

is completed. To reduce the systematic error inherent to a digital delay chain, the same dithering system described in [7] has also been implemented in this scheme.

Architecture (b), shown in Fig. 4b, is a classic digital tapped delay line with delay line length programmable in order to compensate the difference between different channels. In order to increase the resolution, it employs two identical counters working on the opposite clock edge. The second counter can be switched off to save power at the expense of time resolution.

Architecture (c), shown in Fig. 4c, is based on a two-step conversion using Time Amplification (TA) for fine measurement. TA is a method to stretch a time difference by a given amplification factor so that a short time interval T_1 can be converted into a much longer time interval $T_2 = AT_1$. The measurement is activated by the incoming signal that starts the first Ring Oscillator. When the rise-edge master clock arrives, the first 6-bit counter contains the coarse value of the conversion. In the second step, the first oscillator is slowed down to amplify the residual interval (T_1, too short to be measured by the 6-bit converter). The second ring-oscillator will count the number of oscillations needed for the first oscillator to produce a new clock tick (T_2) obtaining the least-significant bits of the conversion. Table 2 summarizes the main characteristics of the three TDC architectures. The advantage with respect to the 130 nm design is mainly in size (90 µm × 130 µm vs. 23 µm × 22 µm) and max resolution (750 ps vs 190 ps LSB), as we can see from reference [7]. For power consumption the comparison between the two technologies shows a slightly advantage for the 130 nm technology, as we can expect from the fact the leakage is larger in 28 nm technology as well as the switching power, caused by the higher adopted frequency. According to Fig. 2, the third scheme shows a power consumption during conversion lower than the others two (65 µW against more than 1 mW). This is due to the fact that the first two schemes work at higher frequency, while the third, being a time amplifier, works at lower frequency, obtaining the same order of resolution thanks to the time amplification. On the contrary, the power consumption at rest is lower in the first two schemes. The reason is related to the fact that the third is a full-custom architecture which requires some bias current to work, that increases the power consumption at rest. The 3 TDC architectures show different pros and cons: (a) and (b) can be implemented in an all-digital flow, thus allowing relatively simple design migration to more advanced technology nodes; (c) requires a full-custom implementation, making design migration more complex, but allows to reduce the

	First Scheme	Second scheme	Third scheme
Size (μm^2)	23 x 22	27 x 22	23 x 21
LSB (ps)	190	50	22
RMS (ps)	47	15	37
Power Active (μW)	1200	1200	65
Power Standby (μW)	10	10	34

Table 2: **TDC characteristics.**

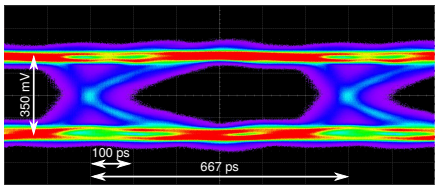


Figure 5: **LVDS measured eye diagram.**

power consumption by using slower oscillator thanks to the two-step conversion architecture.

4. IO interfaces

The output data will be serialized by an interface which provides an LVDS output. An LVDS receiver and an LVDS transmitter have been integrated in the prototype, and they can be connected in loopback configuration for testing purposes. Measurements (in Fig. 5) demonstrate that the LVDS interface can operate up to 1.5 Gbit/s with a Pseudo-Random Binary Sequence (PRBS-7), with a Bit Error Ratio less than 10^{-15} with a total current consumption of 2.7 mA.

5. Conclusion

Simulated performance shows that the proposed 28 nm hybrid pixel FE architecture can be suitable for high luminosity 4D Trackers in terms of resolution, power consumption, area occupation and per-channel variation. Preliminary measurements on the LVDS blocks indicates that the 28 nm technology can achieve the required performance. A first test chip has been manufactured and will enable characterization and radiation tolerance tests on single blocks as well as on the full FE chain. A second prototype which will include an array of a thousand channels is now under development.

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