A Pixel Read-Out Front-End in 28 nm CMOS with Time and Space Resolution

A Pixel Read-Out Front-End in 28 nm CMOS with Time and Space Resolution

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Abstract—Future high luminosity colliders will require front-end electronics with unprecedented performance, both in space and time resolution (tens of micrometers and tens of picoseconds) and in radiation hardness (tens of megagray). Moreover, the high number of events will generate an enormous quantity of data (some terabits per second), and the limited bandwidth requires to perform data selection as close as possible to the front-end stage, to reduce the amount of data transmitted and stored for off-line analysis.

The TimeSpOT (TIME and SPace real-time Operating Tracker) project, funded by INFN, is developing a complete demonstrator of a tracking device including all the features needed for future high luminosity experiments.

In this presentation, we describe the first prototype of the read-out electronics in 28 nm CMOS technology. The modules of the front-end circuitry have been designed and integrated in a test chip, which will allow us to characterize each block separately, and to connect them in a processing chain to evaluate the overall performance.

Index Terms—Pixel detector, tracking, time resolution.

I. Introduction

HIGH luminosities planned at colliders of the next decades pose very severe requirements on vertex detector systems in terms of space resolution, radiation hardness, and data throughput. The expected event pile-up (in the order of 100) requires to add high resolution time measurements already at the single pixel level. This demand pushes towards a new concept of vertex detector system, where all these features must operate at the same time [1], [2].

The capability to satisfy these requirements is decisive for the high energy physics program at future colliders. The Phase-II vertex detector of the LHCb experiment at CERN will be required to operate at an instantaneous luminosity of $2 \leq 10^{34}$ cm^{-2}s^{-1}, with an average of 50 visible proton-proton interactions per crossing and 1500 to 3500 charged particles from the interaction region, within the detector acceptance. Simulation studies demonstrate that, when operating the Phase-I vertex detector in such conditions, spurious hit contamination would increase the fraction of mis-associated (ghost) tracks from 1.6 % to 40 %, and total tracking efficiency would reduce from 99 % to 96 % [3]. Adding a precise measurement of the track's time would restore the reconstruction performances at the required levels.

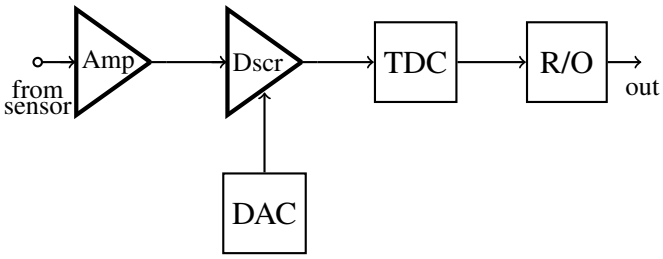

Fig. 1. Block diagram of the pixel read-out circuit.

The general requirements of next generation vertex detectors can be summarized in a few key numbers:

- Pixel pitch: smaller than 100 µm;
- Time resolution on single hit: order of 100 ps or better;
- NIEL radiation resistance: 10^{16} to 10^{17} 1-MeV n_{eq} cm^{-2}.

In addition, the complexity of high-luminosity events at the interaction point urges the need of an improved performance in real-time tracking reconstruction. Fast tracking algorithms and devices are a priority in the system design.

II. Front-End Electronics

The design of dedicated electronics is crucial to fully exploit sensor timing performance. Sensor geometry fixes important constraints about the available area for the single channel, which is about 50 µm × 50 µm. Optimum performance can be obtained only in the strict interplay of sensor and electronics.

Within the TimeSpOT project [4], we are designing a classical linear chain dedicated to the specific characteristics of optimized 3D sensors [5], [6]. The important innovation of this approach consists in the use of very small feature size CMOS, at the 28 nm technology node. We intend to endow the single pixel circuit with the maximum set of functionalities for high system performance in tracking operations, and in particular with time measuring capabilities. This approach is not viable

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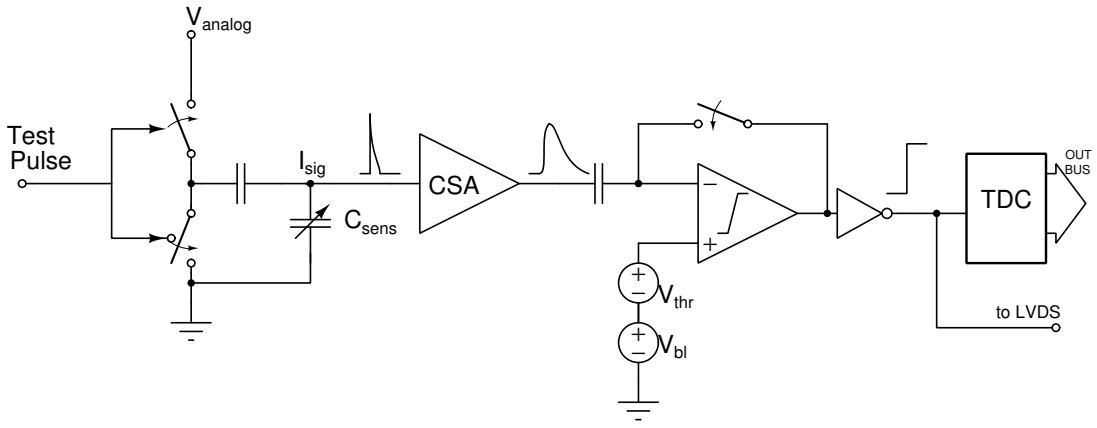


Fig. 2. Schematic diagram of the front-end.

in CMOS technologies already used to design electronic circuits for the Phase-II upgrades (e.g., in 65 nm CMOS) and involves remarkable challenges in front-end design.

Fig. 1 shows the front-end pixel architecture. Every single channel or group of channels should be served by a TDC with suitable time resolution (100 ps or better).

The first prototype integrates a full pixel readout chain stimulated with an on-chip pulse-test generator, and some utility blocks. The full pixel readout chain is made of an Analog Front-End (AFE) and a Time Digital Converter (TDC), which has been integrated in different versions. The AFE and the TDCs can be characterized together or separately. Utility blocks include a DAC, an OpAmp, and LVDS I/O interfaces.

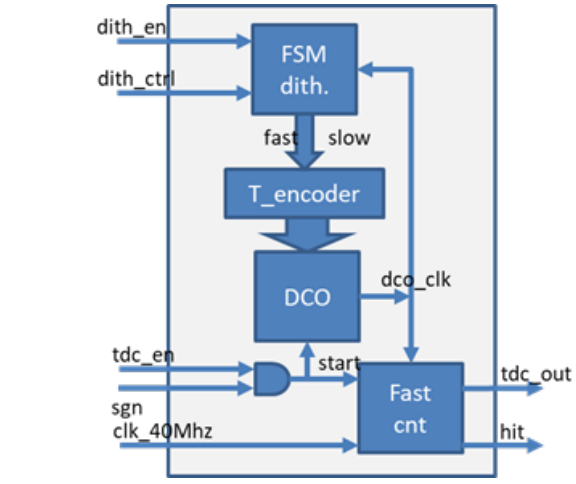
A. Analog Front-End

Fig. 2 shows a more detailed diagram of the first two stages (labelled 'Amp' and 'Dscr' in Fig. 1). The first stage of the chain is a Charge Sensitive Amplifier (CSA) with sensor leakage current compensation based on Krummenacher feedback. It features a charge to voltage gain of 150 mV/fC and signal duration time of 80 ns for the minimum signal. The CSA signal is compared with a voltage threshold using a Leading Edge Discriminator (LED) with auto-zero based offset compensation. The time difference between this pulse and a reference clock is digitized by TDC. This block was designed in order to produce output signal with an rms jitter value less than 100 ps for 2 fC or more of input charge, while having a total power consumption lower than 10 µW. A charge injection circuit is also integrated for both testing purpose and channel calibration [7].

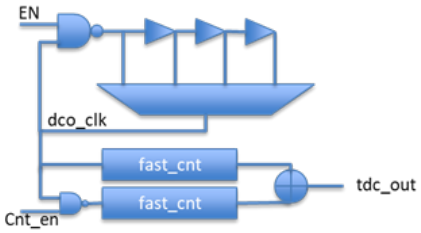
B. Time-to-Digital Converter

Three versions of the TDC have been designed.

The first TDC circuit, shown in Fig. 3(a), employs a fully-digital solution which has been already successfully implemented [8]. It is based on a synthesizable DCO, which drives a fast counter performing the phase measurement, with a resolution of about 50 ps (rms value). The TDC can use a dithering system to minimize the systematic errors due to discrete delay unit. The design has been translated from



(a)



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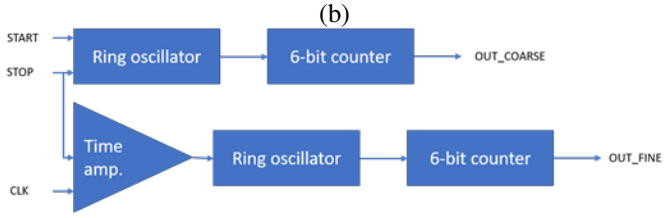

(c)

Fig. 3. TDC architectures: (a) 130 nm redesign from [8]; (b) tapped delay line; (c) two-step

130 nm CMOS technology to a more scaled 28 nm CMOS technology node, to profit from technology scaling.

The second scheme, shown in Fig. 3(b), is based on a classical tapped delay line closed to obtain a fast clock, that is

TABLE I
TIME-TO-DIGITAL CONVERTERS: POST-LAYOUT SIMULATIONS

	TDC1	TDC2	TDC3
Architecture	130 nm re-design [8]	tapped-delay line	two-step conversion
Size	23 µm × 22 µm	27 µm × 22 µm	23 µm × 21 µm
LSB	190 ps	50 ps	22 ps
rms error	47 ps	15 ps	37 ps
Active Power	1.2 mW	1.2 mW	0.065 mW
Stand-by Power	10 µW	10 µW	34 µW

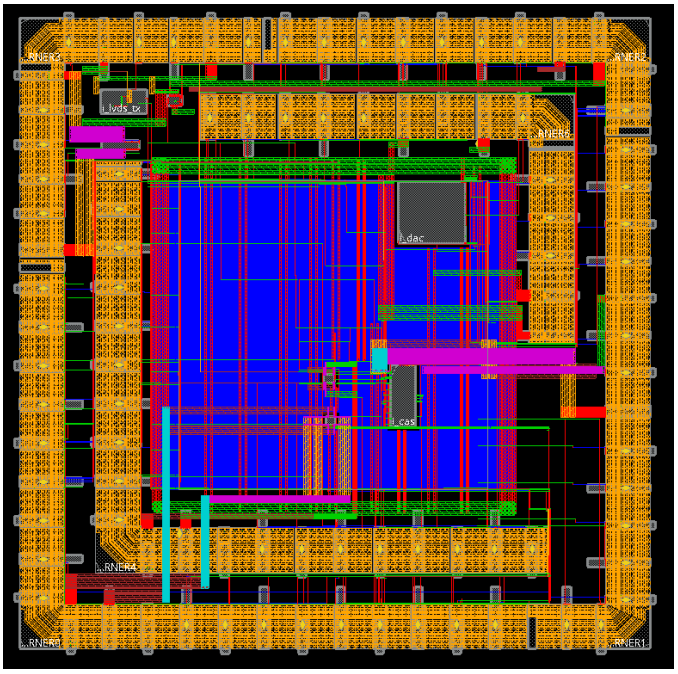

Fig. 4. Layout of the first chip prototype.

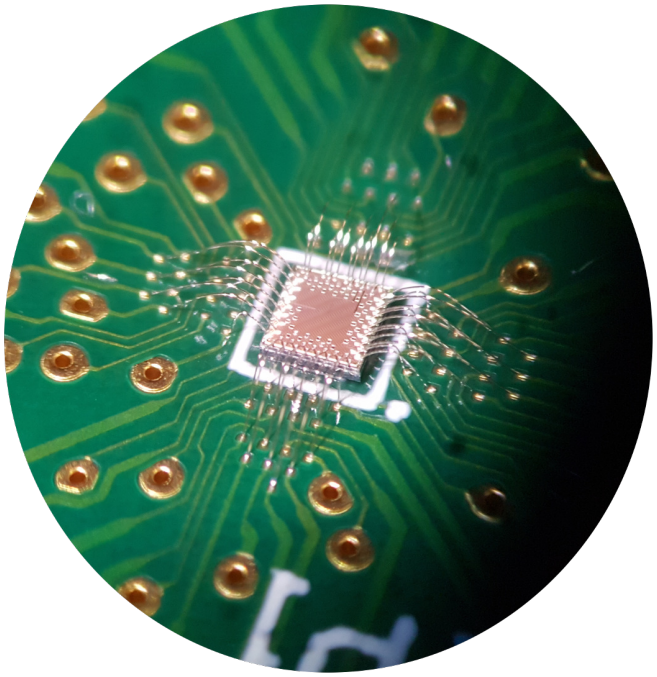

Fig. 5. Photograph of the chip wirebonded to the board for testing

used to drive two different fast counters working on opposite clock edges. The maximum resolution achieved from post-layout simulation is 15 ps (rms value). This architecture is fully digital, and the delay line can be adjusted in order to compensate difference between channels.

The third architecture is based on a two-step conversion using time amplification for fine measurement (Fig. 3(c)). The measurement is activated by the incoming signal that starts the first Ring Oscillator (RO). At the rising edge of the master clock, the first 6-bit counter contains the coarse value of the conversion. The residual (fine measure) is obtained by slowing down the first RO, and by starting a second RO. The number of periods needed by the first oscillator to produce a new clock tick is a properly amplified version of the residual time, and therefore the second 6-bit counter will contain the least-significant bits of the conversion. The maximum resolution achieved from post-layout simulation is 30 ps (rms value).

Table I summarizes the performance of the TDCs.

C. DAC

A digital-to-analog converter with 6-bit resolution provides the reference for the discriminator stage. The module is based on all-transistor R-2R network, where each resistor is made with a transistor operated in linear region. The reference current can be digitally trimmed to correct for PVT variations.

D. Read-out Interface

The data can be send in and out by an interface which convert Low-Voltage CMOS (LVCMOS) signals in Low-Voltage Differential Signaling (LVDS) signals. The LVDS interface with a similar design has been successfully tested in a different 28 nm technology [9].

III. FIRST CHIP PROTOTYPE

The first prototype has been designed to validate the functionality of single blocks. For this reason, the pad ring has been split in different domains. Each domain contains signals and power supplies for the corresponding block. Power supplies have been physically separated to mitigate noise. The chip is connected externally through 84 pads placed over two staggered rings, as shown in Fig. 4. The total silicon area is 1.4 mm × 1.4 mm.

Fig. 5 shows the chip assembled on the test board.

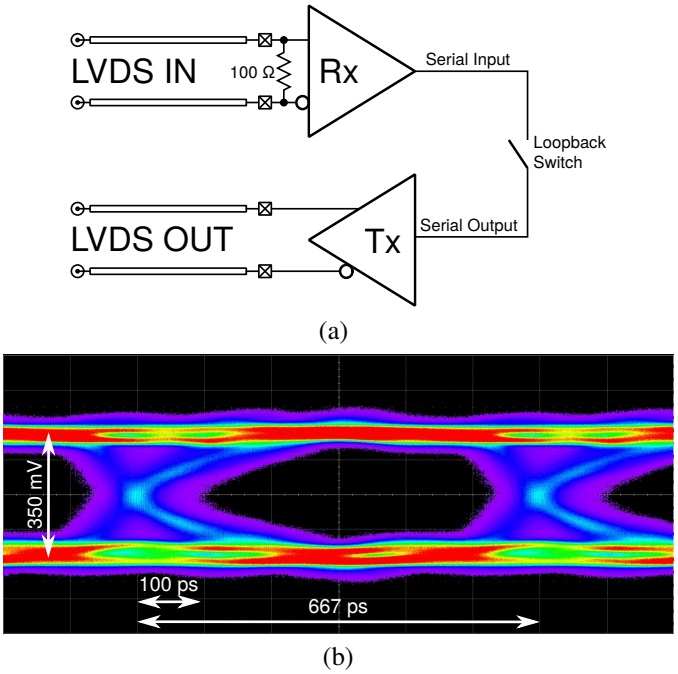

Fig. 6. (a) Schematic diagram of the LVDS loop-back test; (b) eye diagram with a pseudo-random binary sequence at 1.5 Gbit/s (amplitude = 350 mV, jitter = 100 ps)

A. Analog Front-End

Preliminary tests on the AFE demonstrate the functionality. The CSA exhibits good linearity of Time over Threshold (ToT) with respect to the input charge. The offset compensation in the discriminator has been verified, and exhibits an auto-zero voltage stability time comparable to the simulated one. Timing performance is now under evaluation; however, preliminary measurements on the prototype show a total jitter less than 90 ps for the minimum input charge of 2 fC [10].

B. Time-to-Digital Converter

Preliminary measurements on the TDCs demonstrate the functionality. Detailed measurements on timing performance are not yet available.

C. LVDS Blocks

The LVDS transmitter and receiver were characterized in loop-back configuration with four operational modes: Ultra-Low-Power (ULP), Low-Power (LP), TYPical (TYP) and High Performance (HP).

TABLE II
LVDS INTERFACE MEASURED CURRENT

Mode	Current
HP	8.1 mA
TYP	4.1 mA
LP	2.7 mA
ULP	1.6 mA

The Bit Error Ratio is less than 10^{-15} at 1.5 Gbit/s in LP mode.

Table II shows the RX + TX current consumption measured with pseudo-random data at 1.5 Gbit/s.

IV. CONCLUSION

A first prototype of a pixel read-out circuit has been designed and fabricated in 28 nm CMOS technology. Post-layout simulations show that a time resolution of 50 ps is feasible and compatible with a pixel area of 50 µm × 50 µm. Prototypes are fully functional, and measurements are in good agreement with simulations.

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