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A high resolution data conversion and digital processing for high energy physics calorimeter detectors readout

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Summary

The LHC accelerator complex aims to enhance its own performances with the purpose of increasing the potential for discoveries in the next years. The main objective of the HL-LHC upgrade is to enhance luminosity by a factor of 10 beyond the LHC design value in order to obtain an extensive dataset for new physics searches.

The HL-LHC should be operational from 2026 and the upgrade consists of a massive improvement of both the accelerator machine and the experiments. Its development will be a significant technological challenge both in terms of hardware and software.

The increase in peak luminosity will provoke unprecedented levels of event pile-up and all the experiments must plan to upgrade their detectors in order to perform a better event reconstruction, to improve the performances in an harsher radiation environment, and to overcome the aging effect.

This PhD activity is part of the CMS EB upgrade group effort. Indeed the custom LiTE-DTU ASIC developed at the INFN Torino belongs to the baseline choice for the upgraded VFE board. The enhanced board will allow to reduce the shaping time of the signal, mitigate the APD noise, improve the spike identification, and increase the signal information through an higher sampling rate.

The LiTE-DTU ASIC has been fabricated in a 65 nm CMOS technology and has a size of 2×2 mm^2. The ASIC embeds two 12-bit 160 MS/s ADCs, a PLL, and a digital architecture (DTU) dedicated to the online data selection, lossless compression and data serialization at 1.28 Gb/s. The LiTE-DTU ASIC is designed to be placed inside the experimental area, close to the detector. Therefore, considering the harsher radiation environment foreseen for Phase-2, several radiation-hard design techniques have been implemented in the design.

This thesis reports the design and characterization of the first prototype of the LiTE-DTU ASIC and it is organized as follows.

Chapter 1 briefly describes the LHC complex with a focus on the CMS experiment along with its own sub-systems. Moreover, an introduction of the HL-LHC upgrade and the scientific and technological goals are presented.

The legacy readout chain of the EB is introduced in Chapter 2, with particular emphasis on the on-detector electronics. Moreover, the technical reasons of the upgrade for the HL-LHC are presented along with the chosen strategy for the on-detector electronics upgrade. Then, an overview of the two new custom ASICs, CATIA and LiTE-DTU, are described likewise the hardware requirements for the upgraded electronics.

Chapter 3 is subdivided into several parts and provides an outline of the LiTE-DTU ASIC architecture and a detailed description of the building blocks included in the design of the first prototype. In the last part of the chapter, the implementation of the DTU is discussed along with the performed post-layout simulations and the latency study.

Chapter 4 is a report of the electrical characterization of the first prototype of the LiTE-DTU, showing the functionality of each block.

In Chapter 5 the TID and SEU qualification tests performed on the ASIC are reported along with the results.

Chapter 6 closes the thesis with a summary of the PhD activity along with the future development for the following chip submissions.

Acknowledgements

It would not have been possible to write this Ph.D. thesis without the encouragement of several fundamental people around me, to only some of whom it is possible to give a particular mention here.

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"All sorts of things can happen when you are open to new ideas and playing around with things."

- Stephanie Louise Kwolek

Contents

List of Tables

List of Figures

Chapter 1

Introduction

In this chapter the Large Hadron Collider complex is briefly described in order to explore the experimental framework where the LiTE-DTU ASIC will be installed. In particular, the CMS experiment along with its own sub-systems are depicted. The current chapter will end with an introduction to the HL-LHC upgrade, the scientific and technological goals and lastly the project for the upgrade of the CMS detector will be described.

1.1 The Large Hadron Collider

The Large Hadron Collider (LHC) is the largest, most complex and powerful particle accelerator in the world. It is located underground on the Franco-Swiss border nearby Geneva and it is managed by the European Council for Nuclear Research (CERN).

LHC consists of a circular structure, with a circumference of about 27 km, where accelerated beams of protons or lead ions collide with each other to study the basic constituents of matter, the interaction between particles and the fundamental forces. Along the LHC perimeter, there are four positions where beam particles are forced to collide in order to study their interactions. Four purpose-built detectors have been deployed in order to record, store and analyze the particle collisions outcome. As shown in Figure 1.1, the particle detectors are: the Compact Muon Solenoid (CMS), the Large Hadron Collider beauty (LHCb), A Toroidal LHC ApparatuS (ATLAS), and A Large Ion Collider Experiment (ALICE).

The beams acceleration process starts with the extraction of protons from a hydrogen tank, then protons are accelerated up to 50 MeV by Linac 2 which is a linear accelerator. The Proton synchrotron booster (BOOSTER) and Proton Synchrotron (PS) boost the energy of the particles along the way up to 1.4 GeV and 25 GeV respectively. After these acceleration steps, protons are sent to the Super Proton Synchrotron (SPS),

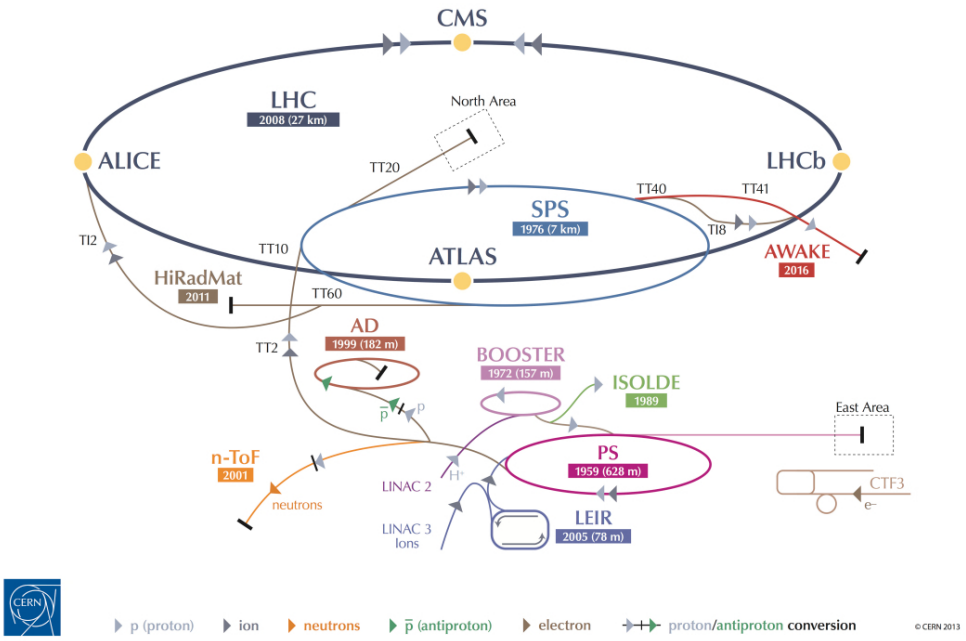


Figure 1.1: The accelerators complex at CERN [1].

where they reach 450 GeV and finally the beams are injected into the LHC.

Inside the LHC, two particle beams travel in opposite directions in separate beam pipes. The beam pipe is a tube kept at ultrahigh vacuum and the beam is held by a strong magnetic field maintained by superconducting electromagnets [2]. The beams are subdivided into bunches, which are about 10^{11} particles confined in few centimeters. The proton bunches can be accelerated up to 14 TeV. Moreover the bunches crossing frequency is 40 MHz therefore the collision period is 25 ns. The next chapters will describe how the short time between the bunch crossings has a dominant implication for the readout electronics design and the trigger system planning.

The majority of protons do not collide and simply continue unaltered their trajectory at every crossing. On the other hand, a single bunch crossing may produce one or more events, when several separate events occur the number of collisions per bunch crossing defines the event pile-up. One of the main particle accelerator parameter is the luminosity. Instantaneous luminosity in particle physics refers to the ratio of the number of events detected N in a certain time t to the interaction cross-section σ: $L = \frac{1}{\sigma}\frac{dN}{dt}$. It has the dimensions of events per time per area and it is expressed in units of $\mathrm{cm}^{-2} \cdot \mathrm{s}^{-1}$. The integrated luminosity is given by the integral of L in time: $L_{\mathrm{int}} = \int L\, dt$, it has units of inverse area and it is usually measured in inverse barns: $1\ \mathrm{b} = 10^{-28}\ \mathrm{m}^2$.

In Figure 1.2 the scientific program of LHC is shown, it covers few decades alternating period of measurements and long technical stop, known as Long Shutdown (LS), to prepare the LHC machine for higher energy and luminosity runs [3]. The design of the

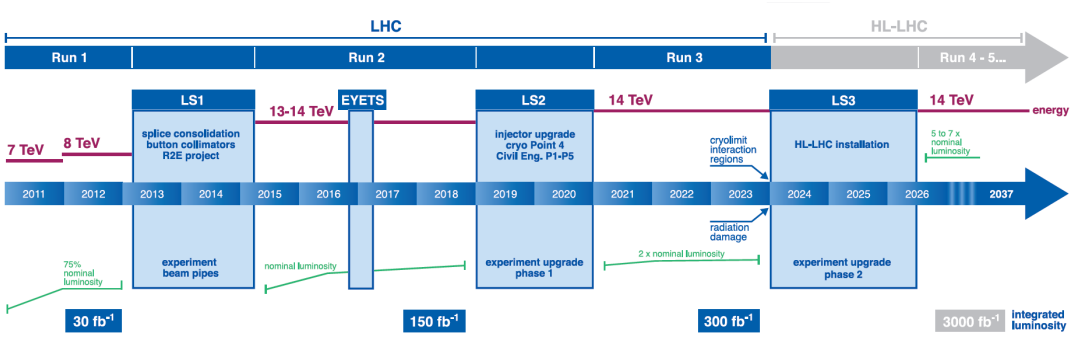


Figure 1.2: Timeline of the LHC and HL-LHC run and shutdown periods at CERN, including for each phases the energy and luminosity targets.

LHC aims to reach a center of mass energy of 14 TeV and an instantaneous luminosity (L) of 10^{34} cm^{-2} s^{-1} for proton-proton (p-p) collisions [4]. Nowadays, LHC has completed Run 2 and the experiment upgrade phase 1 is going to take place during LS2.

Up to now the delivered integrated luminosity has reached 150 fb^{-1}, in run 3 the goal is 300 fb^{-1} while during the High Luminosity LHC (HL-LHC) the integrated luminosity will reach 3000 fb^{-1}, as shown in Figure 1.2. The delivered integrated luminosity for 2010-2012 and 2015-2018 can be seen in Figure 1.3.

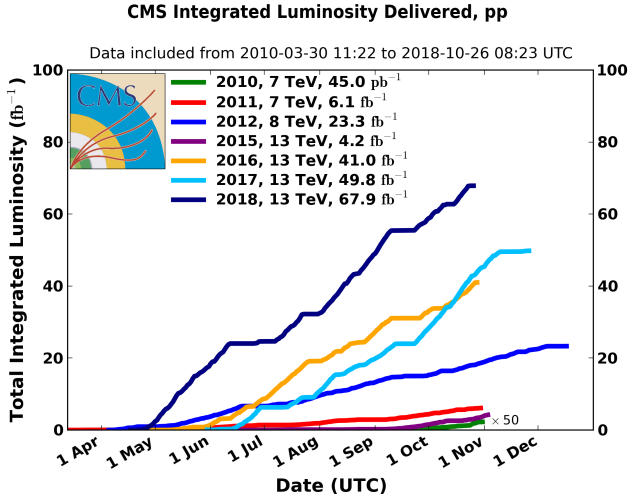


Figure 1.3: Delivered luminosity versus time for 2010-2012 and 2015-2018, data referred to p-p collisions only.

1.2 The Compact Muon Solenoid

CMS is a general purpose detector, its main goal is the study of matter interaction at energy scale of TeV, and to discover and characterize the Higgs Boson. The CMS detector is composed by several subsystems and its layout [5] is shown in Figure 1.4.

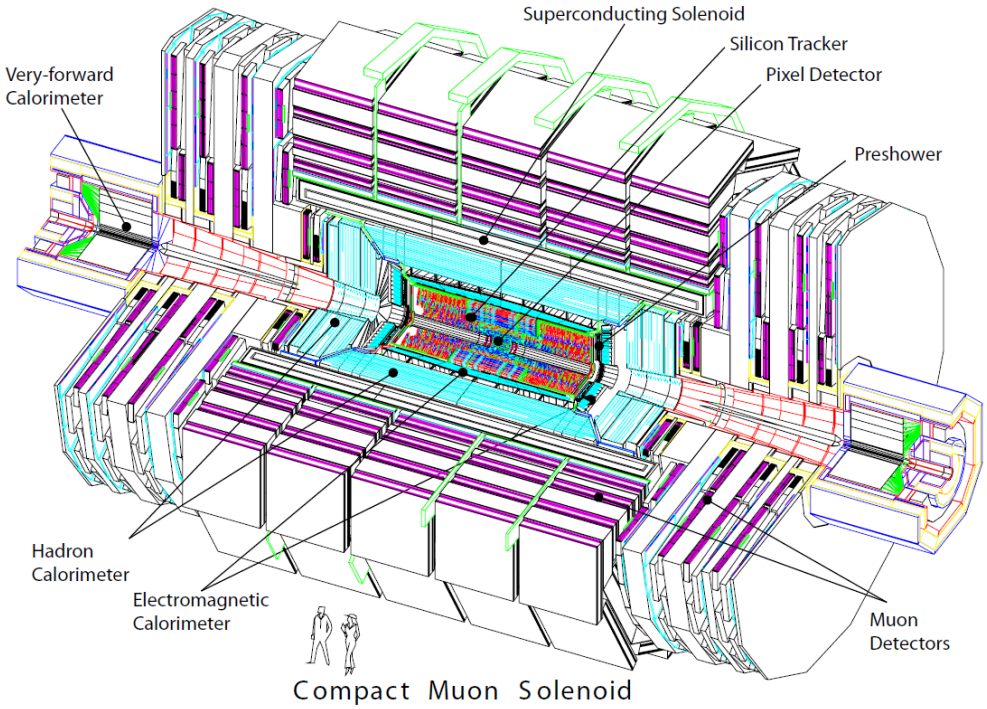


Figure 1.4: Sketch of the CMS detector [6]. The central part is called *barrel* while the two forward regions are the *endcaps*.

The five different layers are: the tracker, the electromagnetic calorimeter, the hadronic calorimeter, the magnet and the muon chambers. The detector has a cylindrical geometry, it is 15 m high and 22 m long and all the subsystems are symmetrically centered around the interaction point. It is designed to detect muons with high accuracy and for this purpose the superconducting solenoid magnet produces a magnetic field of 3.8 T. The tracker and the calorimeter system are enclosed inside the solenoid while the muon chambers are installed on the outside. A transverse slice of the CMS detector can be seen in Figure 1.5.

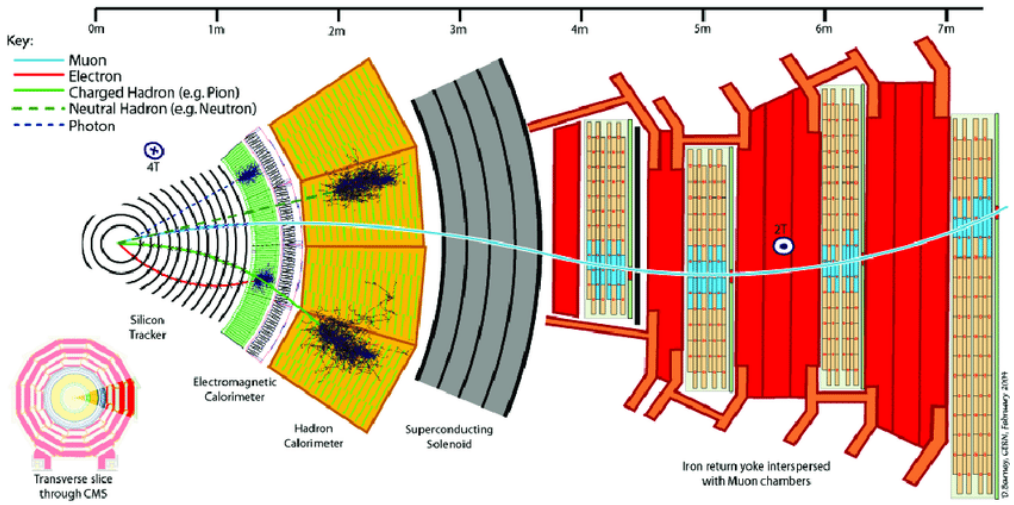


Figure 1.5: Sketch of a transverse slice of the CMS detector. From this representation is possible to follow a different particle path from the collision vertex up to the furthest interaction with the detector.

1.2.1 The tracking system

The inner tracking system surrounds the interaction point and it is designed to provide accurate[1] identification of charged particles trajectories along with efficient reconstruction of secondary vertices.

As mentioned before, the LHC aim in terms of instantaneous luminosity is about 10^{34} cm^{-2} s^{-1} for p-p collisions, therefore in this conditions there is an average of about 1000 particles from more than 20 overlapping p-p interactions traversing the tracker every 25 ns [6]. Consequently, the tracker has to provide a high spatial resolution, high granularity, and a fast signal readout for a good reconstruction of the events. Another technical challenge is the harsh radiation environment. The CMS tracker is the largest silicon tracker ever built [7], with about 200 m^2 of active silicon area. It consists of a core part made by pixels and an outer part composed by microstrips that surrounds it. The tracker is entirely based on silicon detectors which have been historically used as radiation detector [8].

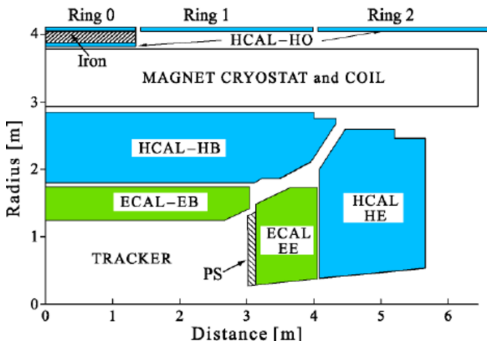
The pixel detector contains 65 million pixels placed in three cylindrical layers at 4 cm, 7 cm and 11 cm from the beam pipe and disks at each end [9]. The silicon microstrip detector is composed by 10 layers with a total of 10 million of detector strips

[1]The requirements on high accuracy for track reconstruction derives from the interest and importance of b-jet events, which are events that contain several particles arising from the hadronization process of a b-quark.

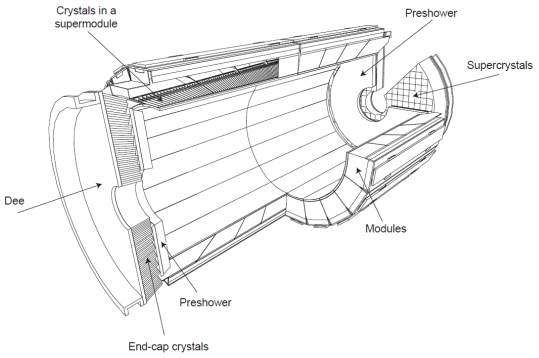
[10]. Because of the high number of sensors and readout channels, the power must be maintained as low as possible in order to relax the requirements for the cooling system. The reconstruction of the particle track is obtained by appropriate combination of bi-dimensional information of particle hits on the different layers.

1.2.2 The calorimeter system

In CMS there are two different calorimeters: the Electromagnetic Calorimeter (ECAL) and the Hadron Calorimeter (HCAL). The purpose of the former is the energy measurement of photons and electrons while the latter is dedicated to perform the energy measurement of charged and neutral hadrons [11]. Figure 1.6a shows a slice-longitudinal fraction of the ECAL detector (green), HCAL detector (lightblue), and the spatial arrangement within CMS.



(a)



(b)

Figure 1.6: The sketch of quarter slice-longitudinal cross section of the calorimeter system of CMS (left) and layout of the CMS electromagnetic calorimeter [12] (right).

The Electromagnetic Calorimeter

ECAL is an homogeneous and hermetic calorimeter, composed of 75848 scintillating lead tungstate ($PbWO_4$) crystals and it is divided in two main sections: the central part of the detector is called ECAL Barrel (EB) and it is closed by two ECAL Endcaps (EEs). A preshower system (PS) is installed in front of the endcap ECAL for π^0 rejection. The PS is made of two layers of silicon strips alternated with passive layers of lead radiators. The EB is placed at radial distance of 1.3 m from the interaction point while the EEs are located at 3.10 m from the center of the detector as shown in Figure 1.6a.

The maximum emission of $PbWO_4$ scintillation light is around 420 – 430 nm and the 80% of the signal is emitted in about 25 ns. This peculiarity is extremely functional

because is of the same order of magnitude as the LHC bunch crossing time. Moreover, the $PbWO_4$ crystals have several characteristics which allow to develop a fast, compact, high granularity, and radiation resistant detector. These characteristics are: short radiation length (0.89 cm), high density (8.28 g/cm^3), and small Molière radius (2.2 cm).

The scintillator bars have an exposed face of 22 × 22 mm^2 and in order to collect the scintillating light from the crystals two different photodetectors are used: Avalanche PhotoDiodes (APDs) for barrel crystals and Vacuum PhotoTriodes (VPTs) for endcap crystals. In EB each crystal has on the rear face a couple of APDs; the APD active area is 5 × 5 mm^2 and the operational gain is 50. The two analog signals are summed and form a single channel. The APDs have been developed from Hamamatsu on purpose for ECAL [13] [14]. In the endcaps, each crystal is coupled to one VPT with an active area of approximately 280 mm^2. The VPT are photomultipliers having a single gain stage, also these devices have been developed for CMS ECAL [15] [16]. The VPT anode is made by a thin copper mesh in order to operate the photomultiplier in the 4-T magnetic field.

More details on the ECAL detector, e.g. electronics readout, are further discussed in the next chapters since ECAL barrel is the environment where the LiTE-DTU ASIC will be installed.

ECAL energy resolution

The energy resolution of ECAL is parametrized as in Equation 1.1, where S is the stochastic contribution, N the noise term, and C the constant term.

$$\left(\frac{\sigma}{E}\right)^2 = \left(\frac{S}{\sqrt{E}}\right)^2 + \left(\frac{N}{E}\right)^2 + C^2 \tag{1.1}$$

S contains contributions from the shower containment, the number of photoelectrons and the variations in the gain process. The noise term includes three contributions: electronics noise, digitization noise, and pileup noise. C depends on light collection heterogeneity, energy leakage, and uniformity and stability of the channel response.

One of the driving criteria during ECAL design was the ability to precisely determine energy and position of photons, in order to obtain a excellent mass resolution. For Higgs physics, a key part was enhance the detector sensitivity to the photon identification because the two-photon decay process, $H \longrightarrow \gamma\gamma$ is one of the most sensitive channels in the search for low-mass Higgs boson ($m_H < 150$ GeV). The ECAL resolution reached during 2010 - 2011 [17] for photons from the Higgs boson decay was one of the fundamental contributor to the discovery of the Higgs boson [18] [19].

The Hadron calorimeter

The HCAL is placed between ECAL and the magnet coil, as shown in Figure 1.6a. This calorimeter is composed by scintillating tiles and brass absorbers. The signals are readout via optical fibres embedded in the tiles and coupled to hybrid photodiodes. HCAL is primarily used to perform the energy measurement of hadrons jets and exotic particles. Behind the magnet, in the barrel region, there is another hadron calorimeter, *tail-catcher* (HCAL-HO), which allows to capture very high energetic hadrons showers not stopped within the ECAL, HCAL, and the magnet. This additional calorimeter helps the discrimination between hadronic jets and muons.

1.2.3 The muon system

The robust and precise detection of muons has always been a fundamental priority to CMS. The muon system has three features: muon identification, momentum measurement, and triggering. In order to have a a fast response to generate a muon trigger and a precise momentum determination, the CMS muon system employes 3 different gaseous particle detectors: Resistive-plate-chambers (RPC), Drift-tube (DT), and Catode-strip-chambers (CSC) [20]. The former is used to notify the presence of high energy muons at trigger level [21], the latter measures the momentum both in the barrel region (DT) and in the endcaps (CSC) [22]. The RPC and DT are alternated in concentric rings in the barrel region while in the endcaps discs of CSC are alternated to RPC detectors.

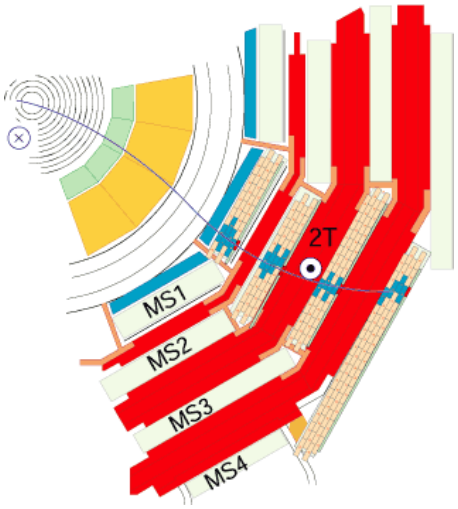


Figure 1.7: A muon, in the plane perpendicular to the LHC beams, leaves a curved trajectory in four layers of muon detectors.

1.2.4 The trigger and data acquisition systems

The CMS Trigger is composed by a two-level trigger system in order to perform the selection of events with an interesting signature, reducing the rate of the non-interesting processes.

The first stage is the Level-1 (L1) trigger [23]; it is implemented in the readout electronics, ASICs and FPGAs, and analyzes the information from the calorimeter and the muon detectors. The L1 accept signal relies on the reception of trigger primitive events, for instance electrons, photons, muons, and jets. The Level-1 trigger reduces the event rate from 40 MHz, which is the crossing frequency of LHC, down to 100 kHz. The architecture of the L1 trigger system is shown schematically in Figure 1.8.

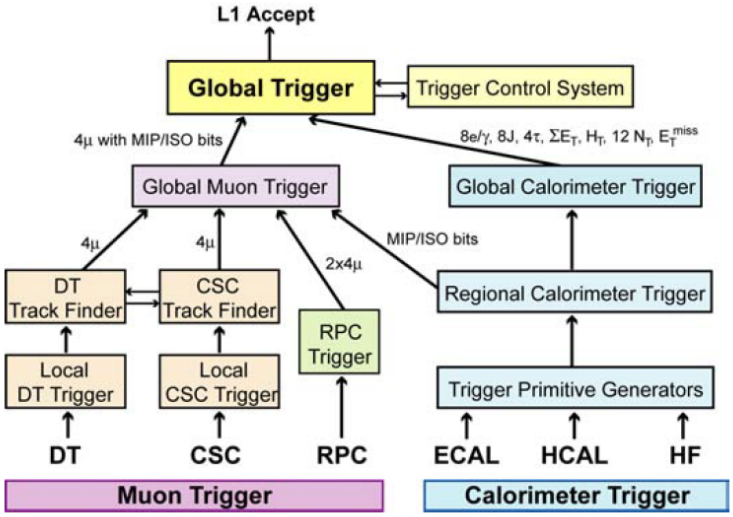


Figure 1.8: A muon, in the plane perpendicular to the LHC beams, leaves a curved trajectory in four layers of muon detectors.

After the L1 trigger selection, the size of produced data is around 100 Gb/s coming from about 650 data sources. The Data Acquisition System (DAQ) system provides the needed amount of computing power for the second trigger stage: the High-Level Trigger (HLT) [24]. HLT is implemented in software on a farm of commercial processors and it reduces the data rate to about 1 kHz. If required HLT can perform a simplified version of the off-line reconstruction analysis in order to perform physics selections. Lastly, the events that pass the HLT are stored and can be analyzed on a grid of computers distributed in a worldwide computing infrastructure.

1.3 High-Luminosity LHC

The LHC accelerator complex aims to enhance its own performances with the purpose of increasing the potential for discoveries in the next years. Therefore the successive step after the Run 3 will be the upgrade of LHC: HL-LHC as shown in the LHC timeline in Figure 1.2.

The main objective of the upgrade is to increase luminosity by a factor of 10 beyond the LHC design value in order to obtain an extensive dataset (3000 fb^{-1}) for new physics searches. For example, during the HL-LHC phase the number of Higgs events per year will increase with a factor of 5 compared to the dataset obtained in 2017.

The HL-LHC should be operational from 2026 and its developments will be conditioned by several technological challenges and innovations.

The design of the LHC upgrade [25] consists of a massive improvement of both the accelerator machine and the experiments. The increase in peak luminosity will result in an higher number of collisions occurring within the same bunch crossing. In LHC the average number of collisions is about 40-60 while during HL-LHC it will increase up to 140-200 [26]. Therefore unprecedented levels of event pile-up will be reached and all the experiments must plan to upgrade their detectors in order to perform a better event reconstruction, to improve the performances in an harsher radiation environment, and to overcome the aging effect [27].

1.3.1 HL-LHC upgrade of CMS

Several upgrades have been foreseen for the CMS experiment which will involve all the sub-systems both on-detector and off-detector devices.

Upgrade of the tracking system

The complete tracker system will be superseded with a new detector with the goal of achieve a solid radiation hardness and to manage increased data rate. Indeed, the Inner Tracker will be exposed to radiation levels up to $2.3 \times 10^{16}\ n_{eq}\,/\,cm^2$ and an accumulated ionizing dose of 12 MGy [28]. New solutions and advanced technologies will be undoubtedly needed for this major upgrade of CMS, in particular from the point of view of readout and powering electronics. The new detector will preserve the same structure and the concept but performing higher granularity. Moreover it will send information to the L1 trigger system thereby improving the even selection mechanism [29].

Upgrade of the calorimeter system

Both the endcaps of ECAL and HCAL calorimeters will be replaced for the HL-LHC phase due to the increase of radiation damage (more than $1.5 \times 10^{15}\,n_{eq}/cm^2$ close to the beam line) [30] [31]. Indeed, the radiations will undermine the ECAL crystals and HCAL photo-detectors and tiles response. The High Granularity Calorimeter (HGCAL) will take the place of the two endcaps. HGCAL is a calorimeter composed of hexagonal silicon sensors with two types of absorbers: tungsten in the ECAL section and lead in the HCAL part [32].

The CMS EB will undergo in an upgrade to preserve its latest performance in the demanding HL-LHC conditions. The crystals and APDs will be unmodified, while both the on-detector and off-detector electronics will be replaced by an upgraded version in order to manage higher trigger latency and to mitigate the higher pile-up [33]. Detailed description of the ECAL barrel electronics upgrade is reported in Chapter 2. Further, the operating temperature will be decreased to mitigate the APD noise [34].

Moreover the calorimeter system is going to be optimized to reach the time resolution of 30 ps for electrons and photons with E > GeV.

Upgrade of the muon system

Regarding the muon system, new detectors will be included to improve the robustness and the performance in the critical forward region. A large-area triple-foil Gas Electron Multiplier (GEM) is going to be added during LS2 while the second GEM and two new generation RPCs will be installed in the forward region during LS3. [35]

Upgrade of the trigger anch data acquisition system

L1 trigger upgrade will exploit FPGAs in a new electronics system, taking advantage of the high-bandwidth optical transmission and more complex algorithms for data rate reduction. The upgraded trigger rate will increase from 100 kHz of LHC to 750 kHz of HL-LHC.

Chapter 2

The ECAL barrel upgrade for the HL-LHC phase

The CMS EB will undergo a crucial upgrade in order to match the operation environment of HL-LHC and thereby fully taking advantage of the larger dataset delivered by LHC.

In this chapter the legacy electronics of the EB is briefly introduced, with particular emphasis on the on-detector electronics. The technical an physical reasons of the EB upgrade for the HL-LHC are presented along with the developed strategy for the EB on-detector upgrade. Finally, the CAlorimeter Trans-Impedance Amplifier (CATIA) ASIC and Lisbon-Turin Electronics Data Transmission Unit (LiTE-DTU) ASIC are described with the hardware requirements for the upgraded electronics.

2.1 The current ECAL barrel system

The first elements of the EB readout system are the $PbWO_4$ crystals, which convert the deposited energy by particles into scintillation light. The produced light is collected and converted into a photocurrent by 2 APDs per crystal, the two signals are summed and form a single channel.

The EB readout chain is composed by two subsystems: the on-detector electronics, which is located directly behind the crystals and is exposed to the radiation environment, and the off-detector electronics, which is placed in the underground counting room close to the experimental area [12]. The communication between the two systems is managed through 90-meter long high-speed optical links, working at 800 Mb/s. A representation of the full legacy readout chain of the EB is shown in Figure 2.1.

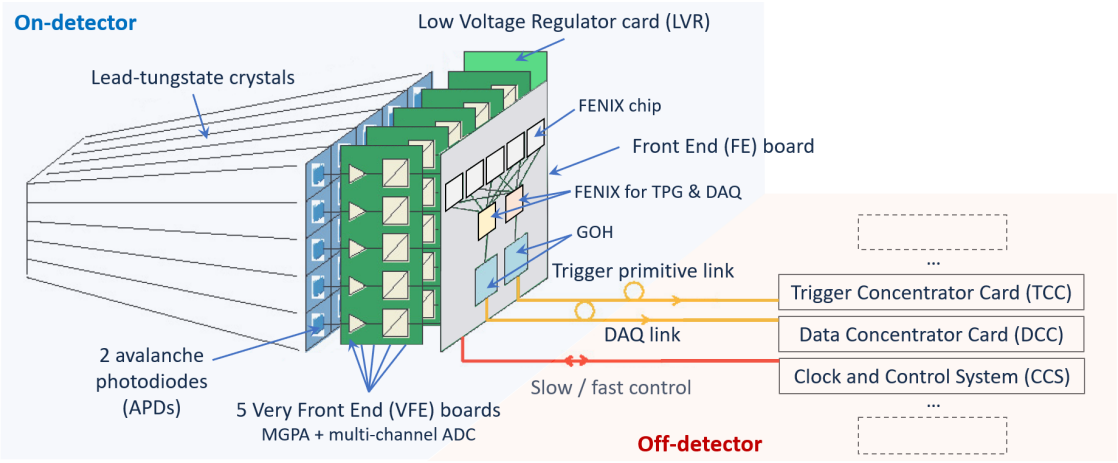


Figure 2.1: Schematic view of the on-detector and off-detector electronics of the EB. The scintillation light is collected by 2 APDs per crystal, then the APD signals are acquired and processed by the on-detector electronics. After that, the data and the trigger primitives are sent from the FE boards to the off-detector electronics through high-speed optical links.

2.1.1 The on-detector electronics

The on-detector electronics installed in the EB has been designed to manage the readout of a Trigger Tower (TT), which represents the basic detector unit. It consists is a structure of 5×5 crystals and the system includes five Very Front-End (VFE) boards, one Front-End (FE) board, two Gigabit Optical Hybrids (GOH), one Low Voltage Regulator (LVR) card and a motherboard [11].

The Very Front-End board

In EB each crystal is coupled to a pair of APDs and a single channel is obtained by the sum of the two APD signals. Then each VFE card manages the readout of five channels. In the readout channel of the VFE boards, the signal is pre-amplified, shaped, amplified by three amplifiers with different nominal gains, and lastly they are digitized and selected. These functionalities are built into the Multi-Gain Pre-Amplifier (MGPA) chip [36] and the multi-channel ADC chip [37], [38]. Both ASICs have been fabricated in a 3-metal layer 0.25 μm CMOS technology. The VFE board along with the two ASICs are represented in Figure 2.2.

The MGPA is based on a Charge Sensitive Amplifier (CSA). The chip provides three analog output signals amplified with three different gain values: x1, x6, and x12, respectively. The employed architecture in the MGPA chip is shown in Figure 2.3.

The pulse shaping is performed by a CR-RC network and the obtained shaping time

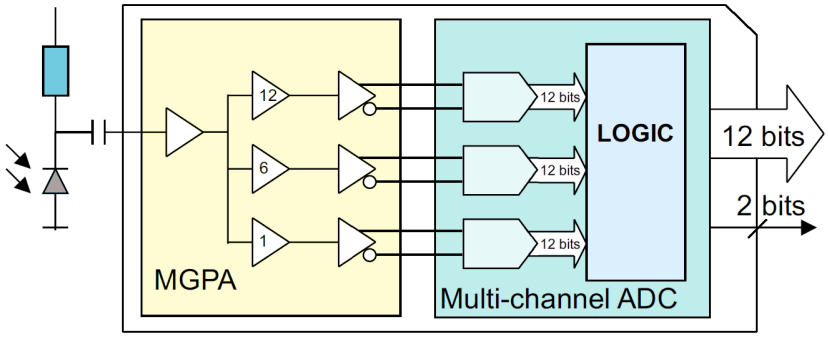


Figure 2.2: Scheme of the VFE board [36], [37].

is about 40 ns, thus the overall pulse peaking time is 50 ns because it includes also the scintillation decay time (10 ns) [36]. The first stage of the MGPA is a CSA with external feedback, then it is buffered by source followers to the three gain channels. The resistors R_{G1}, R_{G2} and R_{G3} set the gains and feed common gate stages which provide current to match the inputs of three differential output stages.

The MGPA can perform a baseline tuning to the ADC inputs through the use of 3 programmable 8-bit DACs. Moreover, an internal test-pulse generator allows to scan the full dynamic range for the validation of the MGPA behavior [36].

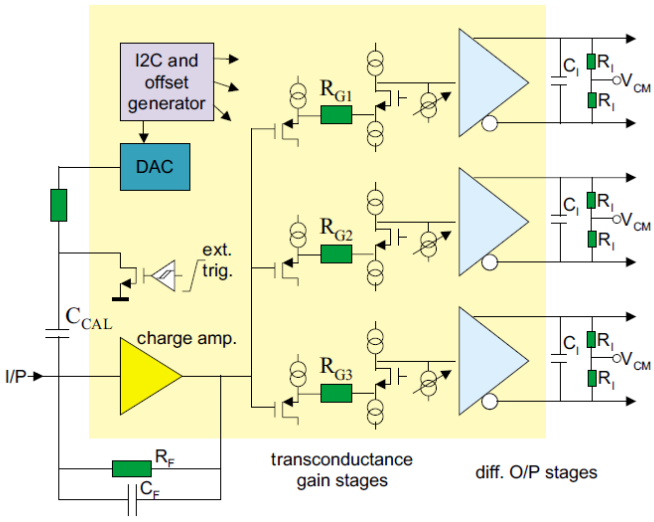


Figure 2.3: Schematic view of the MGPA: the first stage on the left is a CSA with external feedback, it is buffered by source followers to the three parallel gain channels. The gain values are determined by R_{G1}, R_{G2}, and R_{G3}, these resistors are connected to the common gate stages which arrange the currents to match the inputs of the three differential output stages [36].

The multi-channel ADC receives the three MGPA output signals and employs three 12-bit, 40 MS/s ADCs, for the analog to digital conversion. The output of the VFE bard is obtained by the selection unit, which selects the unsaturated sample from the highest gain output possible.

The multi-channel ADC chip has been designed in order to avoid the necessity of a single ADC with a wide dynamic range (15-16 bits) and high resolution (> 10bits). Indeed, the ADC embedded in the multi-channel chip is the *AD41240*: a 12-bit, quad-channel pipelined ADC, it runs at 40 MHz and the ADC design has been developed by *ChipIdea Microelectronica S.A.* (Lisbon, Portugal) [37], [38].

The complete multi-channel ADC chip occupies an area of 4×4 mm^2. The whole dynamic range of the signal has been divided into three gain ranges and a logic unit has been implemented for the selection of samples. The logic selects the highest non-saturated 12-bit sample along with two bit to identify the ADC and the corresponding gain. The saturation occurs by definition when the digital value has the 8 MSBs all equal to one. When the logic unit switches to a lower gain the system does not return immediately to the higher gain but it is forced to readout the next five samples at the lower gain [38]. This selection mechanism allows a full digitization of a pulse to be transmitted in a single gain channel. After 5 clock cycles the multi-channel ADC chip restarts the gain channel selection taking the highest non-saturated sample.

The low voltage regulators and the motherboard

The LVR card employs 11 radiation-hard low voltage regulators, the 2.5 V output voltages are delivered to the VFEs through the motherboard and to the FE card [39].

The motherboard distributes and filters the APDs bias voltage and it connects the 25 APDs of a TT to the temperature sensors. Moreover, it supplies one LVR and five VFE cards [12].

The Front-End board

FE card processes at 40 MHz the data received from five VFE cards in the TT. At the FE level there is the first step of both trigger and data acquisition. Indeed, in the FE board the Trigger Primitive Generation (TPG) is performed and the information about the deposited energy in a TT is stored awaiting the Level-1 trigger decision. The need to store data in the FE board is due to the latency required by the Level-1 trigger decision procedure (3.2 μs maximum) [11]. When the Level-1 accept signal is received by the FE board the stored data are sent to the off-detector system.

Each FE board in EB is connected to three optical links: the first fiber is dedicated

to the data transmission, the second fiber is for sending the trigger primitives, and the last link is used to transmits the clock, control signals and Level-1 signals [40].

The energy information storage and the TPG are realized in the FE board by 6 FENIX ASICs [41]. Five FENIX chips embeds a 256-word deep dual-port memory (called pipeline) [42]. Each of them readouts the output of a VFE and manages the computation of the total Transverse Energy (E_T) measured in a strip of 5 crystals. The sixth FENIX ASIC receives the five results and derives the sum of the overall (E_T) of the TT. The last FENIX chip generates the trigger primitives (14-bit words) and transmits them to the Trigger Concentrator Card (TCC) in the off-detector system through one GOH [43]. The pipelined data are transmitted on another GOH to the Data Concentrator Card (DCC) only when the Level-1 accept signal is received by the FE board [44].

Gigabit Optical Hybrids

The GOH is the optical link system used for the ECAL serial digital data link. The GOH is used in order to transmits TPG and data from the on-detector electronics to the off-detector system. the GOH system includes the Gigabit Optical Link (GOL), a data serializer and laser driver chip, a laser diode, optical fibers, fibers interconnections, and the receiver [12]. The fibers operate in single mode with a wavelength of 1310 nm and at 800 Mb/s.

2.1.2 The off-detector electronics

The ECAL off-detector system is placed in the counting room close to the experimental area. This system is the interface between the on-detector electronics and the global Data Acquisition System (DAQ). It participates in both detector readout and trigger system and it runs at 40 MHz. The off-detector system has to manage data sent from the FE board, deserialize and control the integrity of the information, assemble the event and transmit it to the DAQ. Moreover in the off-detector system the trigger primitives are collected and then are sent to the regional trigger while the system ensure a correct time alignment between channels. All these functions have to be accomplished in a period of 10 clock cycles [45].

The off-detector electronics consist of several boards: Clock and Control System (CCS), Trigger Concentrator Card (TCC), Data Concentrator Card (DCC), Synchronization and Link Board (SLB), and Selective Readout Processor (SRP) [11]. A representation of the ECAL off-detector system architecture is shown in Figure 2.4.

The CCS board controls the digital optical link system running at 40 MHz which is provided to the on-detector electronics. The CCS manages both fast and slow control functions. The former involve the distribution of the information and the 40 MHz clock

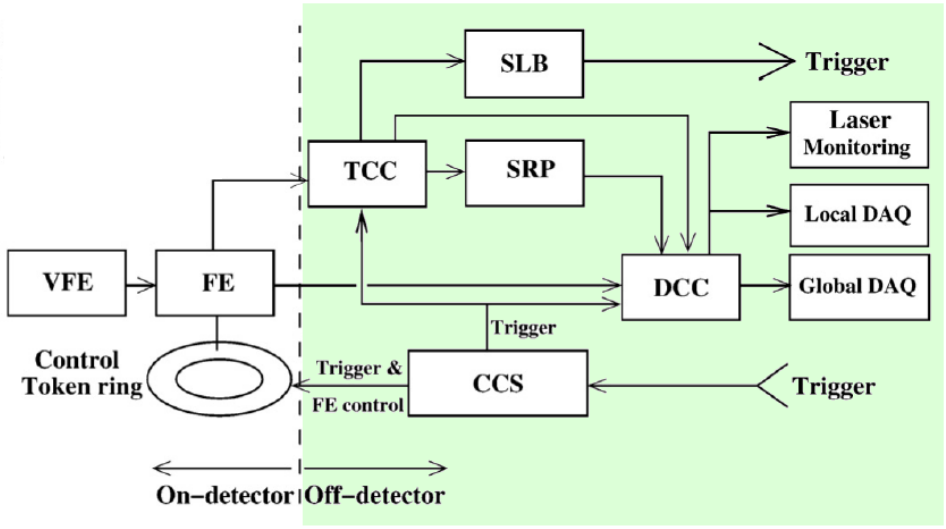


Figure 2.4: In the green area is represented a scheme of the off-detector electronics system of the ECAL detector [12].

while the latter transmit VFE and FE initialization configurations and receives the on-detector status (voltages, APD leakage currents, and temperatures) [45].

The TCC receives the trigger primitives and delivers the information to the calorimeter trigger processor. The transmission is performed at each bunch crossing through the SLB board, a mezzanine card placed on the TCC.

The TCC system evaluates the trigger primitive content and classifies the TT importance in order to obtain information and forward them to the SRP at each Level-1 trigger accept. The SRP synthesizes the information from adjacent TT and transmits the entire readout map to the DCC.

For positive Level-1 decisions, the DCC receives data from the Front-End (FE) system, it performs a data reduction by applying the readout map computed by the SRP and DCC provides the data to the central DAQ [12].

2.2 Upgrade: technical and physical reasons

The main requirement of the EB upgrade is to preserve the physics performance of the Run 1 during the HL-LHC conditions: higher luminosity and pileup level. In order to achieve this requirement, the EB electronics have to be adapted and refurbished for the new Level-1 trigger requirements on latency and rate, grant more precise timing resolution, and boost the APD noise mitigation [46].

Trigger requirements

In the current system, the trigger latency is 4 μs and the Level-1 trigger rate is 100 kHz. The principal technical reason for the EB is the increment of both the trigger latency and the L1 trigger rate, in particular the former will reach a maximum of 12.5 μs while the latter will rise to 750 kHz. The EB on-detector and off-detector readout electronics are going to be renewed to match these trigger requirements and to add tracking information. In the current system the generated trigger primitives have a granularity of 5×5 crystals, whereas in the upgraded system it will be possible to provide single crystal information. As a result, with the granularity improvement of the L1 calorimeter trigger, the electromagnetic showers will be matched more precisely to their tracks.

Precise timing resolution

Traditionally precision time measurements have not been a key aspect of the calorimeters at the hadron colliders. Nevertheless, the position determination of the primary vertex can be improved and it can enhance the detector performance at higher pile-up values.

The goal for the EB upgrade is to obtain a precision of 30 ps on the arrival time of photons produced by Higgs bosons decays. To achieve this level of precision the VFE electronics have to provide signal oversampling, leading to an increase in readout bandwidth as a result.

APD noise mitigation

An improved noise filtering will be performed by the use of a shorter pulse shaping. This will allow a better suppression in Level-1 trigger of anomalous signals [47]. These anomalous signals, termed *spikes*, are isolated large signals observed in the EB. Their energies may exceed the hundreds of GeV and the *spikes* rate is proportional to the collision rate of the proton beams. Therefore, during the HL-LHC they will increase the complexity of the trigger and must be excluded from physics analyses.

Spikes are identified as particles hitting directly the APDs and sporadically interacting to generate secondaries that induce large anomalous signals through direct ionization of the silicon [47]. A reduction of the shaping time of the signal enables to obtain a clearer differentiation between the scintillation signals and the spikes. Moreover the APD leakage current contributes to the noise and it is proportional to the square root of the shaping time.

2.3 EB upgrade strategy: the new readout electronics

2.3.1 Proposed new on-detector electronics

The architecture of the EB on-detector electronics upgrade will preserve the arrangement and form factor of the legacy system.

The $PbWO_4$ crystals, the APDs and the motherboards will be retained during the HL-LHC phase. Indeed, from the longevity test performed, both accelerated aging and irradiation tests, show that for the scintillating crystals the main concern is on the reduction of the light transmission due to the hadron irradiation [48]. However Geant4 simulations and test beam have confirmed that the influence of the light loss on the energy resolution in the barrel region will be negligible [49]. On the other hand, as the integrated luminosity increases, the dark current of the APDs increases. In Figure 2.5 the expected evolution of the APD dark current at $|\eta| = 0$ and $|\eta| = 1.45$ for three different operational temperature are depicted. After an integrated luminosity of 3000 fb^{-1} the predicted dark current at pseudorapidity [2] $|\eta| < 1.45$ is about 200 mA [49]. This implies that the electronic noise will increase by a factor of 10 thus in order to mitigate it, the operational temperature of the on-detector EB system will be decreased from the current 18 °C to 9 °C [50]. Another studied scenario consists in reducing the temperature from 18 °C to 9 °C until the LS4, and from 9 °C to 6 °C afterwards.

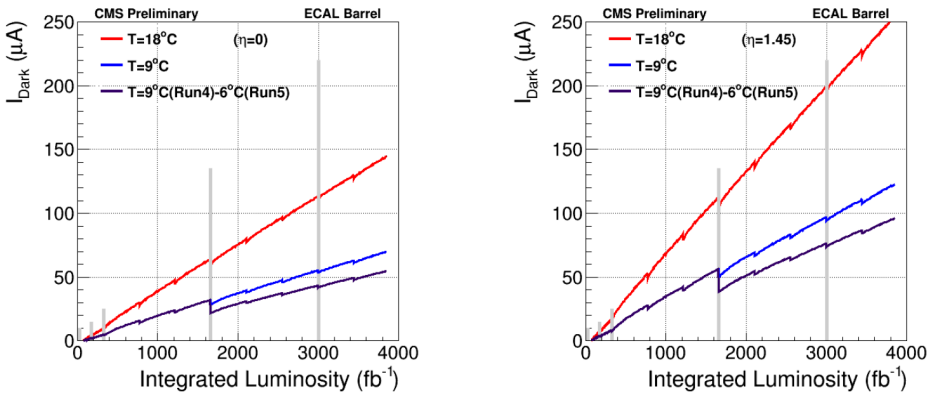


Figure 2.5: The expected APD dark current for three operational temperature: 18 °C (red curve), 9 °C (blue curve) and the switch from 9 °C to 6 °C after the LS4 (purple curve). The vertical lines indicates the LSs and the pseudorapidity values are $|\eta| = 0$ (left) and $|\eta| = 1.45$ (right) [50].

[2] Pseudorapidity is a spatial coordinate describing the angle of a particle relative to the beam axis and it is defined as: η = - ln $(\tan\frac{\alpha}{2})$ where $\alpha = 90°$ is the direction perpendicular to the beam axis and $\alpha = 0°$ is the beam axis. The CMS EB covers the pseudorapidity range of $|\eta| < 1.479$ [12].

2.3.2 The upgraded VFE board

The baseline choice of the CMS EB upgrade group is to substitute the present VFE and FE cards with new and enhanced boards, along with low-voltage distribution system and optical links. The VFE will integrate two new custom chips: CATIA and LiTE-DTU ASICs, mainly in order to reduce the shaping time of the signal, mitigate the APD noise, improve the spike identification, and increase the signal information improving the sampling rate. The architecture of the upgraded VFE board is shown in Figure 2.6.

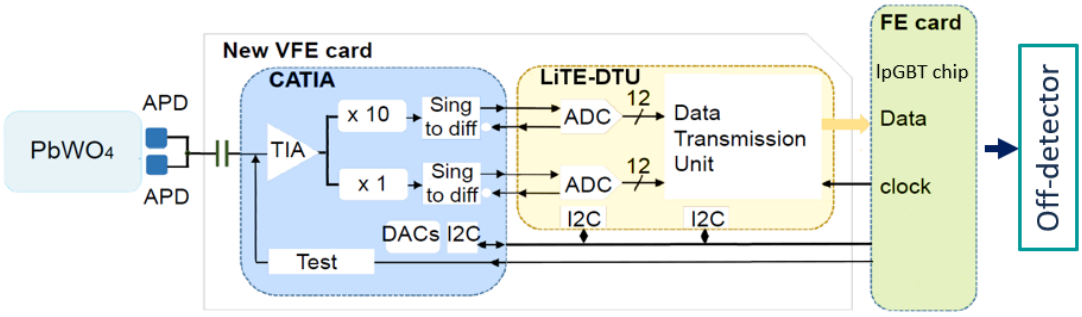


Figure 2.6: Scheme of the new VFE board for the upgrade.

CATIA ASIC

The first chip of the upgraded VFE is the CATIA ASIC. CATIA is a fully analogue chip implemented in 130 nm technology, the scheme of the ASIC is represented in Figure 2.7 [51].

It is a dual gain Trans-Impedance Amplifier (TIA), since in the upgraded VFE board the legacy CSA amplifier has been replaced by a TIA in order to retain the pulse shape of the scintillating crystal coupled to the APD. The TIA amplifies and converts the input photocurrent signal coming from the APD into a voltage signal. The output dynamic range, in equivalent energy of electrons and photons, is between 50 MeV and and 2 TeV. The lower bound indicates the intrinsic noise of the APDs. The full dynamic range is covered by two subranges implemented through two differential amplifiers with gain x10 and gain x1, thus the upper limit of each channel is 200 Gev and 2 Tev, respectively. The first version of the CATIA ASIC has been submitted in 2016, it was a demonstrator and its main purpose was the range optimization of the TIA [51]. The validator version (CATIA_v1) has been submitted in 2018, it has been connected to a 12-bit 160 MS/s commercial ADC and characterized with the laser light and an electron beam during a test campaign at CERN [52]. The test on CATIA_v1 has been carried

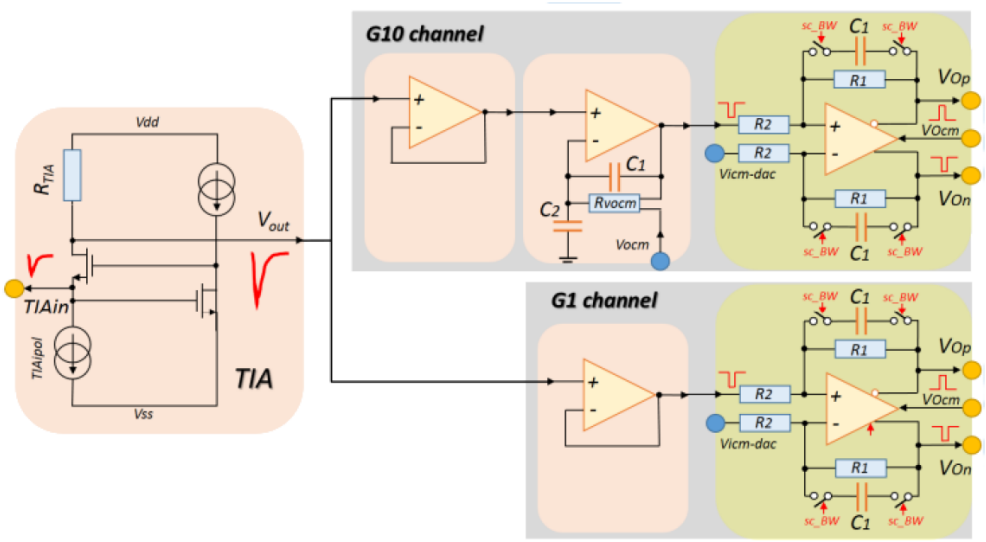


Figure 2.7: The CATIA first stage is the TIA and it has a Regulated Common-Gate (RCG) architecture. Then, the ASIC has the two gain channels with differential voltage outputs, the common mode voltage (V_{CM}) is adjustable in order to allow the coupling between CATIA and an ADC. Indeed the LiTE-DTU requires a V_{CM} = 0.6 V while the commercial ADC used during the characterization tests has a V_{CM} = 0.9 V [51].

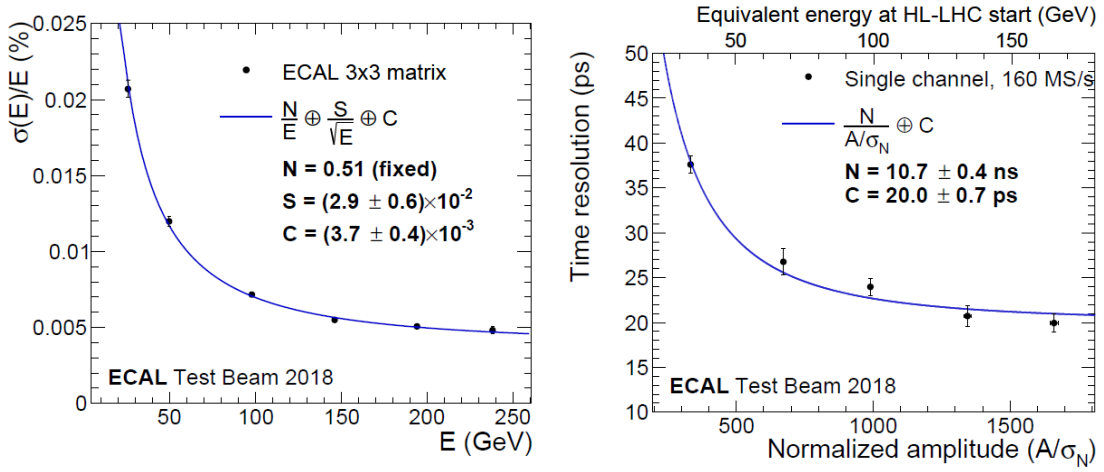
out at H4/H2 beam line of the CERN SPS with an electron beam with a momentum range between 25-250 GeV. The main results obtained during the test beam are shown in Figure 2.8. The energy resolution measurements matches with the legacy electronics performance and the time resolution on a single crystal measurement shows that a 30 ps of time resolution can be achieved for an electromagnetic shower with an energy greater than 50 GeV [52].

Therefore, CATIA has the ability to perform a precision timing measurements of the order of 30 ps for electrons and photons above 50 GeV. This characteristic is relevant because the new VFE board is not going to limit the system time resolution ($PbWO_4$ crystals have an intrinsic time resolution of about 30 ps [50]) and moreover it will improve pile-up mitigation and the rejection of the anomalous signals.

Figure 2.9a shows the single pulse response of the CATIA coupled to an APD. The light signal has been produced with a sub-ns laser and the responses of the gain x10 and gain x1 output have a similar shape signal in the time domain.

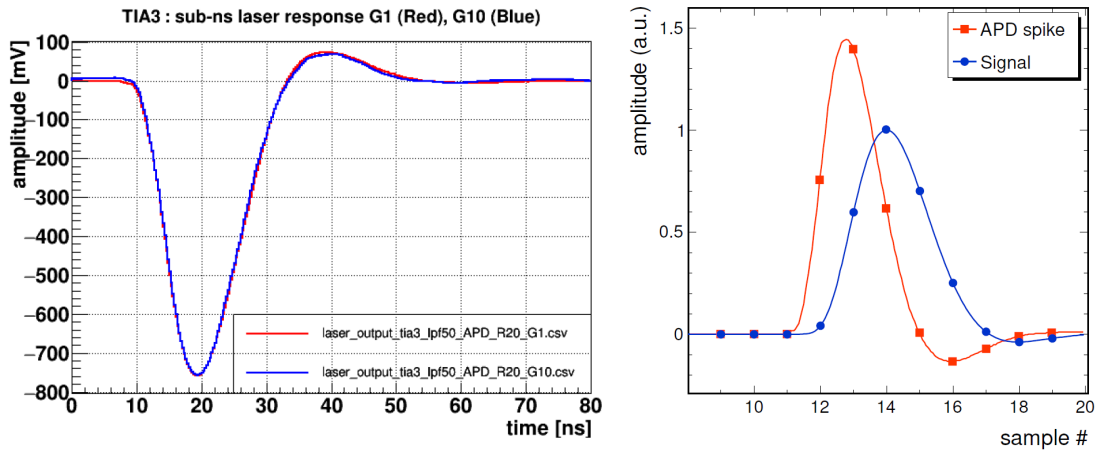
Regarding the improvement of the spike suppression foreseen for the HL-LHC phase, the rejection of the anomalous signals will exploit the pulse shape attributes. Indeed, the spike signals have a shorter arrival time and a faster rising edge in comparison with the signal obtained by the energy deposition in a crystal. This difference is due to the

absence of the scintillation component in the spike signal. A direct comparison between the two signal shapes is shown in Figure 2.9b.



(a) (b)

Figure 2.8: The energy resolution (left) and time resolution on a single crystal (right) obtained during the test beam at CERN of the CATIA_v1 ASIC [52].



(a) (b)

Figure 2.9: Signals obtained in output from the gain x10 and gain x1 channels when the source of light is a sub-ns laser, the pulses are collected by the APDs connected to CATIA ASIC (left). Comparison between the pulse shapes of a spike and a typical signal derived from scintillation, the dots represent the 160 MS/s sampling (right). [50]

LiTE-DTU ASIC

CATIA is followed by a conversion, compression, and transmission chip: the LiTE-DTU ASIC, its features and its operation are explained in detail in the next chapter but a brief description is reported here.

The LiTE-DTU receives the input signals from CATIA and first of all performs a sampling of the pulses at 160 MS/s and digitization the samples through a dual 12-bit ADCs. As in the previous version of the VFE, the system composed by the pre-amplifier and the ADC employs a multi-gain and multi-channel ADC solution to satisfy both the requirements on dynamic range and on resolution. The upgraded VFE is composed by two (instead of the actual three) gain channels to fit the gain toggle for photons. This implementation allows to preserve the detector sensitivity to the two-photon decay process [50]. For this reason, the LiTE-DTU ASIC embeds two 12-bit ADC. Simulations on the correlation between the time resolution and the sampling rates have been performed in order to optimize the ADC sampling frequency. The plot reported in Figure 2.10 that shows that 30 ps of resolution can be obtained sampling the signal with a frequency equal or above 120 MS/s. The sampling frequency of 4 GS/s has been used only for simulation purposes, in order to represent the *infinite* resolution option. However, such high rate is not reasonable taking into account the total number of channels in the EB. The baseline choice for the sampling rate has been set for convenience to 160 MHz, indeed it is consistent to the clock frequency generated by the Low power GigaBit Transceiver (LpGBT) and allows to keep some margin.

The two signals delivered by CATIA ASIC and digitized by the ADCs correspond to the same signal with two different gain, as explained previously. In addition, they cover two distinct sub-ranges so the Least Significant Bit (LSB) of the two ADCs have diverse values: for the gain x10 the LSB corresponds to 48.8 MeV while for the gain x1 the LSB matches to 488 MeV [53], [54]. These values can be obtained simply dividing the upper bound of each channel sub-range to the total number of ADC counts (a 12-bit ADC has 2^{12} = 4096 ADC counts).

The LiTE-DTU has been implemented using a commercial CMOS 65 nm technology. This technology node is sufficient for the design of the high speed logic of the ADC and digital Data Transmission Unit (DTU). During the design phase, attention to the radiation robustness has been taken in order to provide a chip tolerant to the harsh radiation environment during HL-LHC phase. Several studies have been published on the radiation hardness of the 65 nm CMOS technology both through irradiation of the devices with heavy-ion beams and X-rays ([55], [56], [57]). The results of the irradiation of digital prototypes with heavy-ion beams highlighted that there is a direct correlation between the reduction of the Single-Event Upset (SEU) (see Section 5.1.2) probability in

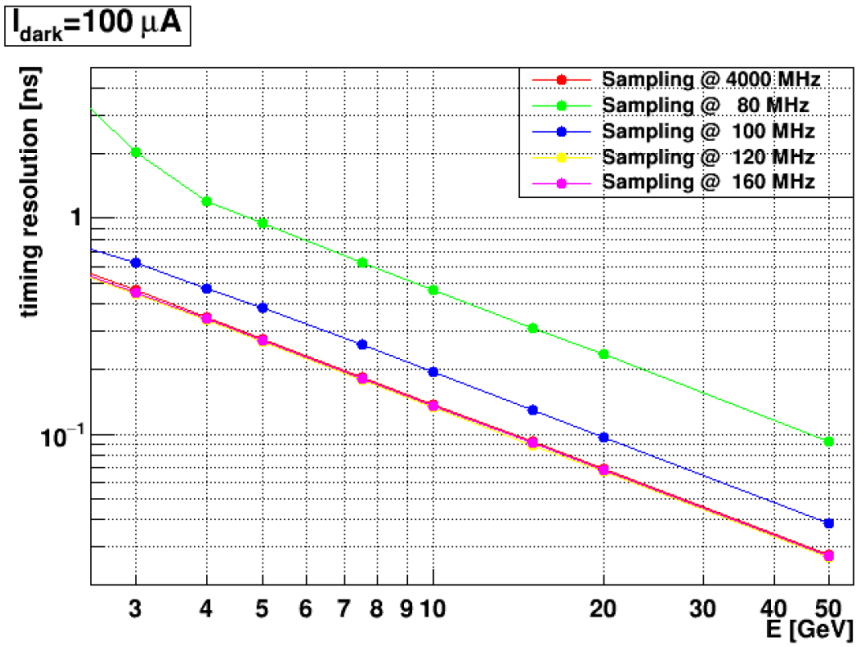


Figure 2.10: Correlation between the sampling frequency of the ADC and the timing resolution employing the CATIA chip and taking into account a level of 100 μA of leakage current in the APD [50].

a device and the decrease of the transistor size and hence its cross section [58]. However, moving from previous technologies to the standard 65 nm cells is not enough to guarantee a SEU robust technology. Indeed, a smaller technology node means that the critical energy required in order to generate an upset is lower because of the reduced node capacitance as well as the supply voltage. Moreover, the 65 nm process technology has an higher density so it allows the integration of much more logic with the same circuit area, inducing an higher SEU exposure of the chip. Lastly, the Multi Bit Upset (MBU) probability of the 65 nm CMOS technology is higher than the probability of previous technologies, therefore considerable attention must be paid during the Place & Route (P&R) design phase in order to properly separate the redundant storage cells. In the next chapters, the fault tolerant strategies employed during the LiTE-DTU design are described in details (Chapter 3) along with the radiation damage test performed in the first LiTE-DTU prototype (Chapter 5). Three plots of the simulated total dose, charged hadron fluence, and neutron fluence in the CMS central region for an integrated luminosity of 3000 fb^{-1} are shown in Figure 2.11 . Therefore, all on-detector ASICs will be qualified up to 5 Mrad, will be extensively tested for high particle fluence, and subjected to accelerated ageing during the validation phase [50].

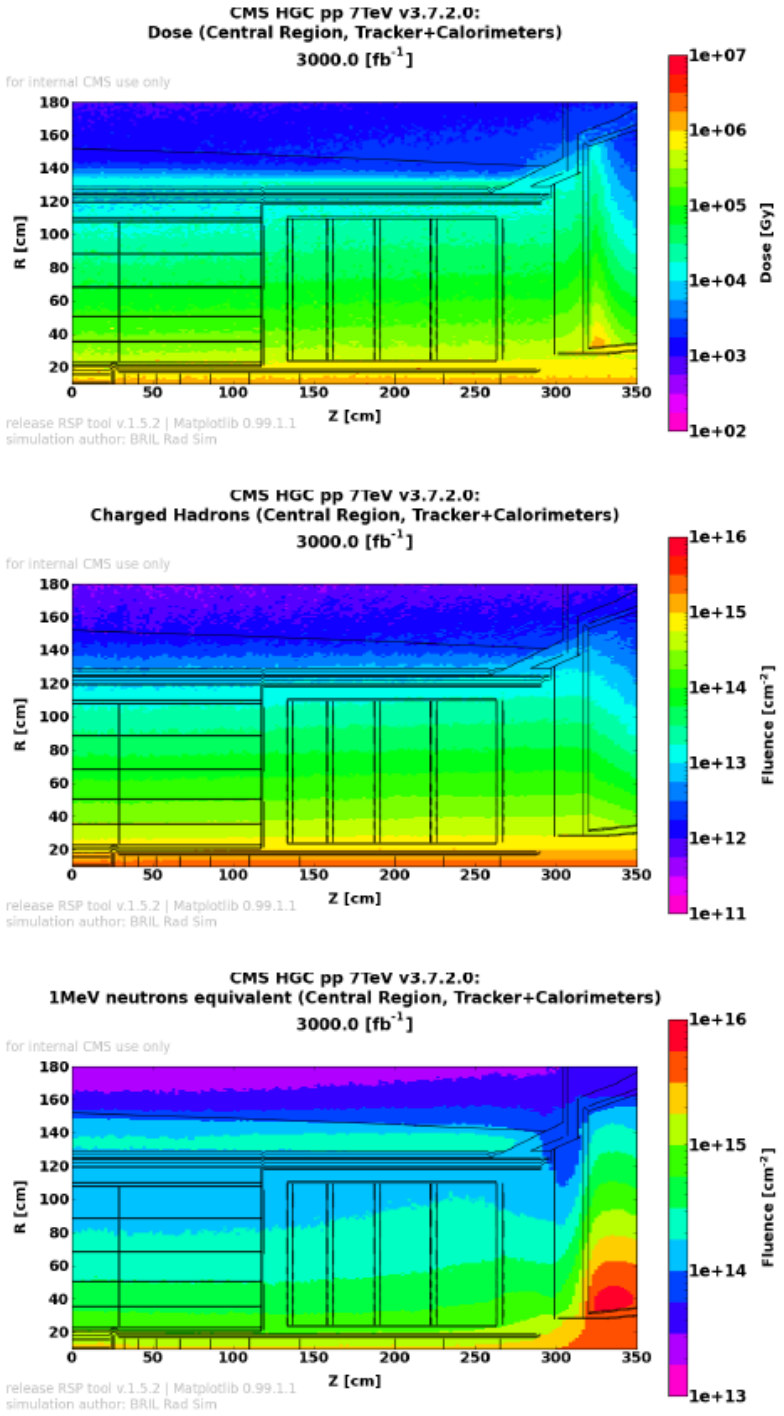


Figure 2.11: Dose, charged hadron and neutron fluence in the central part of CMS calculated by the FLUKA simulation for 3000 fb^{-1} [50].

The switching voltage regulator board

The upgraded VFE and FE boards will receive the power supply from the Switching Low Voltage Regulator Card (SLVR). In a TT, the five VFE cards will necessitate the 2.5 V for powering the CATIA and 1.2 V for the LiTE-DTU. Moreover, the FE card will need both 2.5 V and 1.2 V. The SLVR will embeds an upgraded and rad-hard DC-DC converter [59] designed for the LHC experiments during HL-LHC [50].

2.3.3 The upgraded FE board

The structural geometry of the trigger tower is maintained in the upgrade strategy, therefore the new FE board will be connected to five VFE cards, as in the legacy system. The FE board will manage the distribution of the clock signal and the control signals to the VFE boards, then it will collect the data streams and transfer these to the off-detector system via optical link. The upgraded FE card employs new technology in data transmission to transfer the single crystal information sampled at 160 MS/s to the back-end electronic system. In Figure 2.12 the baseline design of the upgraded FE board is shown.

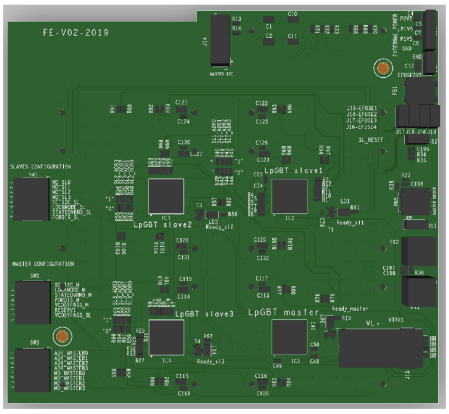


Figure 2.12: The FE board for the EB upgrade [50].

Data from the LiTE-DTU will be sent via electrical link (e-link) to the FE board. The e-link is a serial link without error protection and it can afford a data rate of 320 Mb/s, 640 Mb/s, or 1280 Mb/s [60]. Four Low power GigaBit Transceiver (LpGBT) chips are embedded in the new FE card, the LpGBT chips will concentrate and stream the VFE data and sends them to the back-end electronics via Versatile Link+ (VL+). The VL+ is capable of operating at 10 Gb/s for transmission and 5 Gb/s for reception. The upgraded FE board will allow to enhance the Level-1 trigger granularity by a factor of 25 and to to move the TPG from the FE board to the upgraded off-detector system [50].

2.3.4 Back-end readout and trigger primitive formation

The upgraded off-detector electronic system will be still placed in the CMS cavern, so the radiation hardness is not a requirement for the new electronics. However, the upgraded processor board, known as Barrel Calorimeter Processor (BCP), will have a renewed architecture in order to sustain higher data transfer rates, to perform the TPG and to comply with Level-1 trigger upgrade specifications [50]. The BCP is designed with powerful Field Programmable Gate Arrays (FPGAs) and hosts both the legacy FE operations and the processing integrated in the current off-detector electronics. The selected standard for the baseline choice is the Advanced Telecommunications Computing Architecture (ATCA) industry standard [61].

The BCP scheme and the electronic chain with the FE board and the Level-1 trigger system is represented in Figure 2.13. The BCP processor will embeds several algorithm for spike rejection, process and conversion of the digital samples of a pulse into an E_T information, elementary clustering, TPG, and management of the clock and control signals to the FE board [62].

The upgraded off-detector electronics will receive data from the FEs, perform data integrity checks and the event data alignment to beam crossings. The TCC functionalities will be integrated in BCP functions as well as the DCC and the CCS.

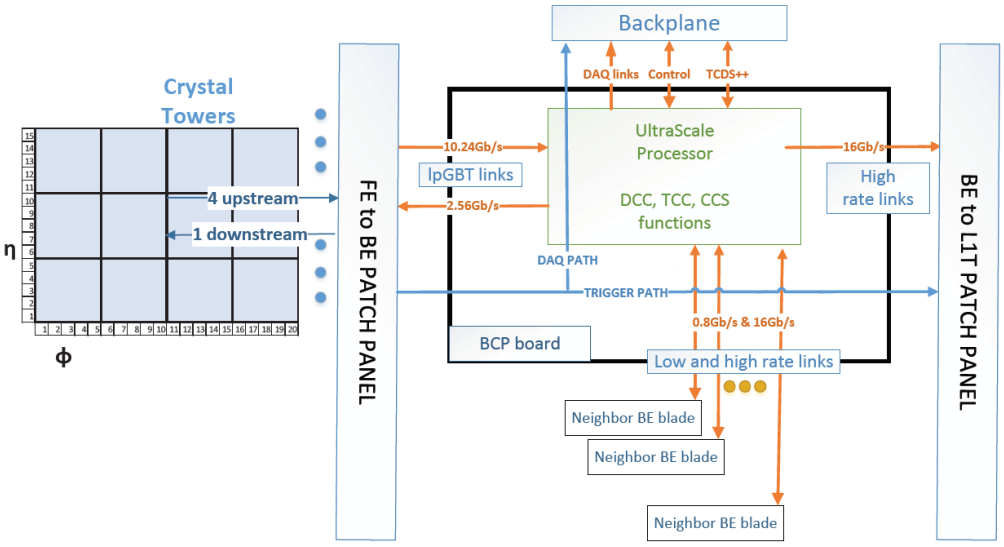


Figure 2.13: Representation of the connections between the FE board, the BCP board and the Level-1 trigger system [50].

2.3.5 The EB electronics upgrade in numbers

The primary requirement of the EB upgrade is to retain the Run-1 physics performance at the HL-LHC conditions. The vast majority of the readout chain shall be refurbished in order to accomplish the challenging target and to meet the new requirements in terms of bandwidth and latency. In Table 2.1 all the new boards along with the required quantity of cards summarized.

Number of readout channels	61200
Number of VFEs	12240
Number of CATIA ASICs	61200
Number of LiTE-DTU ASICs	61200
Number of SLVR cards	2448
Number of FE boards	2448
Number of LpGBTs	9796
Number of data links	9796
Number of control links	2448
Number of BCP cards	108
Number of FPGAs	216
Number of input links	12240
Number of output links	3060

Table 2.1: Summary of the on-detector and off-detector hardware needed for the EB Phase-2 upgrade.

Chapter 3

LiTE-DTU circuit architecture

LiTE-DTU ASIC has been developed for the upgrade of the VFE board of the EB at CMS. The chip has been implemented in a 65 nm CMOS technology and has a size of 2×2 mm^2. The ASIC purpose is the readout of the analog signals coming from the CATIA ASIC, the digitization of the samples, an online data compression, and lastly the high-speed serial data transmission to the FE system.

The LiTE-DTU chip embeds a custom Analog to Digital Converter designed by an external company, the Phase-Locked Loop inherited from the CERN LpGBT project and the digital architecture designed at INFN Torino.

In the earlier part of this chapter, the first prototype of the LiTE-DTU is described in order to provide the ASIC overview. The second part is dedicated to the detailed description of the several blocks included in the design. These sections will set the background for the ASIC characterization chapter. In the last part of the chapter, the implementation of the Data Transmission Unit (DTU) is described along with the performed post-layout simulations and the latency study.

My contribution in the design architecture phase has been mostly on the design of the DTU, from the Register Transfer Level (RTL) up to the final physical layout. The RTL description has been implemented using Verilog, an Hardware Description and Verification Language (HDVL) [63]. During the design the top-down methodology has been pursued, therefore the project started from the definition of the top-level block and the delineation of all the useful sub-blocks. Moreover, several test simulations have been performed in order to characterize the DTU latency and verify the system robustness and the fulfillment of the requirements set by the physics conditions at the HL-LHC accelerator.

3.1 ASIC overview

The LiTE-DTU architecture is based on several functional blocks: 2 ADC IP blocks, a Phase-Locked Loop (PLL), a DTU for data selection, compression and serialization, a synchronization unit, an ADC Test Unit (ATU) and an Inter-Integrated Circuit (I^2C) interface. In order to meet the requirements in Table 3.1, the first prototype has been submitted with the following goals:

- perform standalone test of the ADC IP block;
- validate of the radiation tolerance of the full chip;
- evaluate of the compression method;
- perform system tests within VFE and FE boards.

Specification	Requirement	Note
ADC sampling rate	(80 - 160) MS/s	
ADC resolution	12 bits	
ADC supply voltage	1.2 V	min: 1.08 V, max: 1.32 V
ADC input range	$\pm$ 600 mV	differential
ADC common mode	600 mV	
Output data rate	1.28 Gb/s	in DTU mode
Output data rate	4×1.28 Gb/s	in ADC test mode
Technology	CMOS 65 nm	9 + 1 metal stack
TID tolerance	20 kGy	min value
SEU tolerance	15 MeV cm^2 / mg	min value
DTU latency	< 350 ns	
DTU compression level	> 60%	

Table 3.1: LiTE-DTU requirements.

LiTE-DTU ASIC operates with two different clocks: the first one is the 160 MHz clock (CLK_{160}) and the second is at 1.28 GHz ($CLK_{1.28}$). The former is an external signal that feeds by the ATU, DTU, synchronization unit, and the PLL. The PLL block is used to generate the second clock at 1.28 GHz which is sent to the ADCs and the serializers in the DTU. For ADC characterization purposes, there is the possibility to bypass the PLL and pilot the ADCs with an external clock ($CLK_{1.28\ ext}$) to de-couple the ADCs from the PLL clock generation.

Fault tolerant strategies

In order to obtain a fault-tolerant design, a synchronous active low reset network has been selected and specific methods have been applied during the block design:

- The majority of the blocks have been protected against radiation-induced upsets by using the Triple Modular Redundancy (TMR) technique: the logic is triplicated, each unit performs the same process and then the results are compared by a majority voter. If there are no circuit failures the output is straightforward because the three outputs are identical. If a fault occurs and one output is different the majority voter can correct and mask the fault. The TMR in this ASIC has been implemented using the Triple Modular Redundancy Generator (TMRG) tool: it automatizes the triplication process and ensures that the additional logic is preserved through the design process [64].
  - TMR has been implemented for flip-flops, registers, memory pointers and Finite State Machines (FSM)s. Moreover, during the Place&Route phase, all the triplicated components have been placed spaced apart of at least 20 μm in order to prevent that a Single-Event Effect can upset two different elements of the same TMR group. In Figure 3.1, on the right, the TMR partitions of the DTU are represented;

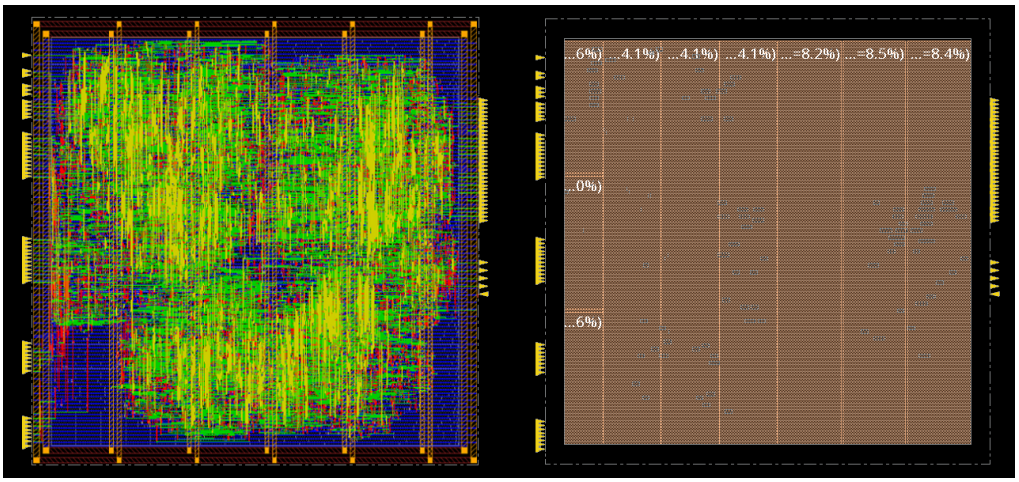


Figure 3.1: Floorplan view (left) and amoeba view (right) of the DTU.

  - The clocks networks have been triplicated.

- An Error Correction Coding (ECC) has been applied both for reliable communication between the outside world and the Synchronization unit and for data protection in the compensation memory embedded in the DTU (more details about the individual implementations can be found in the following sections). The selected ECC is the Hamming code [65], [66], [67], a methodology based on the calculation of parity bits. Parity bits are additional bits which are placed in positions corresponding to the power of 2 and represent a XOR function of groups of

data bits. The encoding phase consists in parity bit calculation while the decoding phase involves the parity bits check and the eventual data recovery in presence of a bit-flip during transmission.

- Cyclic Redundancy Check (CRC) has been adopted for error detection and correction of the 32-bit packets. The CRC information is inserted in the frame trailer.
- The standard cells NR4*, I*NR4, OR4* have been avoided in order to prevent their usage during synthesis phase. These cells have four pMOS transistors in series and are the most critical because the pMOS transistors have shown an higher degradation after irradiation in comparison with the nMOS transistors [68].

3.1.1 ASIC layout

The LiTE-DTU has been integrated using a top-down digital-on-top approach. The layout of the first submitted prototype of the LiTE-DTU is shown in Figure 3.2a. As reported above, the ASIC size is 2×2 mm^2. Figure 3.2b highlights the LiTE-DTU pinout, the 63 pads are organized in the following way:

- 16 pads on the top side are associated to the ADCs and SEU signals, they host: input/output power domain, ADCs external clock ($CLK_{1.28}$ext), calibration input and output signals, ADC overflow signal, three I^2C pads (for address 4, 5, and 6), digital power domain, and two Single-Event Upset signals (analog and digital);
- 14 pads on the right side are related to the ASIC output, clock and synchronization input; they host: four digital output for serial data transmission, input/output power domain, synchronization and clock (CLK_{160}) input signals; all these I/O signals are differential;
- 16 pads on the bottom side are associated to the PLL and I^2C, they host: some output signals coming from the PLL as the PLL_lock and the PLL_clk, power-on reset signal, the PLL Voltage Controlled Oscillator decoupling capacitor, PLL, input/output and digital power domains, data and clock signals of the I^2C, and two I^2C pads (for address 2 and 3)
- 17 on the left side are related to the ADCs and they host: the signal for the activation of the ADC test, input/output power domain, and for each ADC: 2 reference voltages, 2 analogue input and the analogue power domain.

Figure 3.2b indicates the blocks embedded in the LiTE-DTU with different colors: in blue there are the two ADCs, in light green the ATU, in dark green the DTU, in orange the synchronization unit, in yellow the PLL, and lastly the I^2C in red.

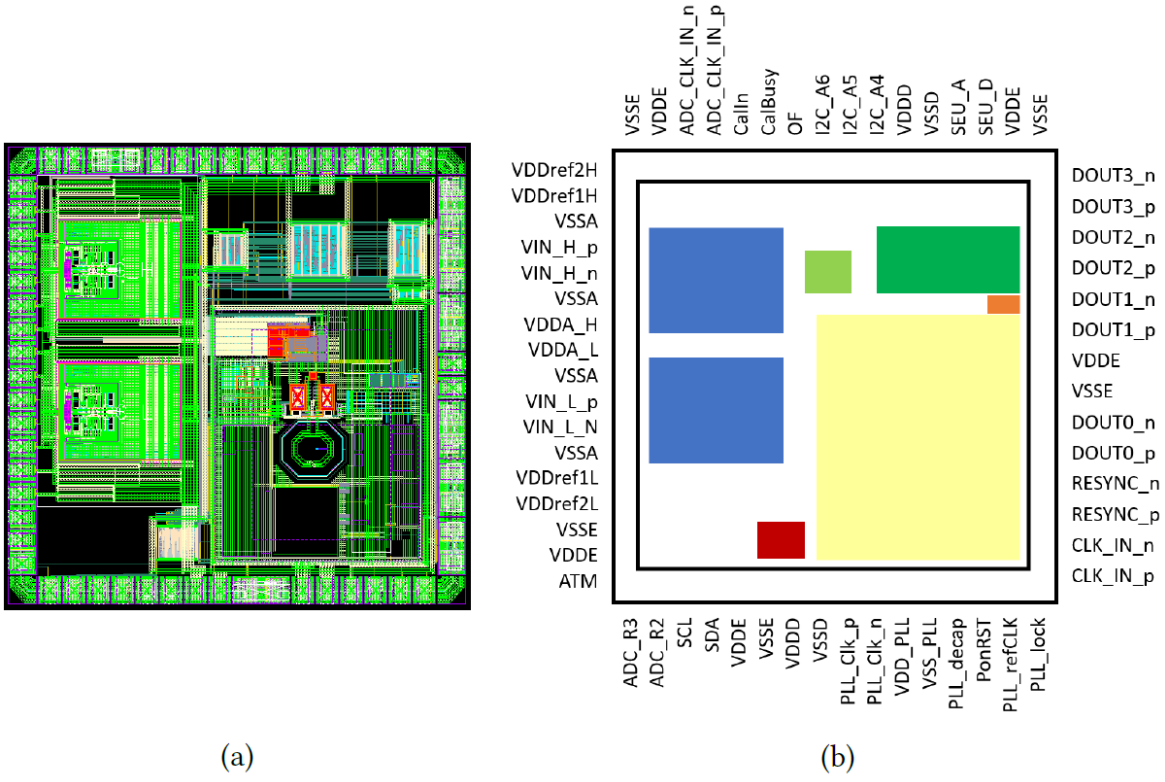


Figure 3.2: LiTE-DTU first prototype layout (left) and pinout and blocks scheme (right).

Power distribution

The power supply is distributed through a power network which employs the thicker metal layers: M7 and M8. The power supply grid is partitioned in order to keep the analogue and the digital power domains distinct and to separate the power supply for the main blocks:

- 3 analogue supplies for ADCs;
- 1 digital supply shared between ADCs, DTU and the low frequency section of the PLL;
- 1 RF supply for the PLL;
- Input/Output drivers and receivers power supply.

3.2 Synchronization unit

The main purpose of the synchronization unit is the management of the blocks reset and the start-up of the ADCs calibration. This is accomplished through the serial-to-parallel data conversion of the resync input signal, and its [8,4] Hamming decoding for reliable communication in the radiation environment. Moreover, in order to make sure to obtain a fault-tolerant unit, the TMR configuration has been applied to the synchronization block.

The synchronization block receives a serial input data and through a first FSM, which decodes the bit stream in a 8-bit word. The FSM remains in an idle state until the *start condition* occurs, then it switches to the load state, where the command words are properly aligned. The FSM state switches between the wait state, during the new word alignment, and the load state until the arrival of the *stop condition*, which brings the FSM back in the idle state. A scheme of the FSM is represented in Figure 3.3. Then the captured 8-bit word has to be decoded in a 4-bit word, through an Hamming decoding. Subsequently a second FSM manages the reset of the units and the ADCs calibration signal.

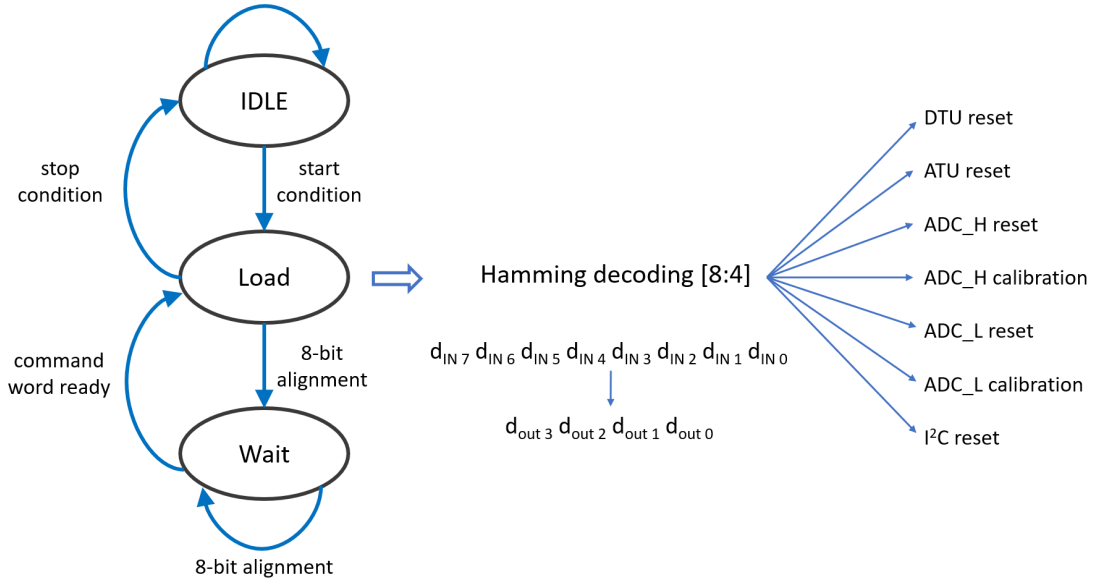


Figure 3.3: Scheme of the FSM used to capture the input command. This phase is followed by the Hamming decoding of the message and a second FSM which manages some operations on the LiTE-DTU blocks.

3.3 Inter-Integrated Circuit

An I^2C interface has been implemented in the LiTE-DTU ASIC in order to upload/-download the configuration registers. The I^2C is a standard bidirectional interface commonly used for managing communications between a master and several slave devices, as shown in Figure 3.4. Each slave on the I^2C bus has a unique address in order to be easly reachable or recognized by the master.

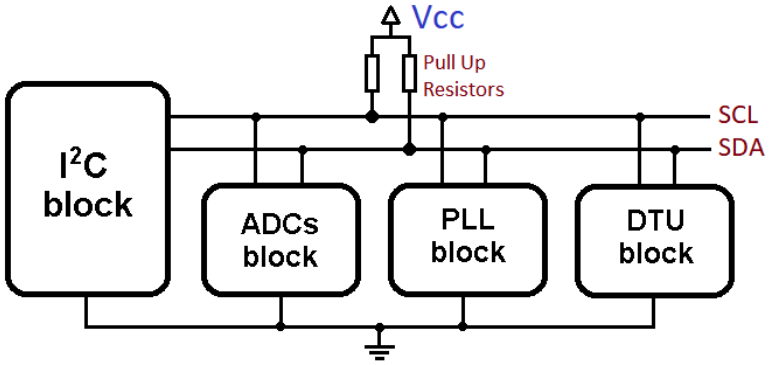


Figure 3.4: Scheme of the I^2C interface in the LiTE-DTU.

At the startup, all the blocks require an initial configuration with the purpose of set the device behavior.

The I^2C interface employs two analogue signals: the Serial Clock (SCL) and the Serial Data (SDA) lines. Both SDA and SCL lines must be connected to VCC through a pull-up resistor.

The communication always begins with a *start* condition sent from the master, then the address of the requested device is transmitted. The latter is followed by the data and lastly by the stop condition. When there is no active communication, the I^2C bus stays in an idle state. This procedure is the same both when the master is a transmitter or when it is a receiver, the only difference is who sends the data message: in the first case the transmission direction is going from the master to the slave while in the second case the direction is the opposite one. An example of the full procedure is represented in Figure 3.5.

3.3.1 I^2C states

The I^2C bus can be in one of four states, it is fully defined by the value of the SCL and SDA lines. The possible states of the bus are: idle, start condition, data transmission, and stop condition.

- the **idle** condition occurs when both SDA and SCL lines are high after a stop condition. Only when the bus is in idle the data transmission can start.
- the **start** condition can be activated only by the master, it occurs when the SDA line transits from high-to-low while the SCL is high.
- the **data transmission** occurs after the start and the transmission of the slave address by the master. During each clock pulse of the SCL one data bit is transferred on the SDA line. Data are transferred in a big-endian order, so the first bit is the Most Significant Bit (MSB) and the last is the Least Significant Bit (LSB). The standard length of a message is of 8-bit while a device or register address has a length of 7-bit and are always followed by a write/read bit. There is no limit on the number of messages transmitted between a start and stop condition.
- the **stop** condition occurs at the end of data transmission, the SDA line transits from low-to-high while the SCL is high.

3.3.2 Acknowledge and not acknowledge

An Acknoledge (ACK) bit sent from the receiver always follows each byte of data or each address byte as shown in Figure 3.5. The ACK bit indicates that the transmission has been successful and another message may be sent. The ACK can be sent by the receiver only if the transmitter has released the SDA line, then the former shall pull down the SDA line during the low phase of SCL. If the SDA line stays high during the ninth clock period, this means that a Not-Acknoledge (NACK) has occurred. This can indicate that the addressed slave did not respond or was unable to process the request.

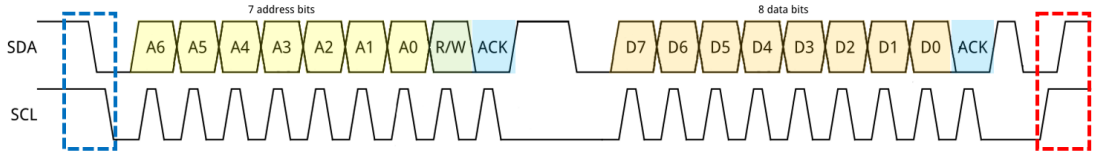


Figure 3.5: Scheme of the transmission procedure. The blue and the red dotted lines highlight the start and stop conditions, respectively. The yellow bits are the address, the orange ones are the data, and the light blue bits are the ACK/NACK bits.

3.4 Phase-Locked Loop block

The Phase-Locked Loop (PLL) block integrated in the LiTE-DTU ASIC has been inherited from the Low power GigaBit Transceiver (LpGBT) project [69], which is the upgrade of the existing GigaBit Transceiver (GBT) [70]. The LpGBT is a high-speed serializer/deserializer device, it has been designed in CMOS 65 nm technology and it will be adopted by both CMS and ATLAS in the foreseen front-end electronics upgrade for the HL-LHC [69] [71]. The LpGBT PLL has the following characteristics [72]:

- It is based on a Charge-Pump Phase-Locked Loop (CP-PLL) configuration with a radiation hardened Phase-Frequency Detector (PFD) and a frequency divider which are protected through the TMR technique;
- It integrates an innovative LC-oscillator architecture which protects the system against to single-event transients by a new varactor topology and it is optimized for a low phase noise.
- The PLL has a Automatic Frequency Calibration (AFC) block, the AFC allows to automatically select the VCO frequency band at the PLL power-up. The AFC is fully digital and TMR protected, it performs a calibration algorithm which controls the bank of switched capacitors in the Voltage Controlled Oscillator (VCO) through a 9-bit voltage DAC.

The architecture of the PLL block is shown in Figure 3.6.

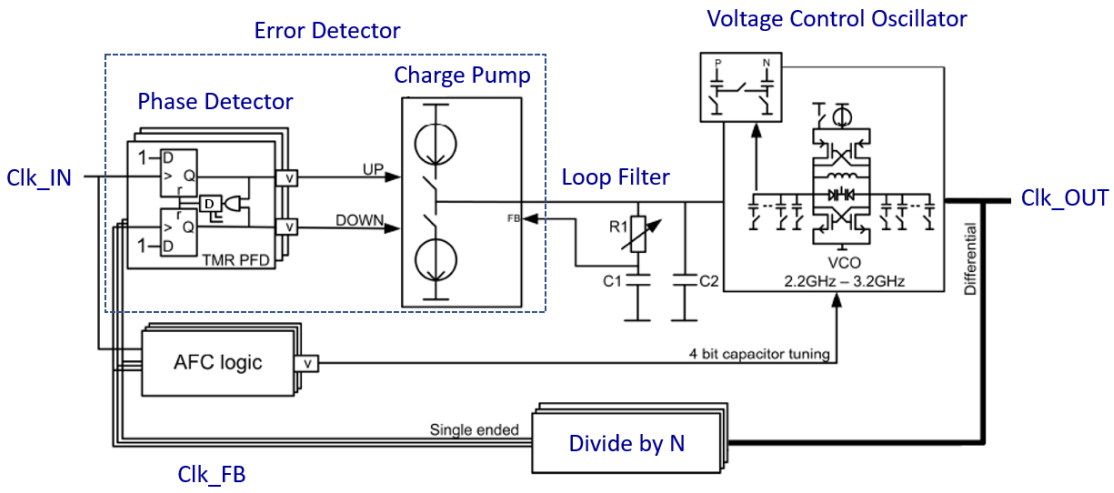


Figure 3.6: The LpGBT PLL block diagram [72].

3.4.1 PLL structure and operation

The PLL purpose is to provide an high frequency clock to the LiTE-DTU, which is derived from a lower frequency clock in input to the PLL. The LiTE-DTU blocks rely on correctness of the PLL operations, therefore a stable and reliable generated clock is essential. The CP-PLL embedded in the LiTE-DTU is used for the $CLK_{1.28}$ generation from the input CLK_{160}. The CP-PLL is composed ov several blocks: an Error Detector (ED) (composed of a PFD and a Charge-Pump (CP)), a Loop Filter (LF), a VCO, a feedback divider, and a AFC [73], [74].

The PFD checks the frequency and the phase difference between the input clock (Clk_IN) and the feedback clock (Clk_FB), then it feeds the *charge-up* or the *charge-down* branches of the CP with pulses that are proportional to the sensed discrepancy. These pulses enable a positive or a negative current sources. The CP output is a current that is a correction signal related to the phase error detected by the PFD. The CP current induces a charge/discharge of a capacitor in the LF [75]. Therefore the LF integrates these currents to produce a tuning voltage to steer the VCO, which modulates the oscillation frequency as a function of its input voltage. Therefore, the LF is one of the most critical node of the PLL because any noise injected into this node provokes an alteration of the VCO output frequency and this alteration is reflected in the PLL output jitter. Another critical node of the PLL design is the matching of the CP currents: mismatch and leakage in the CP imply a phase error on the PLL output. Lastly, the divider block generates a feedback signal which has a frequency equal to an integer multiple of the VCO output frequency (f_OUT) [76]. Therefore, the PLL is *locked* when the $f_{OUT} = N * f_{IN}$ and means that Clk_FB and the Clk_IN are both phase and frequency aligned. In this condition the CP retains a constant voltage value to the LF.
The behavior of the ED components is shown in Figure 3.7.

- The scenario 1.a describes a system which is out of lock and the f_{Clk_FB} is lower than the f_{Clk_IN}. The ED drives the VCO in the positive direction from the first rising edge of the Clk_IN and the value is maintained high until the first rising edge of the Clk_FB. The ED output drives the the input of the VCO, thus an high value of the ED results in an increase of the f_{Clk_FB}.
- The scenario in 1.b is the reverse condition shown in 1.a: indeed, the f_{Clk_FB} is higher than the f_{Clk_IN}, thus the ED drives the VCO in the negative direction in order to bring the Clk_FB frequency much closer to the reference frequency and to approach the locked condition.
- The scenario 2.a describes a frequency-locked feedback signal but the phase of Clk_FB is not equal to the phase of the reference signal. Since Clk_IN is leading

the Clk_FB, the output of the ED is a sequence of positive current pulses. In this case, the VCO tries to align the phase of the Clk_FB to the Clk_IN phase.

- The scenario in 2.b is the reverse condition shown in 2.a: the Clk_IN is lagging behind the Clk_FB, thus the output of the ED is a sequence of negative current pulses. The VCO tries to align the phase of the Clk_FB to the Clk_IN phase.
- The scenario 3 describes the *lock condition*: in this case the Clk_IN and the Clk_FB are perfectly phase-aligned and frequency-locked. There are still several current pulses generated from the ED in order to prevent the phenomena known as the *dead zone* effect. A PLL is in the *dead zone* when the CP currents are not proportional to the phase error detected by the PFD and as consequence a significant spur can appear in the VCO output spectrum [77]. This spur is a sub-harmonic of the PFD reference frequency and if it is a low frequency signal the LF is not able to filter the spurs [76]. The *dead zone* can be avoided by inserting a delay, in the PFD reset path in order to obtain a pulse longer than the minimum switching time of the CP currents.

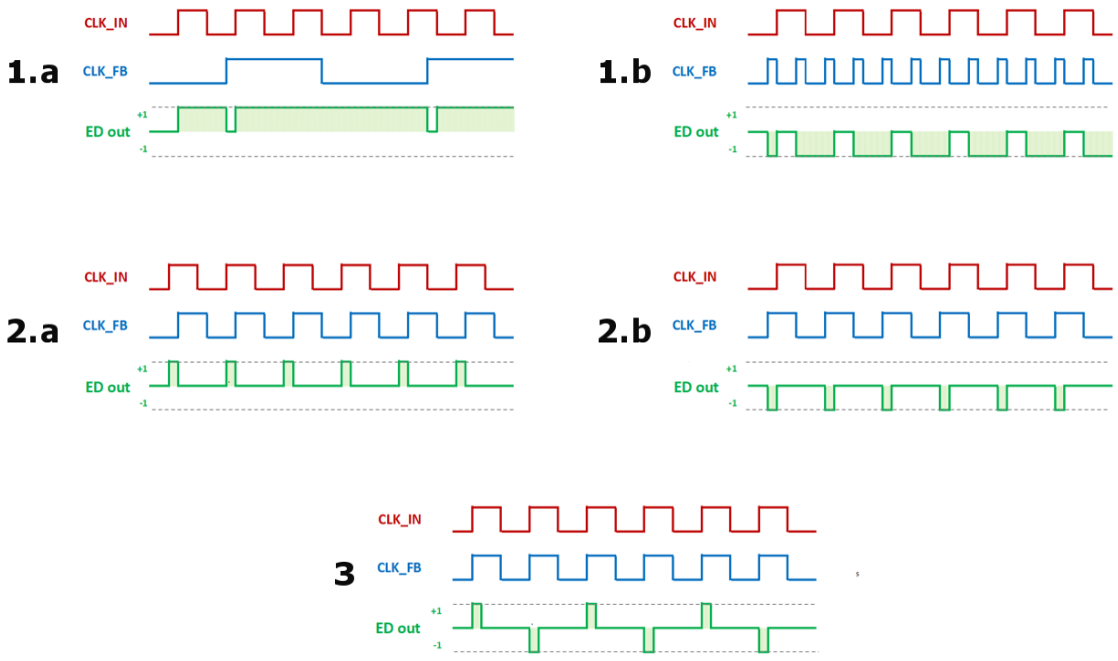


Figure 3.7: Representation of the ED response in three main different situations:
• (1.a) and (1.b): $f_{Clk\_FB} \neq f_{Clk\_IN}$ and $\theta_{Clk\_FB} \neq \theta_{Clk\_IN}$;
• (2.a) and (2.b): $f_{Clk\_FB} = f_{Clk\_IN}$ and $\theta_{Clk\_FB} \neq \theta_{Clk\_IN}$;
• (3): $f_{Clk\_FB} = f_{Clk\_IN}$ and $\theta_{Clk\_FB} = \theta_{Clk\_IN}$ which is the lock condition of the PLL.

3.5 ADC IP blocks

The LiTE-DTU embeds two accurate ADCs for the digitization of the input signals. Henceforth, the two ADCs are called ADC_H and ADC_L since in the final system they will be connected to the gain x10 and the gain x1 outputs of the CATIA. However, the two ADC are identical, the *H* and *L* labels are referred only to their connection in the final system.

The ADC IP block has been designed by *Adesto* (Lisbon, Portugal) and it is based on the Successive Approximation (SAR) architecture. The ADC supports digitization with 12-bit of resolution over a dynamic range of 1.2 V, with a conversion rate of 160 MS/s.

The ADC IP block design implements the time interleaving technique, i.e. two identical ADCs process data at half the sampling rate of the single ADC. Therefore, in order to achieve all the requirements set for the design of the ADC, two kinds of calibration have been implemented. The background calibration procedure of each interleaved ADCs and the intercalibration between them. The ADC specifications are summarized in Table 3.2 and the scheme of the ADC is shown in Figure 3.8.

Specification	**Requirement**	**Note**
Architecture	SAR	
Applied technique	Interleaving ADCs	2 cores at 80 MS/s
Sampling rate	(80 - 160) MS/s	
Resolution	12 bits	
Supply voltage	1.2 V	min: 1.08 V, max: 1.32 V
Input range	$\pm$ 600 mV	differential
Common mode (V_{CM})	600 mV	
Integral Non-Linearity (INL)	$\pm$ 1.5 LSB	max value
Differential Non-Linearity (DNL)	$\pm$ 0.9 LSB	max value
Effective Number of Bits (ENOB)	10.2	with f ≤50 MHz
Operational temperature	25°C	range (-20, 85) °C
Power consumption	20 μW	
Latency	15 T_{clk}	
Calibration time	38200 T_{clk}	max value
Technology	CMOS 65 nm	9 + 1 metal stack
TID tolerance	20 kGy	min value
SEU tolerance (control only)	15 MeV cm^2 / mg	min value

Table 3.2: ADC requirements for the LiTE-DTU ASIC.

The ADC IP block receives two clocks, the 160 MHz sampling clock (CLK_{160}) from the ADC_CLK_IN input pads and the 1.28 GHz working clock, which, in the current

prototype, can be provided either directly by the PLL ($CLK_{1.28}$) or by the external input pads ADC_CLK_IN ($CLK_{1.28\ ext}$). The clock multiplexer is driven by the third bit of the ADC control register.

In order to avoid synchronization problems between the two clocks, the ADC sampling clock can be inverted (from rising edge to falling edge and vice versa) by changing the value of the fourth bit of the ADC control register.

The calibration cycle of the ADC starts in four different conditions: after an ADC reset, when a calibration command is received by the synchronization unit, when a calibration command is sent via the external pad CalIn, or if the fifth bit of the ADC control register is enabled. The calibration values are determined and temporarily stored in unprotected registers. Only at the end of the calibration phase they are passed to SEU-protected registers. Therefore the calibration procedure must be activated when the SEU probability is negligible (e.g. in ECAL environment when there is no beam).

The ADC output can be coded either as straight binary or two's complement. This feature can be activated enabling the second bit of the dedicated control register.

The ADCs require two external signals for the ADC calibration procedure: 850 mV and 350 mV on the VINH± and VINL± input pads, respectively.

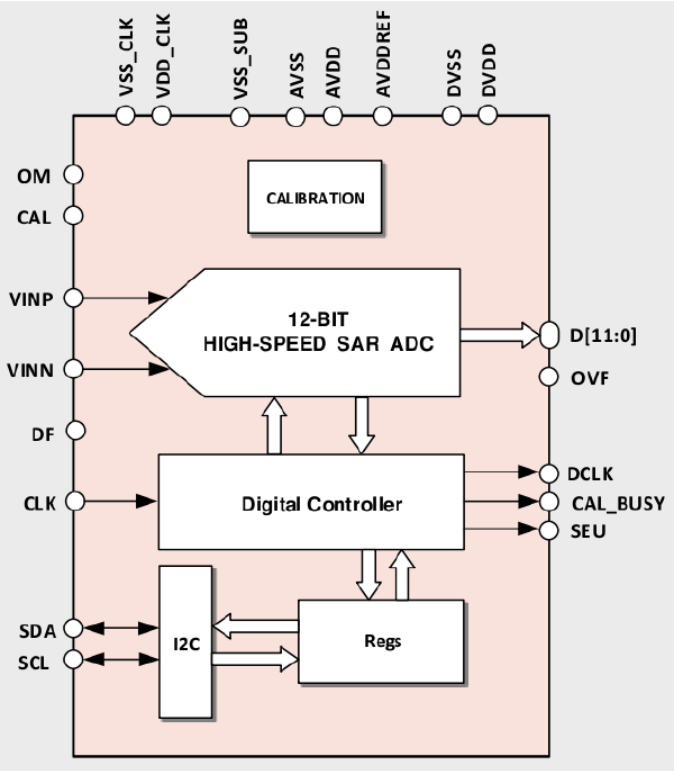


Figure 3.8: ADC IP block designed for the upgrade of the VFE board of the EB [78].

3.5.1 The Successive approximation architecture

The SAR algorithm is a popular technique employed for the ADCs because it allows both fast conversion time and high resolution [79] [80]. Indeed, the required time for a digitization is independent of the input voltage signal, it is fixed and equal to *n* clock periods for an *n*-bit ADC. The SAR ADC topology is composed of a Sample-and-Hold (S/H), a comparator, a SAR, and lastly a n-bit DAC. Figure 3.9 shows the block diagram of a SAR ADC.

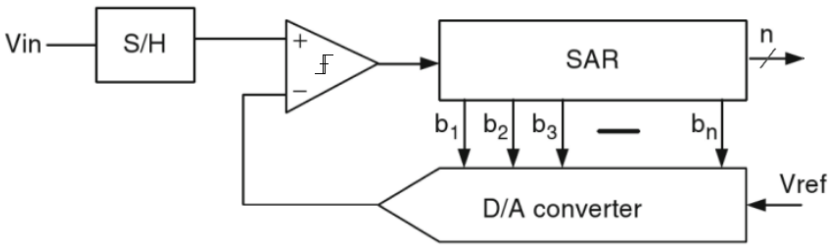


Figure 3.9: Scheme of the basic structure of a SAR ADC.

The SAR ADC implements a binary search to find the conversion result one bit at time, starting from the MSB. Therefore, the conversion technique consists in several comparison steps of the unknown analog input with an accurately-known internal voltage generated by the DAC. Each conversion is independent from the previous one because at the arrival of the conversion command, the S/H is set in the *hold* mode and all the bits of the SAR output register are reset except the MSB. Indeed, the conversion procedure starts comparing the input to the converter MSB value, which is the mid point in the ADC Full Scale Range (FSR). The SAR output drives the internal DAC which generates a voltage proportional to the SAR signal. If the signal in input is greater that DAC output, the bit in the output register is left set to the high logic value. On the other hand if the input is less than the internal DAC output, the bit in the output register is reset to 0. During the successive *n-1* steps, the procedure is repeated with each bit in turn, descending the bit weight. The process continues until the whole output register bits are defined. At this point, the contents of the SAR register coincide to the digital value of the analog input and the *end-of-convert* signal indicates that the digital sample is ready [81] [82].

Typically in a SAR ADC, the DAC structure is based on a binary-weighted capacitors network. The capacitors network is shown in Figure 3.10 and the parallel branches in the network can switch between a reference voltage V_{REF} and ground. The analog input signal (A_{IN} is the counterpart of the digital code output of the SAR. During each iteration cycle, the SAR output is sent to the DAC, it allows to charge/discharge the parallel

combination of the all capacitors in the network. When a bit capacitor is switched to V_{ref}, the network adds a voltage to node *A* that corresponds to the weight of that bit. On the other hand, when the bit capacitor is switched to ground, the voltage is subtracted from node *A*. The DAC output is the internal voltage signal that is compared with the sampled input signal.

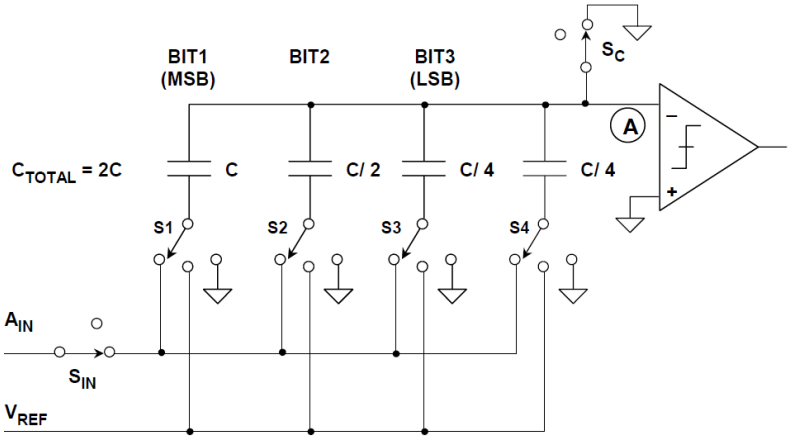


Figure 3.10: Structure of a binary-weighted capacitors network 3-bit DAC [82].

3.5.2 Characterization of an ADC

A 12-bit ADC can generate 2^{12} digital codes. With a differential FSR of 1.2 V, the LSB corresponds to 0.29 mV.

The ideal transfer function of an ADC is a model that describes the relationship between the continuous analog input signal and the discrete digital values in output [83]. The ideal transfer function is the straight line curve which approximates the staircase curve obtained by dividing the FSR into uniform intervals with nominal width Q and the number of code transition levels is 2^N - 1. The ideal transfer function can be represented by $D = K + G{\cdot}A$, where D is the digital code, A is the analog signal, K is the offset (ideally, for an unipolar ADC, K is zero), and G is the ADC gain. An example of the transfer function curve of a 3-bit ADC is shown in Figure 3.11.

The quantization process performed by an ADC causes errors that contribute to the discrepancy between the ideal transfer function and the actual transfer curve. The quantization error is the unavoidable result of the conversion process with a finite number of bits, even for an ideal ADC. If a ramp signal is given to an ideal ADC, the output error curve is a sawtooth waveform with maximum error equal to $\pm \frac{1}{2} LSB$. The quantization error as a function of input signal value is shown in Figure 3.11. The quantization

error spreads uniformly over the Nyquist [3] bandwidth: from DC to $f_s/2$, where f_s is the sampling frequency. The rms value of the quantization noise is $\frac{Q}{\sqrt{12}}$ [84] [85]. Real ADCs have additional errors that limit the performances and they can be categorized as static and dynamic errors.

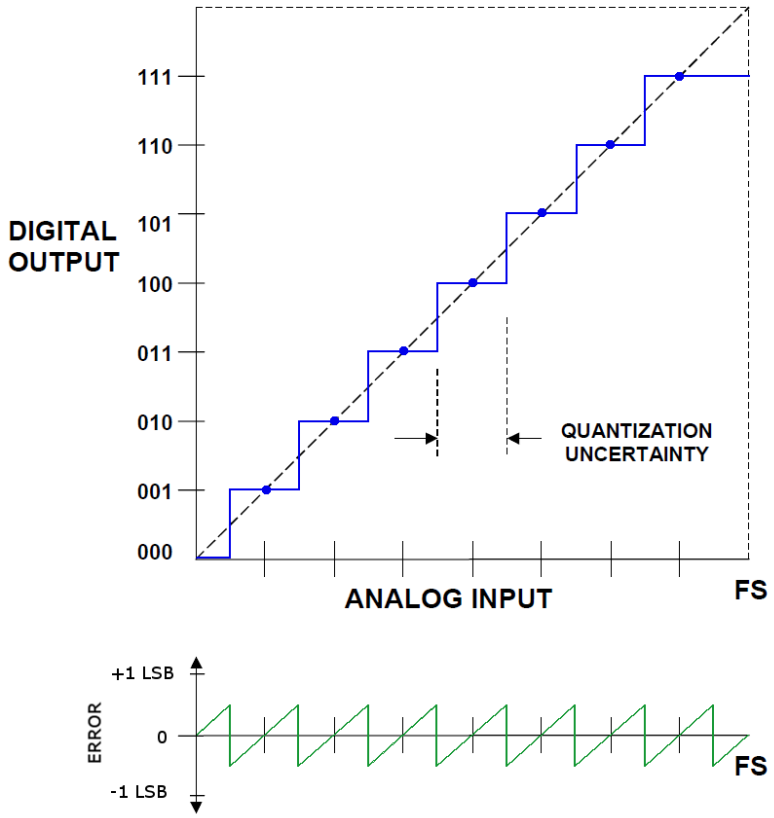


Figure 3.11: The top plot shows the representation of the transfer function curve (the dashed straight line) and the staircase curve (blue line) of an ideal 3-bit ADC [82] using the mid-tread convention. This convention sets the first transition at $Q/2$ above the minimum value of the FSR midpoint of the levels is in the middle of the code [83] [84]. The bottom plot represents the quantization error of an ideal ADC that receives a ramp signal in input.

[3]The Nyquist criteria requires that the f_s has to be at least twice the highest frequency contained in the input signal in order to obtain an accurate digital representation of the analog input and to avoid losing information. If f_s is less than twice the maximum analog signal frequency, a phenomenon known as aliasing will occur.

Static performance

The non-ideal elements integrated in the ADC design can generate a displacement of the code transition points and therefore a shift of the transfer function. An ADC can have four different DC errors: offset error, gain error, and two types of linearity errors: differential and integral. Gain and offset errors influence all codes uniformly but through pre-processing or post-processing these errors are corrected.

- The **offset error** is the deviation of the bottom end point of the transfer function from the ideal one. The offset generates a shift of the transfer function and due to the shift a fraction of the ADC range is lost. Indeed, if the offset is positive the digital output starts to saturate before reaching the ideal maximum analog value. On the other hand, with a negative offset error the digital output saturates to the all zeros value before reaching the ideal minimum analog value [82]. An example of positive offset shift is shown in Figure 3.12 (red line).
- The **gain error** is the deviation between the actual transfer function curve from the ideal one, measured at the midpoint of the last step of the ADC, with the offset error component removed. In presence of a gain error, the actual transfer function has a different slope from the ideal transfer function [85]. An example of transfer function affected by gain error is shown in Figure 3.12 (orange line).

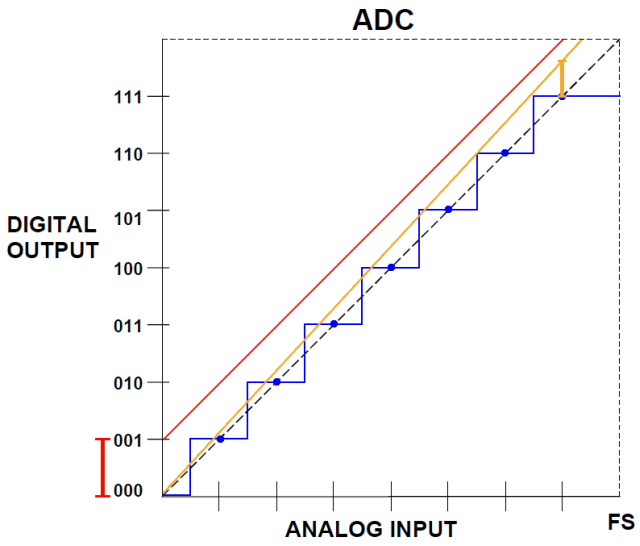


Figure 3.12: Comparison between the transfer function curve (the dashed straight line) of an ideal 3-bit ADC with two transfer function curves affected by offset error (red straight line) and gain error (orange straight line) respectively. The offset and gain errors are highlighted in the plot with two segments.

- The **full scale error** includes both the gain and offset error of an ADC and it can be measured in LSB or Volts.
- The **Differential Non-Linearity** (DNL) is the maximum deviation between a code bin width of the actual transfer function and the ideal code bin width (1 LSB), after correcting for gain errors. The DNL produces quantization code bins with varying widths: a positive DNL implies a code bin width larger than the nominal Least Significant Bit (LSB) value while a negative DNL represents a narrow code bin width. The DNL by definition can be higher than 1 LSB but the lower bound is -1 LSB and when it occurs the consequence is the presence of a missing code. A missing code is a code that can never appear at the output. Therefore an ADC with |DNL| < 1 LSB guarantees no missing codes [81]. An example of DNL effects and of a missing code can be seen in Figure 3.13.
- The **Integral Non-Linearity** (INL) is the maximum vertical deviation between the ideal and actual transition curve, with both the offset and gain error components removed. A positive INL value indicates that the transition curve is above the ideal curve and this is due to at least a code bin with a narrow step. On the contrary, the INL is negative when the actual transition curve is below the ideal curve. The INL as function of k and expressed in percentage of FSR is given by Equation 3.1, where $\epsilon[k]$ is the residual error corresponding to the k^{th} code transition [83]. The ADC INL is the maximum value of the INL*[k]* for all *k*. An example of transition curve affecte by a positive INL is shown in Figure 3.13.

$$\mathrm{INL}[k] = 100\% \times \frac{\epsilon[k]}{FSR} \tag{3.1}$$

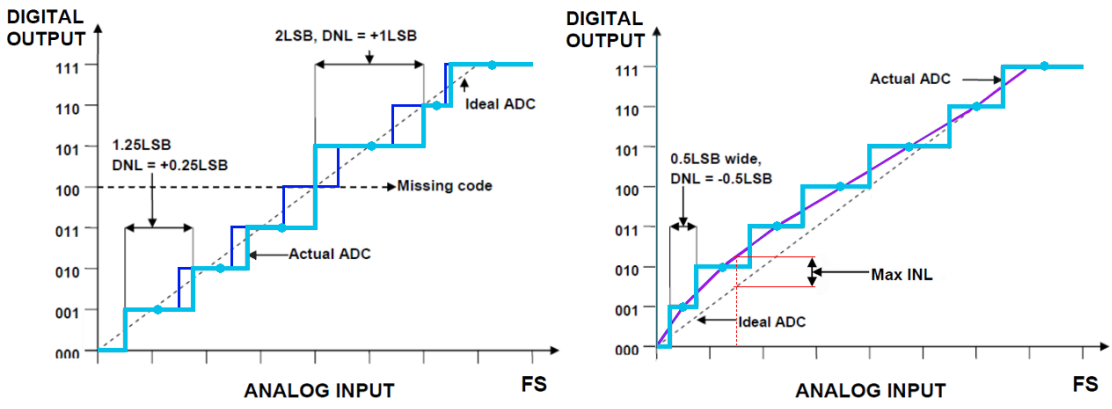


Figure 3.13: Representation of DNL (left) and INL (right) in a non-ideal 3-bit ADC [84]

- An ADC is defined **monotonic non-inverting** when it has output codes that are regularly increasing with increasing input and decreasing with decreasing input stimulus [83].

Dynamic performance

The DC specifications are the most significant requirements when the ADC is employed for applications with steady or low frequency input signals compared to the sampling frequency of the converter. In the other cases, the ADC performance is affected by additional errors. Indeed, ADC defects introduce noise and distortion into the sampled output which are frequency-dependent. Therefore, in addition to the DC specifications, the AC performance features have to be specified such as Signal-to-Noise Ratio (SNR), Signal-to-noise-and-distortion ratio (SINAD), and Effective Number of Bits (ENOB) [83], [82].

- The **SNR** of an ADC is the ratio between the fundamental frequency signal power level (P_{sign}) to the noise power level (P_N) and it is described by Equation 3.2.

$$SNR\,(\text{dB}) \;=\; 10 \cdot \log_{10} \frac{P_{\text{sign}}}{P_{\text{N}}} \tag{3.2}$$

  The maximum theoretical value as function of the ADC resolution N and expressed in dB can be determined applying in input a sine wave with amplitude equal to the FSR. In this case, the P_{sign} is equal to $\frac{Q \cdot 2^{N-1}}{2}$ while the P_N is $\frac{Q^2}{12}$ because it derives only by the quantization error. Therefore, the theoretical SNR is reported in Equation 3.3.

$$SNR\,(\text{dB}) \;=\; 6.02 \;\cdot\; N \;+\; 1.76\,dB \tag{3.3}$$

  A consequence of Equation 3.3 is that every additional bit raises the SNR by 6 dB. Formula 3.3 is valid also for any input signal, apart from the offset value.

- The **SINAD** is the ratio between the fundamental frequency signal power level (P_{sign}) to the noise plus distortion power level (P_{N+D}) and it is described by Equation 3.4.

$$SINAD\,(\text{dB}) \;=\; 10 \cdot \log_{10} \frac{P_{\text{sign}}}{P_{\text{N+D}}} \;=\; SNR \;-\; THD \tag{3.4}$$

  The SINAD is an important specification in order to evaluate the ADC dynamic performance because in addition to the noise it includes also all the distortions

and harmonics. Usually the input for the SINAD measurement is a sine wave, its amplitude and frequency shall be specified because the measure depends on these two parameters [83]. The Total Harmonic Distortion (THD) component is the ratio of the fundamental signal power level to the power of the sum of its harmonics. Generally, the first five harmonics are the bigger contributors to the distortion.

- The **ENOB** is a useful value in order to compare the actual ADC performance to the behavior of an ideal ADC. The ENOB is the number of bits of an ideal ADC which has a SNR equal to the SINAD of the actual ADC. Therefore, the ENOB value (Equation 3.5) is obtained using the theoretical SNR Equation 3.3 by replacing SINAD to SNR and solving it for the ADC resolution.

$$ENOB = \frac{SINAD - 1.76\,dB}{6.02} \tag{3.5}$$

The ENOB should be always related to a range of input frequencies and it reports the converter accuracy as a function of the chosen sampling rate and the frequency of the input signal. If the amplitude of the input sine wave is less than the FSR the Equation 3.5 requires a correction factor in order to take into account the SINAD reduction. The ENOB becomes:

$$ENOB = \frac{SINAD - 1.76\,dB + 20\log\frac{A_{FSR}}{A_{in}}}{6.02} \tag{3.6}$$

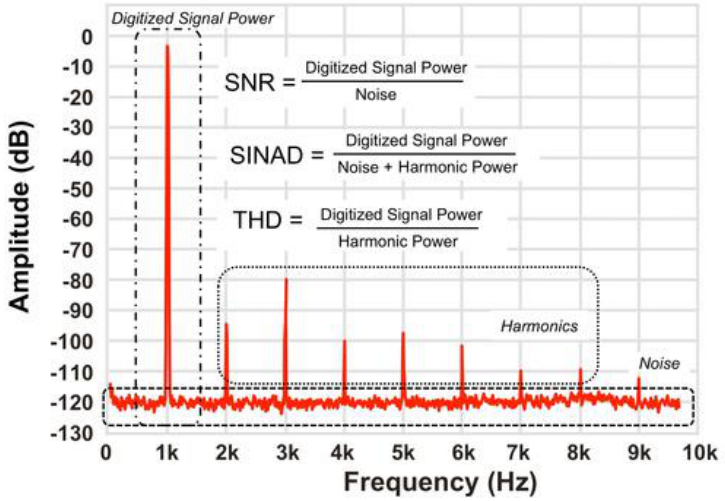
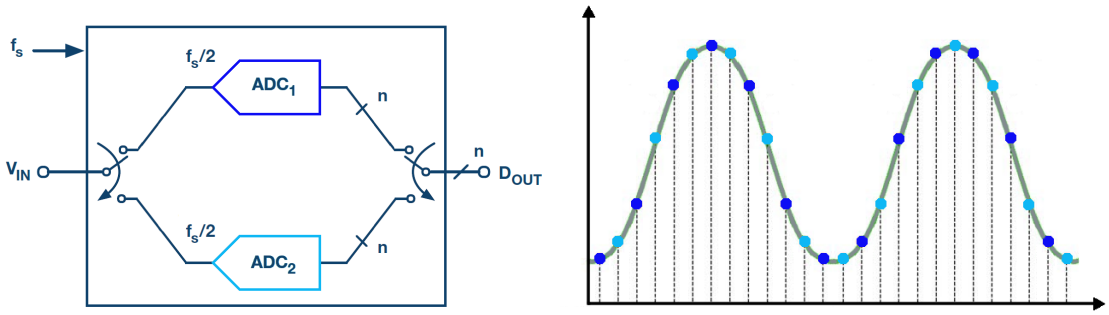


Figure 3.14: Example of a FFT plot along with the SNR, SINAD and THD.

3.5.3 Time-Interleaved ADCs

The adopted ADC IP block includes two interleaving ADCs. The time interleaving technique is implemented to obtain a digitization process at an higher rate than the sampling rate of each individual ADC core [86]. In this particular case the final sampling and conversion rate is 160 MS/s while the two cores work at the lower rate of 80 MS/s. In Figure 3.15a a block diagram of the ADC IP block is shown in which f_S = 160 MHz is the sampling frequency and n = 12 is the number of bits for the two identical ADCs. The sampling of the analog signal V_{IN} is performed by ADC_1 and ADC_2 in a periodic alternation with a delay of $T_S = 1/f_S = 6.25$ ns as shown in Figure 3.15b. The 12-bit digital output, D_{OUT}, is reassembled from the time interleaved ADC in the right order as it has been sampled.



(a) (b)

Figure 3.15: Two-way interleaved ADC on the left and the sampled signal on the right.

This effective technique is commonly employed in order to obtain an ADC with defined requirements such as sample rate, number of bits, and linearity, and there are no ready-made ADC. Moreover the time-interleaved method can be applied in all ADC topologies. However the time interleaved approach is not free of functional challenges [86]. Actually, even with completely linear components, some unwanted spurious frequency can appear in the output spectrum. These frequencies are called interleaved (IL) spurs, and can appear due to timing errors and offset/gain mismatches. The SNR of the converter is affected by the presence of these errors related to the time-interleaving [87], [88].

In a two-way interleaved ADC, if ADC_1 and ADC_2 have different gains, G_1 and G_2 respectively, the even and odd digital output will have different amplitude set by the ADCs gain. Providing a sinusoidal input at frequency f_{IN}, the output frequency spectrum will contain a gain spur at $f_{gain} = f_S/2 \pm f_{IN}$, as shown in Figure 3.16.
The gain spurs magnitude relies on the gain error mismatch, therefore the V_{FS1} and

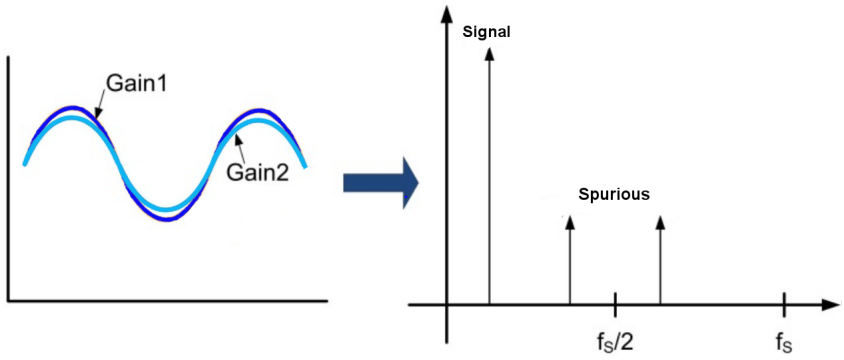


Figure 3.16: IL spurious tone due to gain mismatch between two interleaved converters.

V_{FS2}, that are the full scale peak-to-peak voltages of ADC_1 and ADC_2 [89]:

$$IL_{gain}\,(dBc) \;=\; 20 \times \log_{10}\left(\frac{1 - \frac{V_{FS1}}{V_{FS2}}}{2}\right) \tag{3.7}$$

A clock skew between the two channels or a mismatch in the group delays in the analog section of the ADCs results in timing spurs. Timing spurious tone has the same spectral location of the gain spurs with a magnitude that depends on f_{IN} and the timing mismatch $\Delta\tau$ [89]:

$$IL_{timing}\,(dBc) \;=\; 20 \times \log_{10}\left(\frac{f_{IN}\,\Delta\tau}{2}\right) \tag{3.8}$$

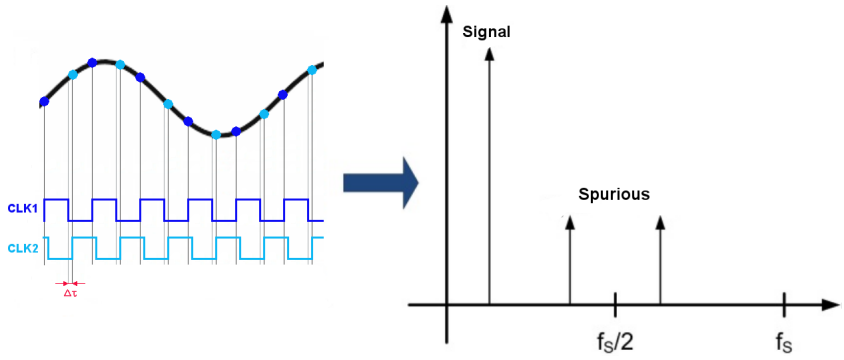


Figure 3.17: IL spurious tone due to timing skew between the two channels of the interleaved ADC. In this case the CLK_2 has a skew and causes an error on the sampled data.

Another cause of IL spurs is the offset mismatch: a difference between the interleaved ADCs DC offset value introduces the spurs, as shown in Figure 3.18. The first component in the output spectrum is at dc while the spurious tone is at the fixed frequency $f_{offset} = f_S / 2$ and with a magnitude proportional to the offset mismatch itself [89]. In order to observe the offset mismatch spurious tone, the application of an input signal is not necessary because this IL spurs is the result of the switch between the static DC offset of each ADC at a rate of $f_S/2$.

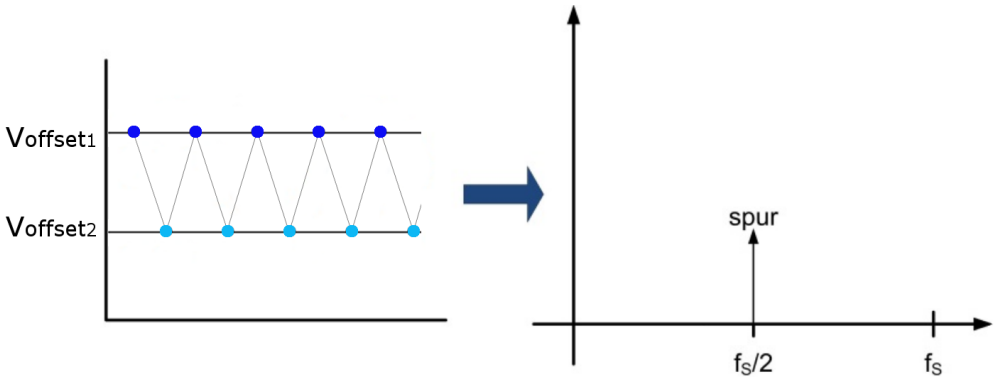


Figure 3.18: IL spurious tone due to offset mismatch of the two channels of the interleaved ADC. The output switches between $V_{offset1}$ and $V_{offset2}$ at a rate of $f_S/2$.

$$IL_{offset}\,(\text{dBFS}) = 20 \times \log_{10}\left(\Delta_{offset} \times \frac{2}{2^{res}}\right) \tag{3.9}$$

Therefore the output spectral degradation, due to IL spurs, only depend on the relative discrepancies between gain, timing and offset of the two channels of the interleaved ADC. The technique adopted in order to reduce the spurious tones due to the offset and gain mismatches is based on the selection of one ADC as a reference. The calibration method has to match as well as possible both the offset and the gain values. During the calibration phase, the ADC sample conversion is disabled and the ADC needs a reference signal in order to detect and fix the gain mismatch. Lastly, in order to reduce the timing mismatch causes, the phase relationship between the two ADC input clocks need to be strictly controlled to be as close as possible to 180°.

In Section 4.2.2, the obtained data from test done in laboratory show the observed (IL) spurs of the ADC IP block embedded in the LiTE-DTU.

3.6 ADC Test Unit

The ADC Test Unit (ATU) has been embedded in the LiTE-DTU in order to facilitate the acquisition of the samples digitized by the ADCs for testing purpose. The idea is to serialize directly the output samples of the two ADCs over 4 different serial links and transmit them in parallel at 1.28 Gb/s. For the ADCs sample transmission, in contrast to the DTU condition explained in the next sections, there is no need for data compression: for this reason, on each output link, a sample word of 32 bits is serialized in 25 ns.

A 32-bit word contains two 12-bit samples labeled and prefixed by 4-bit each. These 4-bit blocks are helpful for the ordering of the samples and for the word detection and alignment performed by the DAQ system. The samples coming from ADC_H are transmitted to the output: dout_0 and dout_1, while the ADC_L utilizes the remaining output: dout_2 and dout_3.

In Figure 3.19 a scheme of the ATU module is represented. It works with the CLK_{160} and contains a FSM which manages the sample word generation and the packet transmission to the serializers. The TMR method has been applied on the entire ATU block so the 4 32-bit sample words are the resulting packet of the voting operation.

The ADC samples format in the 32-bit sample word for ADC_H and ADC_L are reported in Figure 3.20 and Figure 3.21, respectively. From the pictures it is possible to notice that the even and odd samples of the same ADC are contained in different sample words and this is another useful feature for testing purposes. Indeed, as was discussed in Section 3.5.3, the integrated ADC IP block includes a two-way time-interleaved ADC. Therefore the even and odd samples, which belong to ADC_H_1 and ADC_H_2 or ADC_L_1 and ADC_L_2, can be easily separated with the aim to test and compare the performances of the interleaved ADCs.

The ATU unit is activated by the high logic level of the ADC Test Mode (ATM) test signal (in Figure 3.2b it is the bottom pin on the left side of the LiTE-DTU pinout), which disables most of the DTU operations but it keeps the four serializers active. In this test configuration, when there is a LiTE-DTU reset (it involves both the ATU unit and the DTU module), or at least one ADC in reset or in calibration the 32-bit words sent from the ATU to the serializers are a defined Test Mode idle pattern (TM_idle pattern): **0x5A5A5A5A** (in binary: **01011010010110100101101001011010**).

The TM_idle pattern transmission can be seen in Figure 3.22 when the DTU reset is active (the signal is highlighted in blue, as mentioned before the reset is active low) or in Figure 3.23 when the CALIBRATION_BUSY signal has an high logic value (again, the signal is highlighted in blue). In both figures, the ATU sample words and the seriaizers output are respectively:

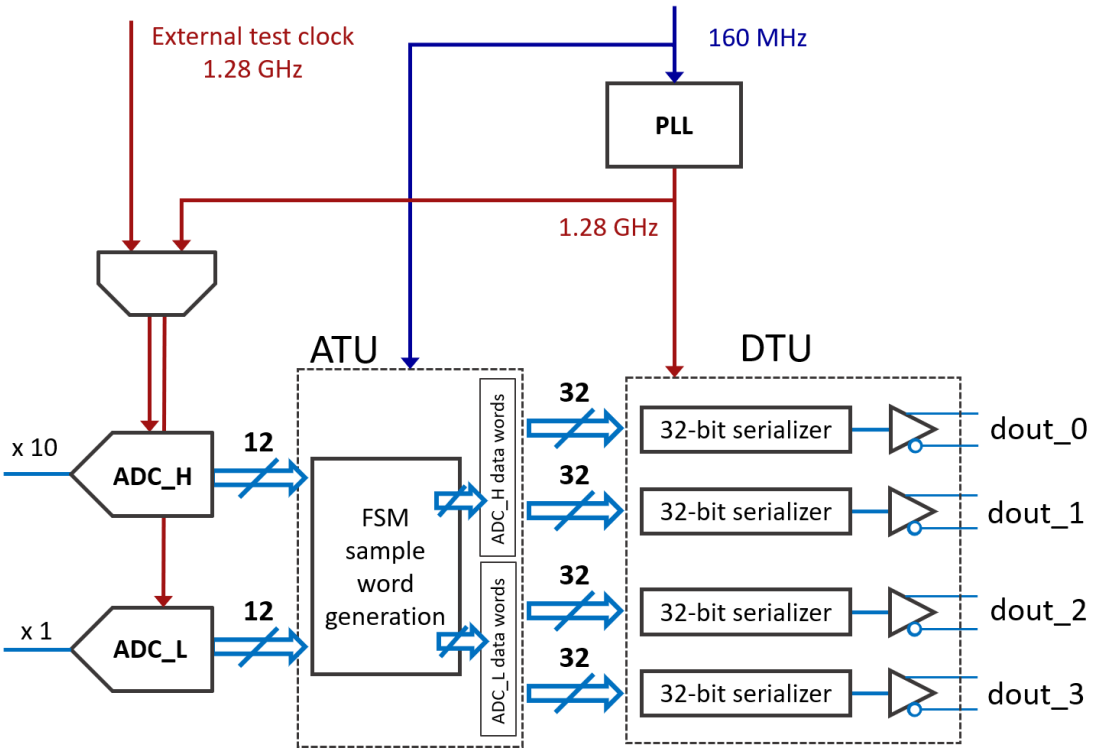


Figure 3.19: Schematic of the ADC test unit.

		Bit range				
		[31 : 28]	[27 : 16]	[15 : 12]	[11 : 0]	output
ADC_H	odd sample word	0011 (**0x3**)	ADC_H (i+3)	1001 (**0x9**)	ADC_H (i+1)	dout_0
	even sample word	0110 (**0x6**)	ADC_H (i+2)	1100 (**0xC**)	ADC_H (i)	dout_1

Figure 3.20: Output scheme of the ATU for the ADC_H samples. In yellow are highlighted the 4-bit labels and the temporal order of the samples for the ADC_H is characterized by the label sequence: 0xC - 0x9 - 0x6 - 0x3.

- ADC_H odd sample word: DATA_ADC_TEST_UNIT_0 → BIT_OUT_0;
- ADC_H even sample word: DATA_ADC_TEST_UNIT_1 → BIT_OUT_1;
- ADC_L odd sample word: DATA_ADC_TEST_UNIT_2 → BIT_OUT_2;
- ADC_L even sample word: DATA_ADC_TEST_UNIT_3 → BIT_OUT_3.

On the other hand, when the ATU is active and there are no reset or calibration signals, the sample words are continuously transmitted through the four digital output as shown in Figure 3.22 and Figure 3.23.

		Bit range				
		[31 : 28]	[27 : 16]	[15 : 12]	[11 : 0]	output
ADC_L	odd sample word	1100 (**0xC**)	ADC_L (i+3)	0110 (**0x6**)	ADC_L (i+1)	dout_2
	even sample word	1001 (**0x9**)	ADC_L (i+2)	0011 (**0x3**)	ADC_L (i)	dout_3

Figure 3.21: Output scheme of the ATU for the ADC_L samples. In yellow are highlighted the 4-bit labels and the temporal order of the samples for the ADC_L is characterized by the label sequence: 0x3 - 0x6 - 0x9 - 0xC.

In Figure 3.22), during the reset condition, the four outputs are always at the low logic level because the read pointer of the serializers are forced to remain fixed to their initial value under the effect of the reset condition. As described in Section 3.7.6, the serial transmission is performed following the big-endian order, which means that the first bit transmitted is the MSB. Therefore, in this particular case, during the reset condition, the serialization outputs are always 0. On the contrary, when the rising edge of the reset occurs the serializers start to transmit the TM_idle pattern, the sample word serialization will start only when the packets arrive and the previous word has been completely sent out.

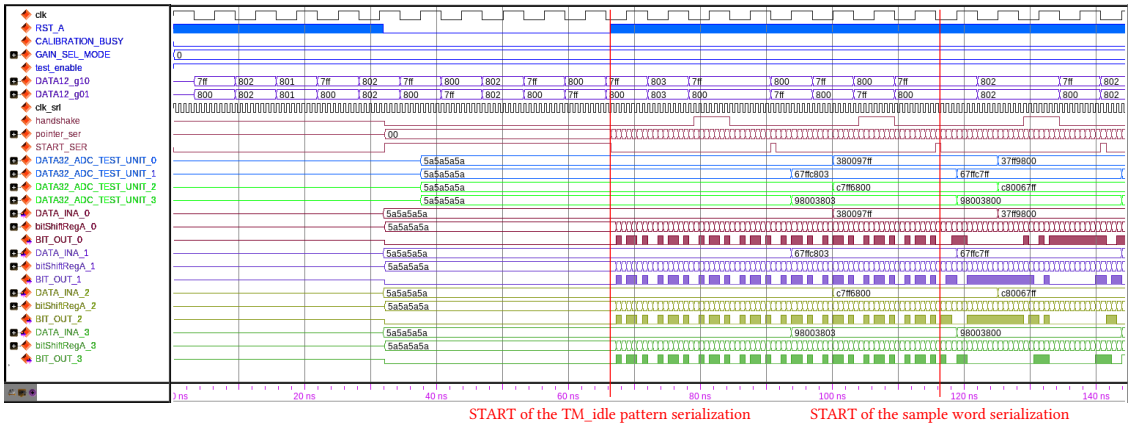


Figure 3.22: Simulation of the behavior of the ATU module during and after a reset of the system.

In Figure 3.23, when at least one of the ADCs is performing a calibration the ATU starts to send to the serializers the TM_idle pattern. At the end of the calibration, the ATU restarts to transmit the sample words and the serializers act accordingly. From the point of view of the DAQ system, after the 32-bit word detection based on the four 4-bit blocks, a reorder of the samples is needed. An example of these two phases is shown in

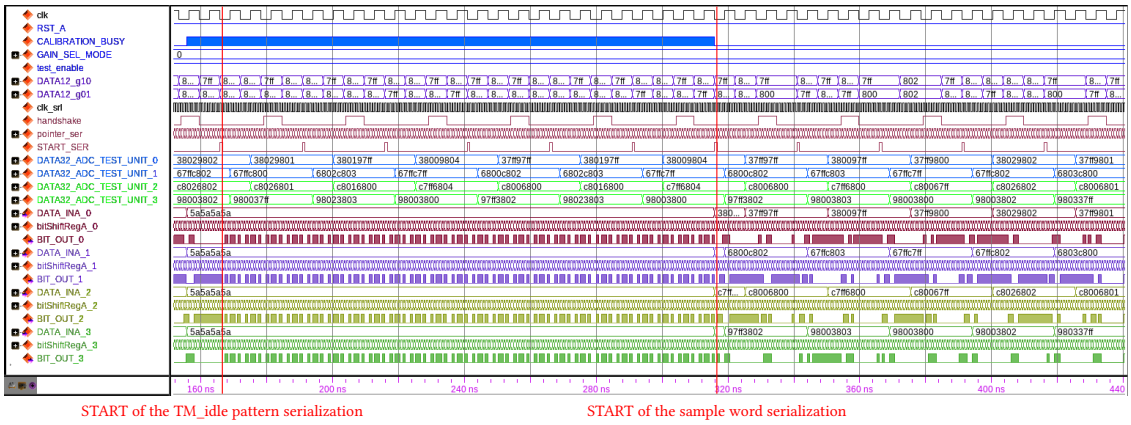


Figure 3.23: Simulation of the behavior of the ATU module during and after the ADCs calibration.

the Figure 3.24.

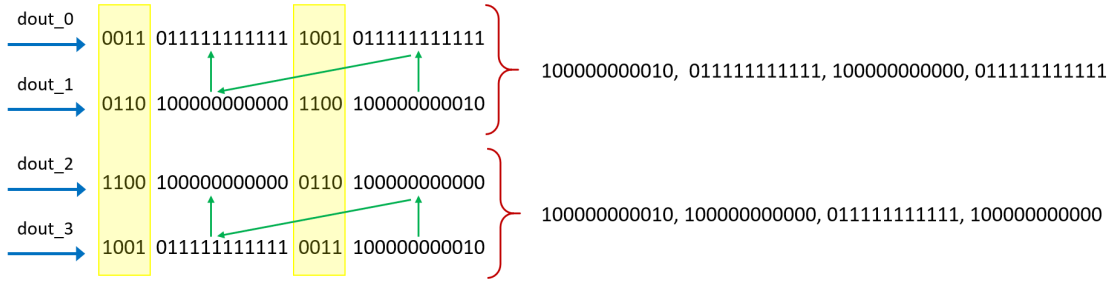


Figure 3.24: Detection of the sample words transmitted through 4 output at 1.28 Gb/s (left) and reordering of the ADC samples (right). The transmitted samples are around the mid value of the dynamic range, indeed these are the typical values obtained after the ADC calibration.

3.7 Data Transmission Unit

The Data Transmission Unit (DTU) performs the gain selection, an online lossless compression in order to reduce the necessary bandwidth for the data transmission, and lastly the high-speed serialization of the packets. In Figure 3.25 a scheme of the DTU block and all the connection between it and the ADCs, PLL, and ATU is represented.

The DTU block works mainly with the CLK_{160} but receives also the $CLK_{1.28}$ for the serializers. DTU contains several modules; all of them have been protected in order to obtain a robust design against radiation-induced upsets. Moreover, the Hamming

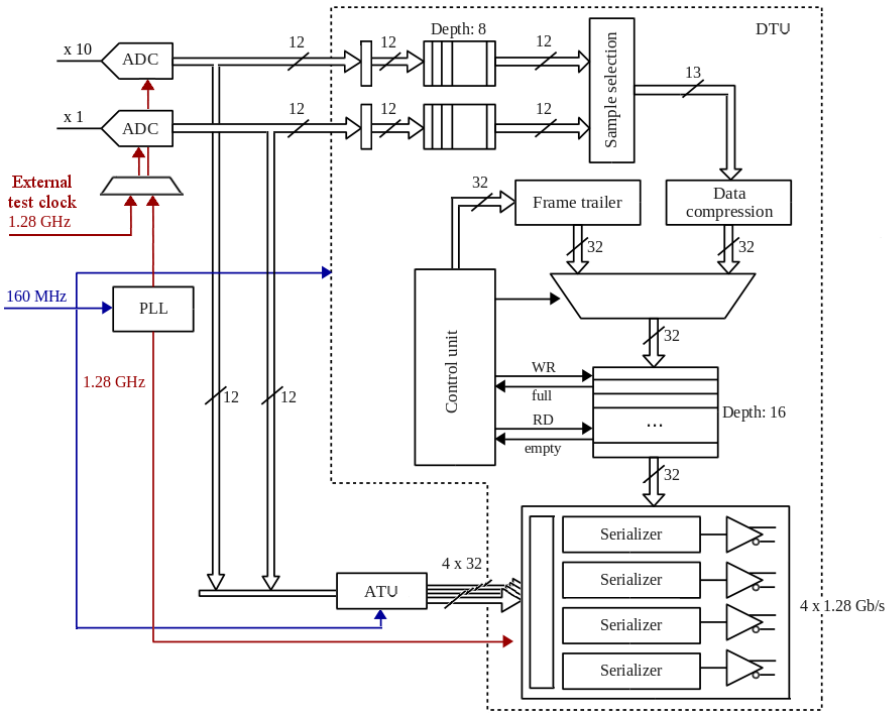


Figure 3.25: Schematic of the DTU connected to the ADCs and the ATU.

encoding and decoding has been used in the compensation memory with the purpose of increasing the data protection.

The DTU unit is activated by the low logic level of the ATM test signal (the bottom pin on the left side of the LiTE-DTU pinout, see Figure 3.2b) which disables the ATU operations. This configuration is the operational mode of the LiTE-DTU ASIC; the serial output transmission in uniquely performed on the dout_0 while on the other three output the TM_idle pattern (0x5A5A5A5A) is continuously transmitted.

The Operational Mode idle pattern (OM_idle pattern) is a 32-bit word defined as: **0xEAAAAAAA** (in binary: **11101010101010101010101010101010**). This packet is transmitted when there is a LiTE-DTU reset or at least one ADC in calibration or when the LiTE-DTU is actively performing operations and the data packet rate decreases due to the compression process. The former implies an empty condition of the compensation memory (more details in Section 3.7.6).

The first two possible transmissions of the OM_idle pattern can be seen in Figure 3.26 after the reset of the LiTE-DTU (the signal is highlighted in blue, as mentioned before the reset is active low) or in Figure 3.27 when the CALIBRATION_BUSY signal has an high logic value (again, the signal is highlighted in blue).

In Figure 3.26, during the reset condition the serializer connected to the dout_0

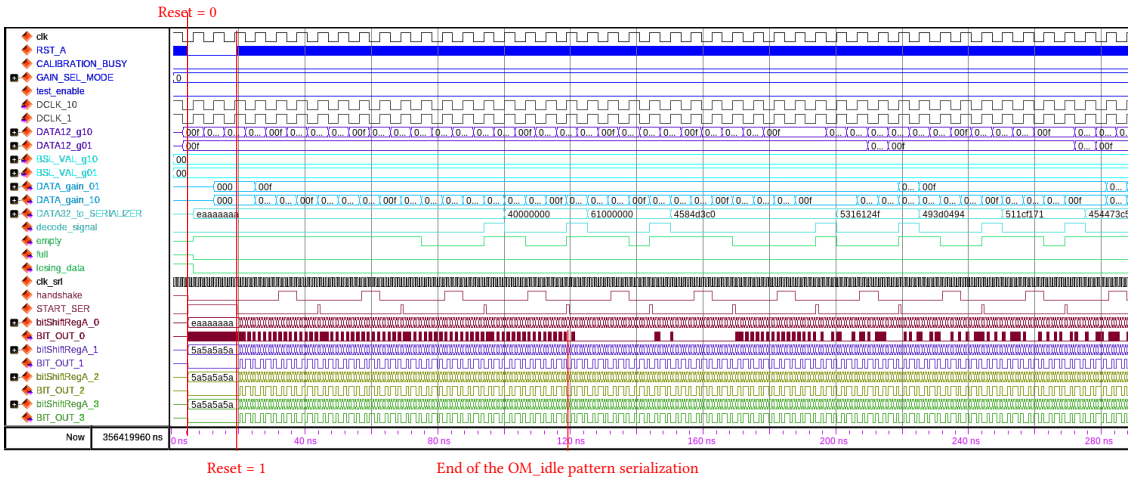


Figure 3.26: Simulation of the behavior of the DTU architecture during and after the reset of the system.

output transmits the high logic level while the other outputs are at the low logic level. As previously explained in the ATU Section 3.6, the read pointer of the serializers are forced to their initial value under the effect of the reset condition. The dout_0 level is different from the other output because the MSB of the OM_idle pattern is 1 while the MSB of the TM_idle pattern is 0. On the other hand, when the rising edge of the reset occurs, the first serializer starts to transmit the OM_idle pattern bits at 1.28 Gb/s. The data word serialization starts only when the compressed packets are complete and sent from the compression unit to the compensation memory, as described in Section 3.7.5, and when the serialization of the OM_idle pattern is concluded.

In Figure 3.27 it is possible to see that, when at least one of the ADCs is performing a calibration, the first serializer starts to send out the OM_idle pattern. At the end of the calibration, the DTU restarts all its operations, so only when the first data word is stored in the compensation memory the data packet transmission restarts too.

3.7.1 Baseline subtraction unit

The DTU first stage is a baseline subtraction unit and it is directly connected to the two output of the ADCs which sample and digitize the analog signals coming from the CATIA transimpedance amplifier. The two 12-bit output correspond to two different gains of the same input signal (x 10 and x 1). They are transmitted to the DTU at each falling edge of a 160 MHz clock generated internally in the ADCs block and it is referred to the $CLK_{1.28}$. The baseline subtraction block embeds two 8-bit registers, controlled via I^2C, which allows the samples to be captured at the rising edge of the CLK_{160} and then

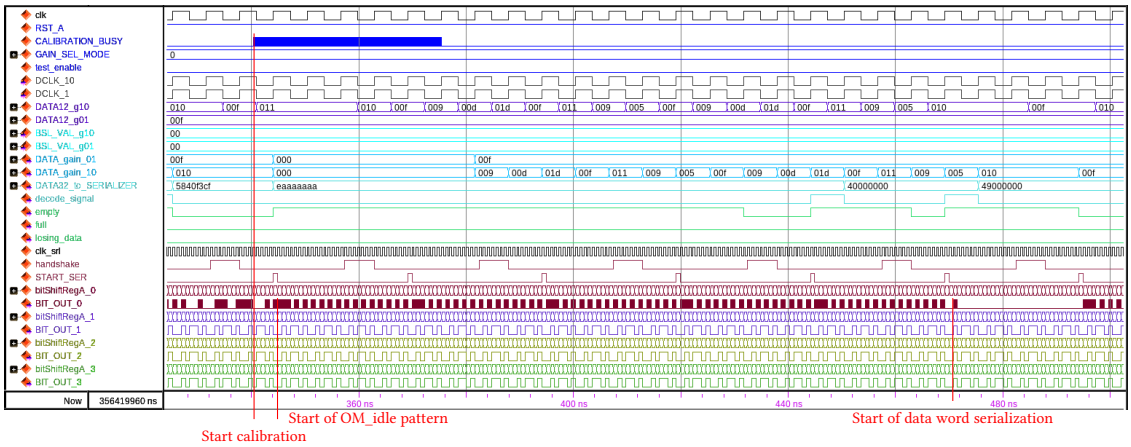


Figure 3.27: Simulation of the behavior of the DTU architecture during and after the ADCs calibration.

subtract baseline values from the 12-bit samples.

3.7.2 Gain channel selection unit

The baseline subtraction unit is followed by a module used for the selection of the gain channel. As shown in Figure 3.28, the unit inputs are the CLK_{160}, the reset signal, the samples received by the baseline subtraction unit, i.e. two 12-bit words, and a 2-bit word controlled via I^2C, the GAIN_SEL_MODE, which sets the operation mode of the unit. The output is a 13-bit signal, made up by the selected 12-bit sample combined to a bit label to specifies the gain channel, a 1-bit signal flag, which tag the type of the output data, and lastly the TMR error signal.

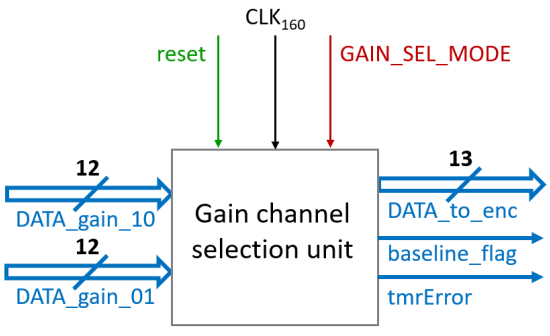


Figure 3.28: Schematic of the gain channel selection unit of the DTU.

The gain channel selection unit has three different operation modes that can be

chosen through the GAIN_SEL_MODE signal:

- GAIN_SEL_MODE == 2'b11: selection of the gain x1 samples
- GAIN_SEL_MODE == 2'b10: selection of the gain x10 samples
- GAIN_SEL_MODE[1] == 1'b0: activation of the look-ahead algorithm for the sample selection

The first two options have been implemented for debug purposes while the third one is the operational mode of the gain channel selection unit for the LiTE-DTU. The simulated behavior of the unit when the look-ahead algorithm is disabled is shown in Figure 3.29 and in Figure 3.30. During these two modes, the signal output sent to the compression unit are:

- a stream of 13-bit samples:
  - gain label bit: **1** + 12-bit sample from gain x1 channel Figure 3.29
  - gain label bit: **0** + 12-bit sample from gain x10 channel Figure 3.30
- baseline_flag signal always at low logic level

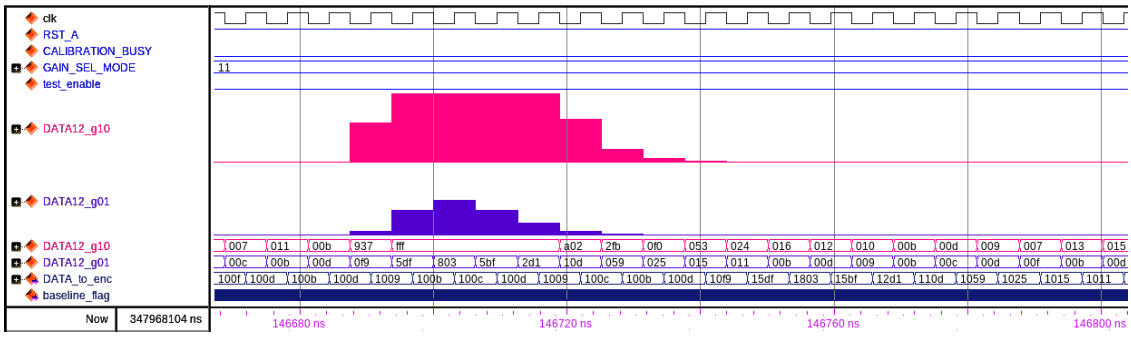


Figure 3.29: Simulation of the behavior of the gain channel selection unit of the DTU when GAIN_SEL_MODE == 2'b11. The magenta signal is the gain x10 sample stream while the dark slate blue signal is the gain x1 sample stream. The selected samples are the ones from gain x1 channel and the baseline_flag (dark blue signal) has always a high logic value.

When the selection of the gain channel is based on the look-ahead algorithm, the selection module employs two FIFOs, with a depth of 8, which are fed with gain x10 and gain x1 samples, respectively.

A scheme of the two FIFOs is shown in Figure 3.31a. As illustrated the FIFO related to the gain x10 channel has an additional pointer with respect to the gain x1 FIFO. The

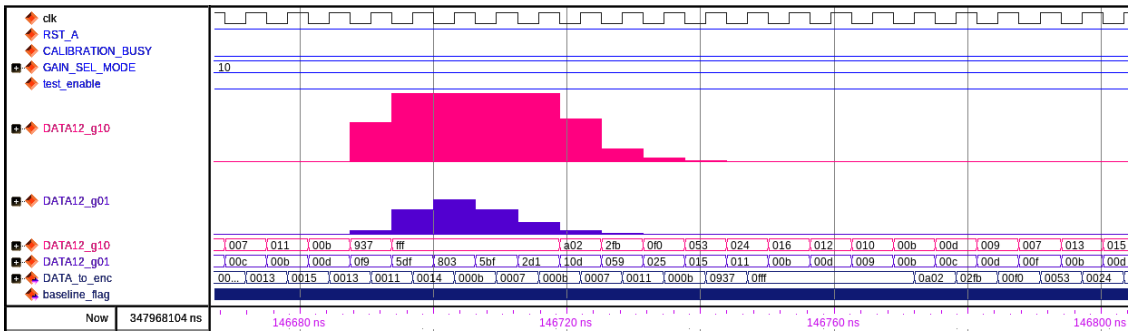


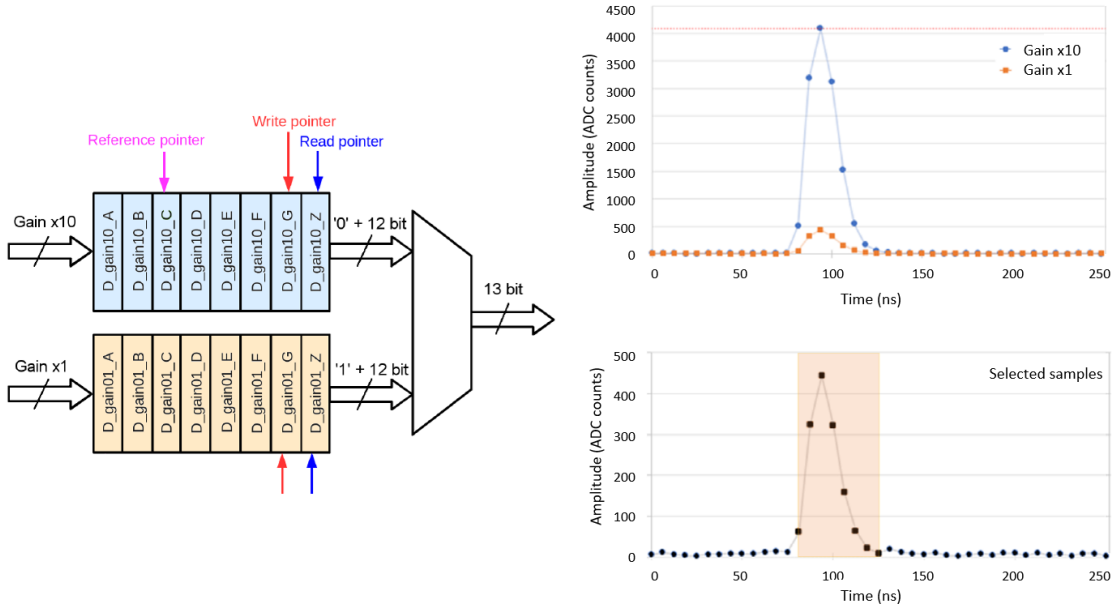
Figure 3.30: Simulation of the behavior of the gain channel selection unit of the DTU when GAIN_SEL_MODE == 2'b10. The magenta signal is the gain x10 sample stream while the dark slate blue signal is the gain x1 sample stream. The selected samples are the ones from gain x10 channel and the baseline_flag (dark blue signal) has always a high logic value.

extra pointer is a reference indicator, it is employed with the aim of checking the sample value and it is constantly separated from the read pointer by three units. If the sample in reference position is saturated (i.e. value = x0FFF), the look-ahead algorithm opens a time window around that sample and during this interval only gain x1 samples are processed. The duration of the window increases as long as there are saturated samples. Otherwise, if saturation does not take place, only samples from gain x10 are selected. In both cases an additional bit is added to the 12-bits data as a gain indicator: gain x10 samples are labeled with 1'b**0** and gain x1 samples with 1'b**1**.

The design of the selection mechanism, the position of the time window with respect to the saturated sample and the FIFOs depths are based on the duration and the shape of the APD signal. The signal lasts about 40-50 ns, thus 7-8 samples will be extracted per event (Figure 2.9a and Figure 2.9b). The saturation check performed with the look-ahead algorithm is done in order to prevent the mixing of samples from different gains in the same APD signal. Moreover, if a saturation occurs the gain will always switch in correspondence of two samples before the start of the saturation (from gain x10 to gain x1) and five samples after the end of the saturation (from gain x1 to gain x10).

In Figure 3.31b, in the top plot the two stream of samples are represented, where the dotted horizontal red line is the reference for the channel saturation, while in the bottom plot there are the samples selected by the look-ahead algorithm and the time-window for the gain x1 sample transmission.

The simulated behavior of the gain channel selection unit for the LiTE-DTU is shown in Figure 3.32, in Figure 3.33, and in Figure 3.34. In Figure 3.32 two signals are shown, the first one saturates and activates the selection of the gain x1 samples, while the second one does not saturate. Therefore, the output of the gain channel selection



(a) (b)

Figure 3.31: Representation of the two FIFOs embedded in the gain channel selection unit (left) and example of the sample selection system when a sample of gain x10 channel is saturated (right).

unit is composed only by gain x10 samples. The baseline_flag output (the dark blue signal) is a reference for the compression method which is applied by the successive block (Section 3.7.3). Baseline_flag signal has a high logic value when the sample (valid only for gain x10 samples) is lower than 0x40 (in binary: **000001000000**). In the remaining cases the baseline_flag signal has a low logic value. In the same figure (3.32) there are two signals and the corresponding duration of the low value of the baseline_flag is different: in fact the first one is longer than the second one. This is due to the saturation of the first signal, which activates the time window of the look-ahead algorithm and the number of gain x1 samples transmitted increases with respect to the number of the saturated samples in the gain x10 stream.

Figure 3.33 shows a zoom-in of the first and higher peak represented in Figure 3.32. From this simulation, the selection of the samples between gain x10 and gain x1 channels can be noticed. Moreover the delay due to the FIFOs (Figure 3.31) embedded in the gain channel selection unit is easily visible. In Figure 3.34 a zoom-in of the second peak represented in Figure 3.32 is shown. This simulation displays that the selected samples

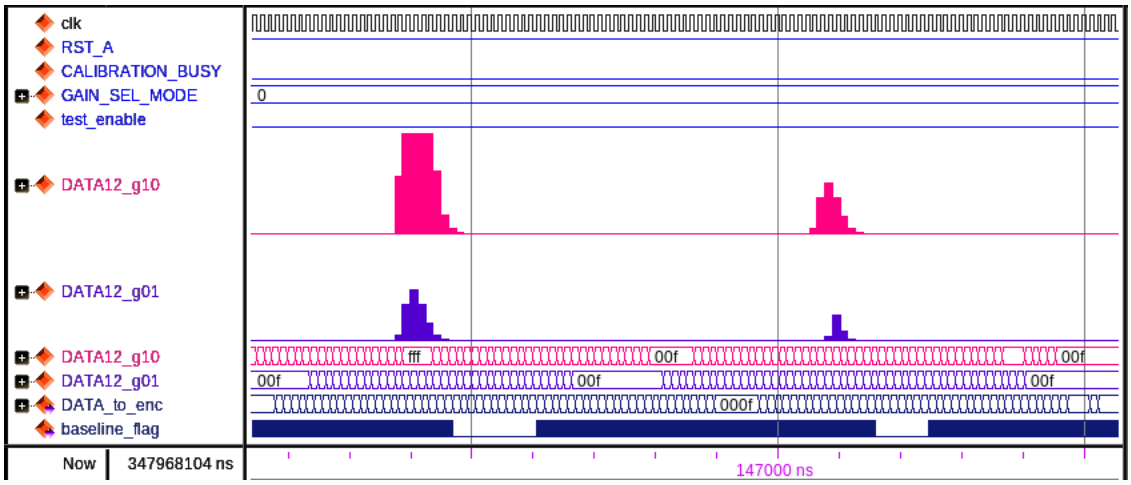


Figure 3.32: Simulation of the behavior of the gain channel selection unit of the DTU when GAIN_SEL_MODE[1] == 1'b0. The magenta signal is the gain x10 sample stream, the dark slate blue signal is the gain x1 sample stream, and the baseline_flag is in dark blue.

result uniquely form gain x10 channel and the period with a low value of the baseline_flag lasts exactly the number of clock periods during which the gain x10 samples have a value higher than 0x3F (7 samples).

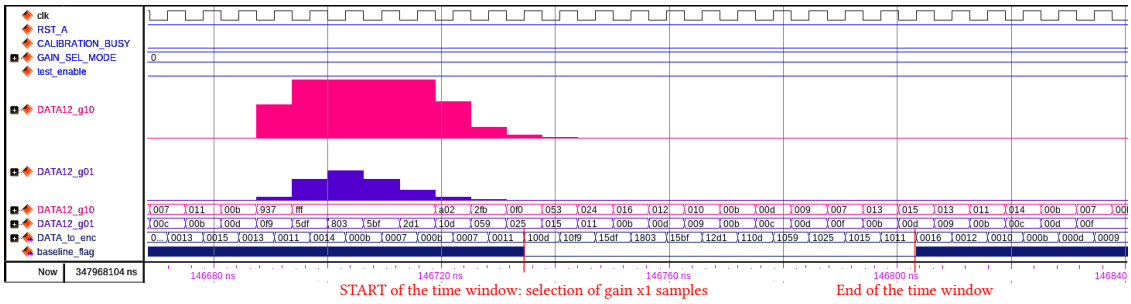


Figure 3.33: Zoom-in of the first peak represented in Figure 3.32

3.7.3 Data compression and data word generation unit

One of the requirements of the LiTE-DTU ASIC is to transfer every single ADC sample to the off-detector electronics. Thus a large amount of data needs to be transferred via LpGBT links from the FE to the BCP. A unit for a lossless compression of the data samples has been embedded in the LiTE-DTU.

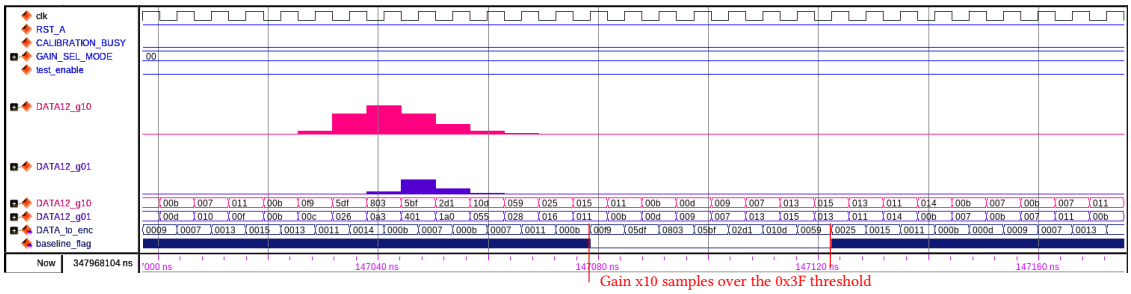


Figure 3.34: Zoom-in of the second peak represented in Figure 3.32

This unit follows the gain channel selection module and it performs a data compression and the generation of the data words. As shown in Figure 3.35, the unit inputs are the CLK_{160}, the reset signal, the 13-bit received by the preceding module, and the baseline_flag signal. The outputs are a 32-bit signal, which contains the samples, a 1-bit signal to notify that the 32-bit data word is complete, and lastly the TMR block signal.

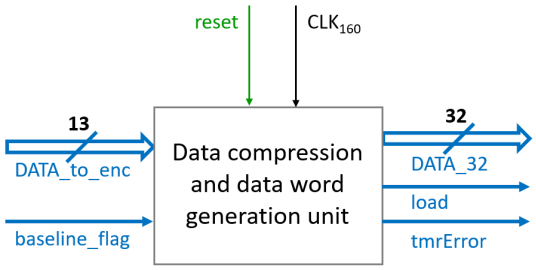


Figure 3.35: Schematic of the Data compression and data word generation unit of the DTU.

As explained in the previous section, each LiTE-DTU ASIC provides 13 bits of information per 160 MHz clock cycle, generating 2.08 Gb/s data flow per channel corresponding to: 10.4 Gb/s per VFE card (5 channels) and thus 52 Gb/s per FE card (5×5 channels). In order to transmit 52 Gb/s, at least 6 LpGBT chips are required, because each LpGBT has 7 e-links running at 1.28 Gb/s, therefore the maximum data rate per LpGBT chip is 8.96 Gb/s.

A lossless compression algorithm has been implemented in order to compress the LiTE-DTU data. With such a feature a FE card can be connected to 4 LpGBT ASICs. This allows to reduce the number of LpGBT chips, scaling the rate to 1.024 Gb/s per channel, 5.12 Gb/s per VFE card, and 25.6 Gb/s per FE card, respectively.

The lossless compression algorithm is based on the Huffman coding [90] and it takes into account the statistical distribution of the LiTE-DTU input values. This compression

code is based on the probability of occurrence of the input values and assigns a variable length code to each input symbol inversely proportional to the symbol probability. However, a variable length code is difficult to manage, especially if transmission errors can occur. In fact, the e-links between VFE boards and FE cards don't implement an encoding or error protection (Section 2.3.3). Taking into account the probability of transmission error on the e-link, the modest required compression rate (~ 0.6) and with the performed simulation studies [91], a simplified Huffman coding has been adopted. The simulations (see Section 3.7.7) show that the probability of an event with more than 6 significant (non-zero) bits (> 0x3F), for a single crystal and in HL-LHC conditions, is lower than $5.8 \cdot 10^{-4}$ ($P_{>\ 6\text{-bit}}$) at the highest possible pseudorapidity in the ECAL barrel. Therefore the straightforward coding is based on just two code lengths: 6-bit and 13-bit, it is shown in Table 3.3.

Gain channel	Significant non-zero bits	Sample Classification[a]	Output (number of bits)
x10	$\leq$ 6 bits	"Baseline" sample	6 bits
x10	$>$ 6 bits	"Signal" sample	13 bits (MSB = 0)
x1	any value	"Signal" sample	13 bits (MSB = 1)

[a]Note that the terms "baseline" sample and "signal" sample are used to identify samples that fit or not fit in a 6 bits word and do not necessary refer to the presence or absence of a detector signal.

Table 3.3: Applied compression scheme in LiTE-DTU ASIC.

The chosen coding is based on 32-bit data word, each packet can accommodate up to five 6-bits consecutive samples ("baseline" packet) or up to two 13-bits samples ("signal" packet). Both "baseline" and "signal" packets have an alternative version: indeed the data word can remain incomplete if is not possible to fill the 32-bit word with consecutive samples of the same type. The baseline_signal flag coming from the channel gain selection unit is the indicator of the sample category, so it is an input of the FSM, made of 8 states which describes the data packet generation, as reported in Figure 3.36. The baseline_flag rising edge determines a transition from the "signal" packet to the "baseline" packet, while when there is a falling edge of the baseline_flag the changeover is the opposite one. In Figure 3.36 the former is characterized by the orange arrows while the latter by light blue arrows. When the baseline_flag has a stable value, the consecutive samples are of the same type. In Figure 3.36 these cases are represented in red, for baseline_flag = 1'b1, and in blue for baseline_flag = 1'b0.

The possible 32-bit data packets are:

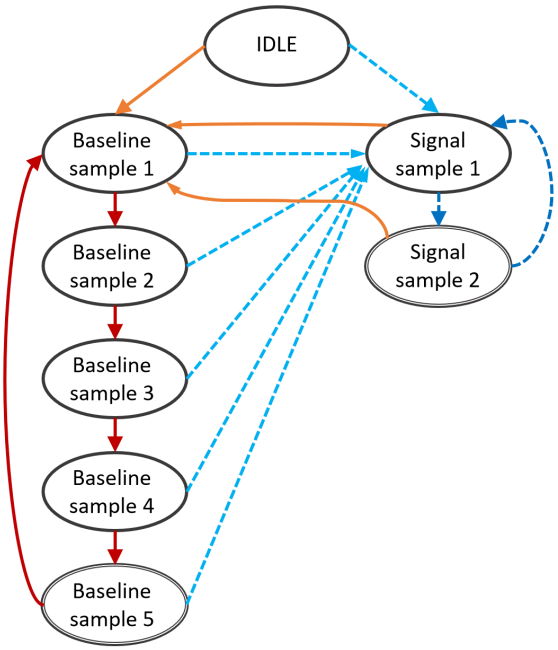


Figure 3.36: State chart of the data encoding FSM. The 32-bit packet is completed when the current state of the FSM is the Baseline sample 5 or the Signal sample2.

- **Signal packet**: it is composed by 2 consecutive "signal" samples. The packet consists of the **001010** header followed by the 2 13-bit samples.
- **Signal incomplete packet**: it contains only one "signal" sample and it occurs when there is a baseline_flag transition from 0 to 1. The packet consists of the **001011** header followed by the **0101010101010** pattern, and by the 13-bit sample.
- **Baseline packet**: it contains 5 consecutive "baseline" samples. The packet consists of the **01** header followed by five 6-bit samples.
- **Baseline incomplete packet**: it contains less than 5 consecutive "baseline" samples (from 1 to 4) and it occurs when there is a baseline_flag transition from 1 to 0. The packet consists of the **10** header followed by 6-bit for the number of samples in the packet (sample map), and by 4 packet slots, that can be filled with the samples or by all zeros depending on the sample map.

In every case, the rightmost sample is the earliest in time and the leftmost is the latest. In Figure 3.37 the four data packets are wrapped up while the mapping of 32-bits words is depicted in Figure 3.38.

Signal	001010	13 bits sample	13 bits sample		
Signal incomplete	001011	0 1 0 1 0 1 0 1 0 1 0 1 0	13 bits sample		
Baseline	01	6 bits sample	6 bits sample	6 bits sample	6 bits sample	6 bits sample
Baseline incomplete	10	# Sample map	00 / 6 bits sample	00 / 6 bits sample	00 / 6 bits sample	6 bits sample

Figure 3.37: Data format used for the simplified Huffman encoding.

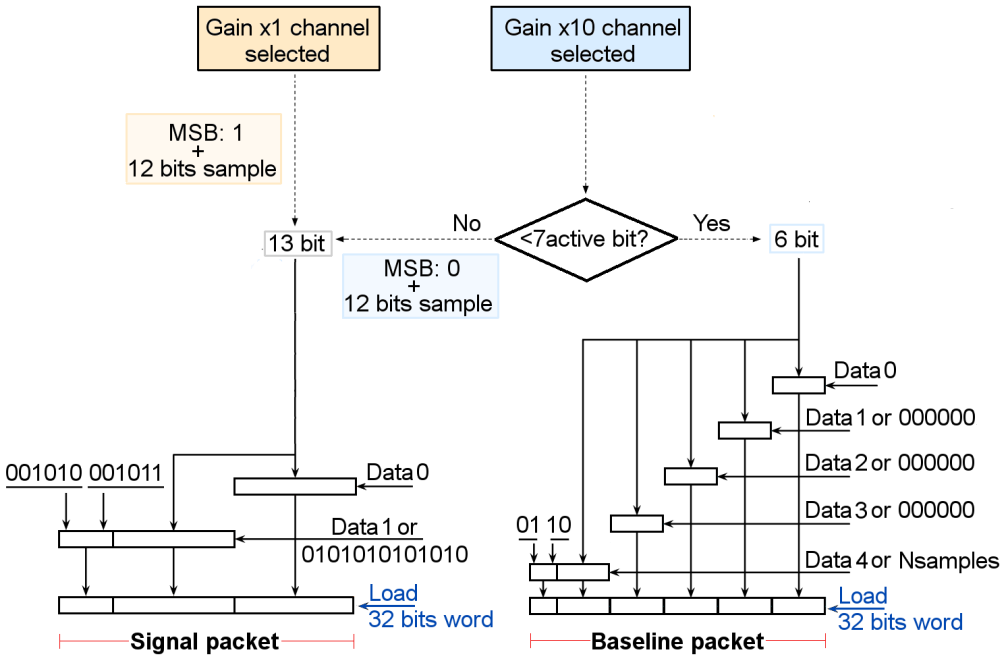


Figure 3.38: Scheme of the 32-bit packet generation system.

The applied compression allows the reduction of the data rate per LiTE-DTU ASIC from 2.08 Gb/s to ∼ 1.08 Gb/s [Equation 3.16]. The estimated output bandwidth takes into account the rate contributions of the diverse data packets, as reported below, and a predicted protocol overhead of 50 Mb/s. Therefore the overall data rate allows to still have a 16% free bandwidth on the e-link available bandwidth.
The event probability with more than 6 significant (non-zero) bits is:

$$P_{>\ 6\text{-bit}} = 5.8 \cdot 10^{-4} \tag{3.10}$$

and the sampling frequency:

$$f_s = 160\,\text{MS/s} \tag{3.11}$$

The number of samples in the baseline packet, in the signal packet, mean value in the baseline incomplete packet, and in the incomplete signal packet are: $N_B = 5$, $N_S = 2$, $N_{B\_S} = 2.5$, $N_{S\_B} = 1$. Thus the four data packets bandwidth are respectively:

$$B_{rate} = f_s \cdot (1 - P_{>\ 6\text{-bit}}) \cdot 32\ \text{bits}/N_B = 1.02\ \text{Gb/s} \tag{3.12}$$

$$S_{rate} = f_s \cdot P_{>\ 6\text{-bit}} \cdot 32\ \text{bits}/N_S = 1.5\ \text{Mb/s} \tag{3.13}$$

$$B\_S_{rate} = f_s \cdot P_{>\ 6\text{-bit}} \cdot 32\ \text{bits}/N_{B\_S} = 1.2\ \text{Mb/s} \tag{3.14}$$

$$S\_B_{rate} = f_s \cdot P_{>\ 6\text{-bit}} \cdot 32\ \text{bits}/N_{S\_B} = 3.0\ \text{Mb/s} \tag{3.15}$$

The overall data rate for a single LiTE-DTU ASIC can be calculated as:

$$\text{Bandwidth}_{\text{channel}} = B_{rate} + S_{rate} + B\_S_{rate} + S\_B_{rate} + \text{overhead}_{rate} =< 1.08\ \text{Gb/s} \tag{3.16}$$

However, the LiTE-DTU introduces a latency which needs to be carefully evaluated in order not exceed the overall EB trigger latency budget (1.5 μs) [50]. The latency due to the compression mechanism must count on a modest fraction of this time period. The details on the latency studies performed on the DTU are reported in Section 3.7.7.

In Figure 3.39 the result of a simulation of the data compression and data word generation unit is shown. In input there are two peaks, the selected samples are transmitted from the gain channel selection unit along with the baseline_flag signal and the compression procedure handles the latter in order to generate the 32-bit output (in red). When the data word is complete there is a rising-edge of the Load signal. The Load rises-up every 5 clock periods when there are only baseline packets generated, while during the signal packet assembling its rate increases. Figure 3.40 is a zoom-in of the first part of the previous simulation. In this picture is possible to distinguish the different kind of generated data words.

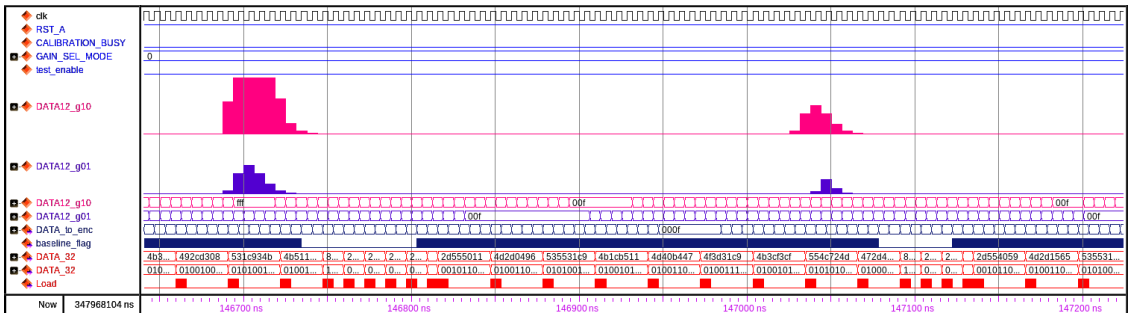


Figure 3.39: Simulation of the behavior of the compression method applied in the DTU. The red signals are: the generated 32-bit data word (both in hex and binary) and the Load signal.

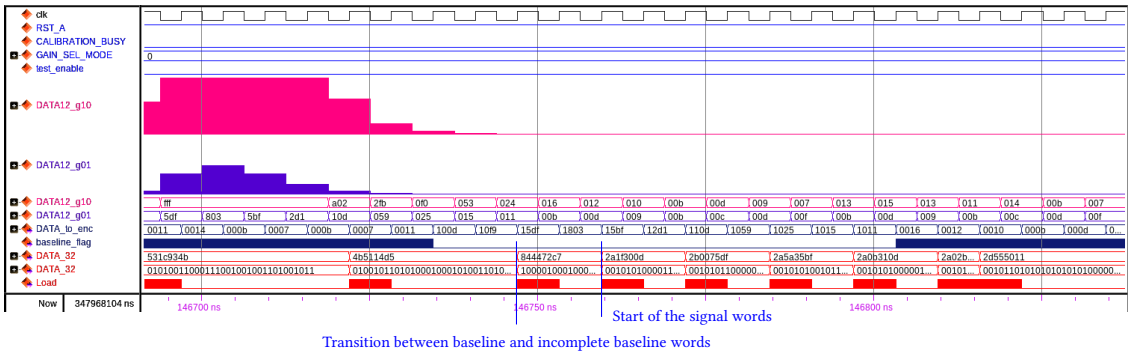


Figure 3.40: Simulation of the behavior of the compression method applied in the DTU. The red signals are: the generated 32-bit data word (both in hex and binary) and the Load signal.

3.7.4 Control unit block

The Control Unit (CU) of the DTU is connected to the data compression and data word generation block, to the compensation memory, and to the serializer block. The CU manages the data frame generation, through the insertion of a trailer words in the stream of data words, the storage of the data words in the compensation memory, and it takes part in the handshake process with the serializers. As shown in Figure 3.41, the unit inputs are the Clock at 1.60 MHz (CLK_{160}), the reset signal, two signals from the previous block: the 32-bit data words (DATA_32) and the Load signal, a full signal from the compensation memory and the handshake signal coming from the serializers. The output are a write signal and the associated 32-bit word signal, a read signal, a losing_data signal and the TMR block signal.

The CU organizes the 32-bit data word in frames, each frame is completed by a frame trailer and contains 51 data word. The trailer is a 32-bits word, it contains some

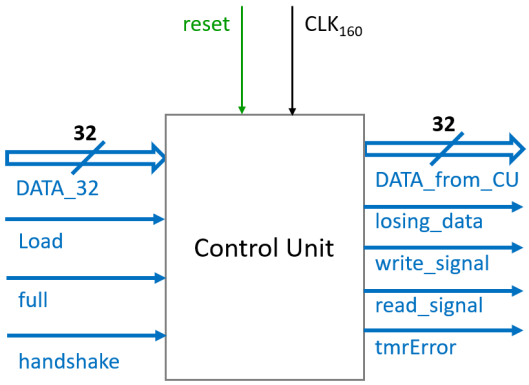


Figure 3.41: Sketch of the control unit of the DTU.

useful information about the entire frame in order to have some guidelines for the data correctness monitoring in the DAQ system. Trailers are composed by an header "1101", followed by 8-bit dedicated to the number of samples transmitted since the previous delimiter, 12-bit for the Cyclic Redundancy Check (CRC) of the 51 data packets, and the last 8-bit represent the frame identifier number.

An example of the trailer structure is reported in Figure 3.42. To count the number of samples there is a block that reads the header of 32-bit data words and keeps track of the total number of samples in the frame. The distance between trailers is fixed to 51 because if there are only baseline packets, the number of samples turns out to be 255, and the counter saturates to its maximum value. The 12-bit CRC is calculated and updated whenever there is a new 32-bit data packet generated by the compression unit. The CRC is an error-detecting code used to prevent random errors in transmission and to determine if data has been corrupted. This method is similar to the checksum but is uses polynomial division to determine the value of the CRC [92], [93].

The CRC implemented in the CU of the DTU is a standard Telecom CRC-12 based on the polynomial $x^{12}+x^{11}+x^3+x^2+x+1$. Lastly, the frame identifier number is managed by a block which simply counts incrementally the number of the completed data frames. Trailers are sent to the compensation memory paying attention not to overlap with the 32-bit data word coming from the compression mechanism (the data words have always the priority). An example of trailer sent to the compensation memory is shown in Figure 3.48. The trailer is highlighted in yellow and it is 0hDFB8485B which means that in the frame there are 251 (0hFB) samples, the CRC is 0h848, and the identification number of the frame is 91 (0h5B).

The CU continuously communicates with the compensation FIFO and the serializers block. The former directs the memory write operation, when there is a data word or a

Trailer	1101	# Samples (8 bits)	CRC 12	Frame ID (8 bits)

Figure 3.42: Structure of the trailers inserted by the control unit in order to divide and organize the data words.

trailer to be stored, and starts the read action when the serializers block through an handshake process send a signal to check if there are some packets in the memory.

3.7.5 Compensation memory module

The compensation memory block is a FIFO embedded in the DTU, preceded and followed by an Hamming encoder and decoder respectively. The compensation memory module is directly connected to the CU and serializers block. As shown in Figure 3.43, the block inputs are: the CLK_{160}, the reset, the 32-bit data packets or trailers coming from the CU, the read and write signals. The output signals are an empty and full signals, the TMR block signal, and lastly the 32-bit decoded packet and the related signal which notify that the decoding is concluded.

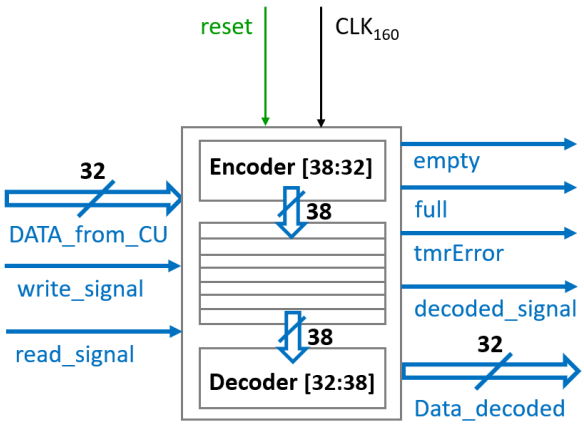


Figure 3.43: Schematic of the compensation memory of the DTU.

The CU sends the 32-bit data packets or trailers to the compensation memory system, when they are ready. In order to do so, the write signal activates the encoder [38:32]. The applied encoding is the Hamming code, therefore a 38-bit word is obtained from the 32-bit packet through a series of XOR operations on the data bits. The Hamming code is an error detection and correction technique [65], [66], and [67] is used for data protection. In Figure 3.44 a scheme of the [38,32] Hamming encoding is represented: the d-bit are the data bits, the p-bit are the parity bits added to the 32-bit packet.

Each row next to the parity bit highlights which data bit are covered by the correspondent parity bit. After the encoder, the 38-bit word is inserted into the compensation

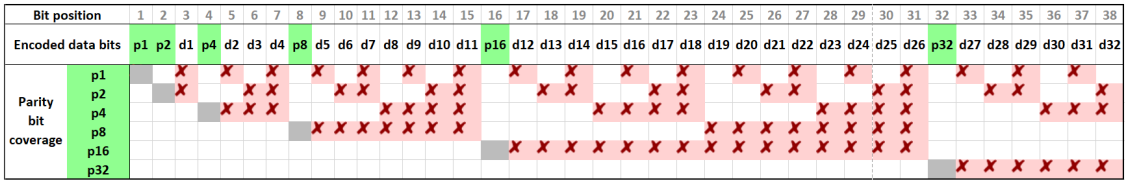


Figure 3.44: Scheme of the applied Hamming code in the compensation memory of the DTU.

memory which is used to temporarily store the packets and balance the rate of the data word generation intrinsic to the compression process. Indeed, the number of clock cycles required in order to complete a baseline packet is higher with respect to the time needed for a signal packet generation, as shown in Figure 3.39. The depth of the FIFO is 16, this size has been selected in order to avoid the introduction of a non-negligible latency component. The latency studies performed on the DTU are reported in Section 3.7.7. Therefore, the selected size is a trade-off between the maximum number of packets which can be stored and the block latency contribution.

When the CU receives the handshake signal from the serializers block, it sends a red signal to the compensation memory. If the compensation memory has at least one packet stored, it starts the Hamming decoding procedure and at the end sends to the serializers block the 32-bit packet. The decoding operation is the opposite of the encoding one, therefore a 32-bit packet is obtained from a 38-bit packet. If during the storage period, a radiation-induced error has occurred in the packet, the block detects and corrects it automatically.

On the other hand, if the memory is empty, the empty signal is transmitted to the serializers block to send out the OM_idle pattern. This situation is very likely and it happens when several baseline packets arrive one after the other in the compensation memory. Indeed, the baseline packets are spaced in time, from each other, by 5 clock periods (31.25 ns), while the serializers block tries to ask for a new packet every 4 clock periods (25 ns) as shown in Figure 3.45. In the center of Figure 3.45 some signals managed by the compensation memory are displayed:

- data_38_ham_in is the 38-bit Hamming encoded word which is stored in the FIFO;
- empty, full, and losing_data signals are flags useful to determine the memory status;
- the distance signal is a register which continuously update the difference between the reading and writing pointer of the FIFO;

- data_38_ham_out is the 38-bit packet stored in the FIFO which have to be decoded in a 32-bit word;
- the decode signal is triggered by the read_signal coming from the CU and starts the Hamming decoding of the data_38_ham_out which becomes the DATA32_to_serializer.

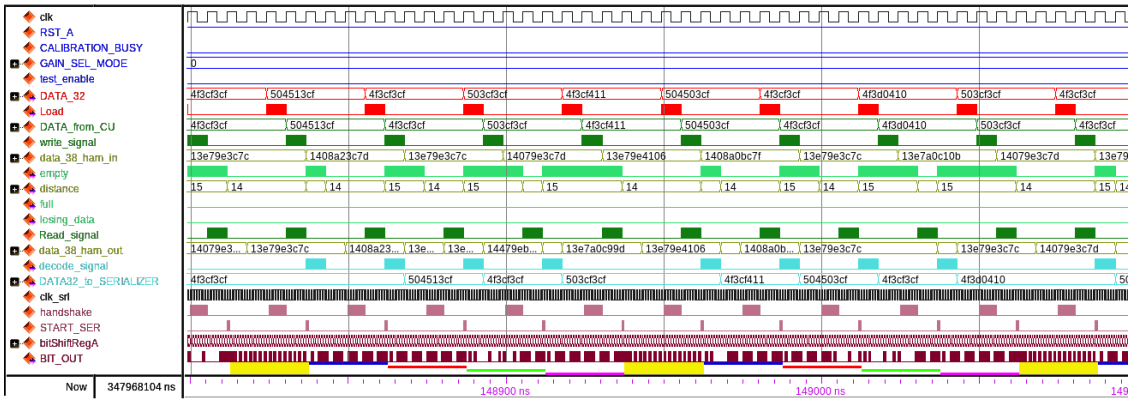


Figure 3.45: Simulation of the behavior of compensation memory during the transmission of baseline packets. At the bottom of the waveform plot, the typical pattern of serialized OM_idle pattern packets, highlighted in yellow, are transmitted every 4 consecutive 32-bit data packets (highlighted in blue, red, green, and magenta, respectively).

3.7.6 High-speed serializers block

The serializers block is a radiation tolerant block embedded in the DTU for high-speed and reliable communication. The radiation hard design is based on TMR technique and this module is the only one in the LiTE-DTU which receives both CLK_{160} and $CLK_{1.28}$. The block employs four 32-bit serializers in order to send out data packets through e-links at 1.28 Gb/s. The serializers block receives data from ATU or from the compensation memory, depending on the value of the ATM test signal. As anticipated in Sections 3.6 and 3.7, if the ATM test signal has a high logic value the serializers receive packets from the ATU, on the other hand if the ATM test signal has a low logic value the data packets come from the DTU.

As shown in Figure 3.46, the block inputs are: the $CLK_{1.28}$, the CLK_{160}, the reset, the ADC calibration signal, the ATM test signal, and the 32-bit signals coming from ATU and DTU. The output signals are the four differential output: dout_0, dout_1, dout_2, and dout_3, the handshake and the TMR block signals. The serializers are 32-bit shift-registers that sends out the packet bits with a big-endian order.

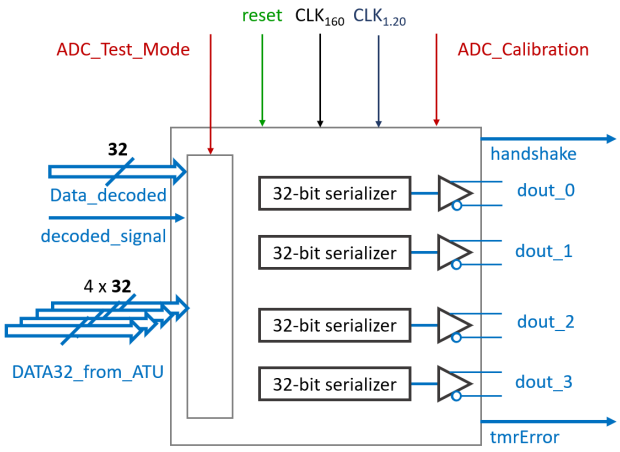


Figure 3.46: Schematic of the high-speed serializers block of the LiTE-DTU.

During the operational mode of the LiTE-DTU, the serializers block manages the handshake process in order to check if in the compensation memory there is at least one data packet. In case of empty memory the block transmits on the dout_0 the OM_idle pattern, with the purpose of keeping the serial link active and to avoid the loss of synchronization. The clock-like structure of the OM_idle pattern is illustrated in Figure 3.47. As anticipated in Section 3.7.5 and shown in Figure 3.45, when the compensation memory receives mostly baseline packets, after 4 data words serialized an OM_idle pattern is inserted.

IDLE	1110	10101010101010101010101010

Figure 3.47: Structure of the OM_idle pattern.

The handshake signal rising-edge occurs when the read pointer for the serialization has a value of 0x0F and it returns back to the low logic value 7 $CLK_{1.28}$ periods later. This process takes into account that the handshake signal is sent to the CU which, in presence of a packet in the memory, has to trigger the Hamming decoding. As a result, the decoded data arrive in time for the serialization, avoiding packet superposition. Figure 3.48 shows the handshake mechanism in the two different cases: when the compensation memory is empty and when there is a stored packet.

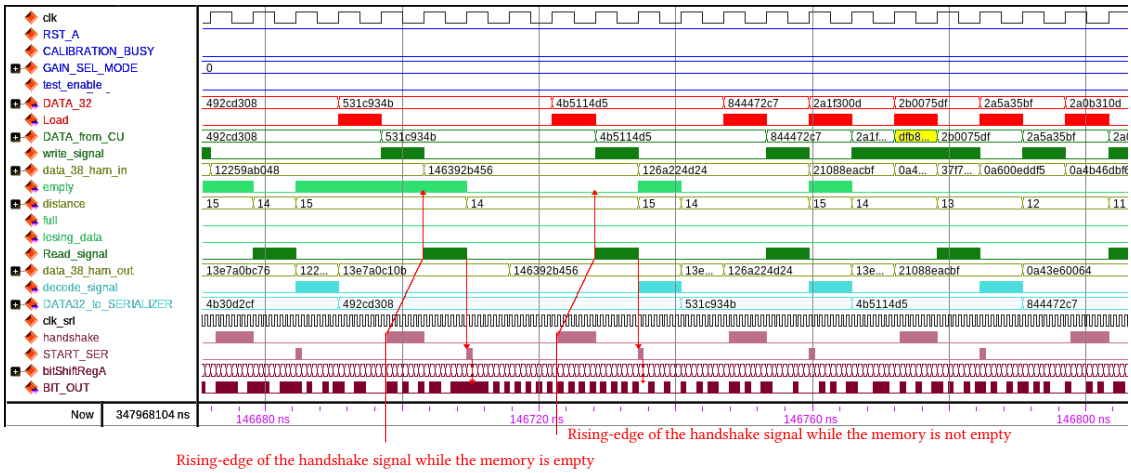


Figure 3.48: Simulation of the behavior of the serializers unit. Moreover, in yellow is highlighted a trailer inserted by the CU, 0hDFB8485B, which has been inserted between two signal packets.

3.7.7 DTU latency studies

Several tests have been performed, using both real data and simulation, to verify that the DTU design is robust and all the requirements are satisfied. Firstly, the DTU must transmit all the samples, without any data loss. Then the system latency must not exceed the 350 ns, which is considered the safe limit [91]. The purpose of these latency study is to investigate the event rate and energy combinations for which the DTU requirements are dropped, and estimate their probability during the data taking.

At the end of the HL-LHC phase, the expected maximum RMS noise will be equivalent to a signal of 250 MeV, dominated by the APD leakage current. In the low gain channel, 250 MeV corresponds to 5 ADC counts, because the maximum energy value is 200 GeV and the ADC LSB for 12 bits corresponds to 48.8 MeV (see Section 2.3.2). The pedestal is set to 3 σ from zero thus 15 ADC counts. Referring to the threshold between the baseline and signal samples (6-bit or 64 ADC counts) and taking into account both the noise and the pedestal, the maximum energy value that can be coded with 6-bit during HL-LHC will be:

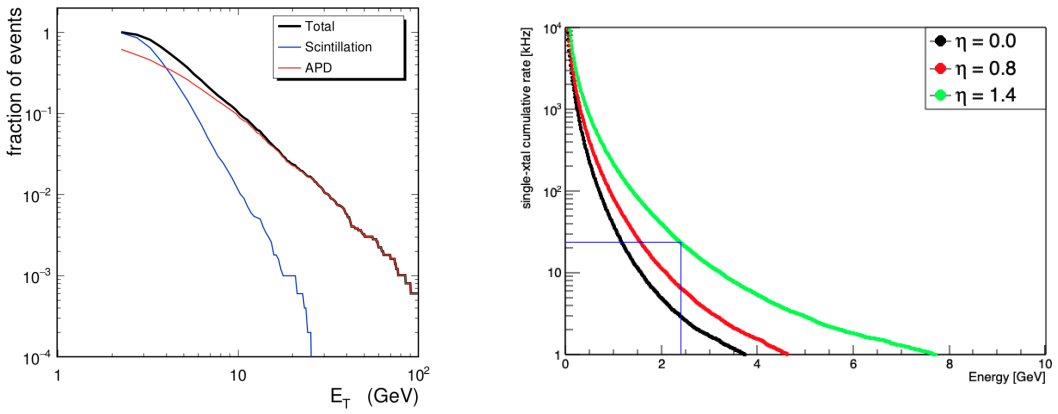
$$E_{max\_bas} = (64 - 15)\ ADC\_count \cdot 48.8\ MeV/ADC\_count = 2.4\ GeV \tag{3.17}$$

As anticipated in Section 3.7.3, the simulation [91] shows that the fraction of hits in a single crystal in HL-LHC conditions with E > 2.4 GeV is $5.8 \cdot 10^{-4}$ [Equation 3.10] at the highest pseudorapidity value. In this condition the total estimated output bandwidth of the DTU is 1.08 Gb/s [Equation 3.16] leaving a 16% free bandwidth from the

1.28 Gb/s available. Assuming that the fraction of events requiring 13-bit is forty times higher than $5.8 \cdot 10^{-4}$, the calculation results in 1.276 Gb/s, still within the allocated bandwidth. In order to assess the DTU latency limits with detailed simulations several dataset have been generated with a Monte Carlo (MC) simulation. The simulation output have been analyzed by a dedicated software written in python which performs the data packet decompression, the direct check between the input files and the output files, the calculation of the samples latency, and generates report plots.

Monte Carlo strategy

The compression algorithm of the DTU unit will act on a stream of un-triggered ADC samples. In CMS Phase I, these data are called *ZeroBias* stream. The events have the same frequency of the HL-LHC bunch-crossing signal rate which is 40 MHz. Figure 3.49a [50] highlights the contribution to the total rate from scintillation light and *spikes*, respectively.



(a) (b)

Figure 3.49: Estimated fraction of scintillation and spike events (left) and cumulative event rate for individual channels at three different pseudorapidity values obtained by the MC simulation (right).

Figure 3.49a shows that the spike events rate dominates above an energy of 5 GeV. Thus in order to generate a dataset of *ZeroBias* stream both electromagnetic showers and *spike* events have to be taken into account. This evaluation has been performed with a simplified MC simulation, which generates hits according to an energy spectrum derived from a full simulation. The dataset obtained by the MC includes physical events, *spikes*, and the expected HL-LHC pile-up is added.

Figure 3.49b shows the cumulative event rate in each individual channel of the EB, for three values of pseudorapidity. Therefore the expected total rate of hits above 2.4 GeV [Equation 3.17] does not exceed 20 kHz.

With the goal of figure out the combinations of energy and rate at which the DTU system starts to lose data or goes over the target latency of 350 ns, the used datasets for the simulation contain pulses of a given energy at different rates.

The streams of 12-bit samples have been fed to the DTU backannotated Verilog model. Each dataset contains a train of pulses lasting two LHC orbits ($\sim$ 177 μs). Figure 3.50 shows the typical structure of a LHC orbit.

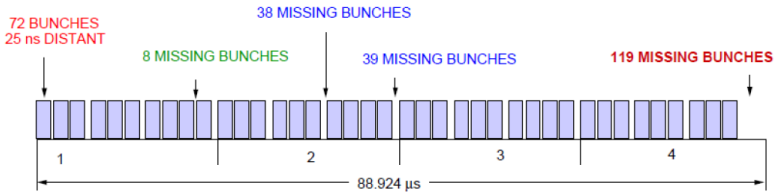


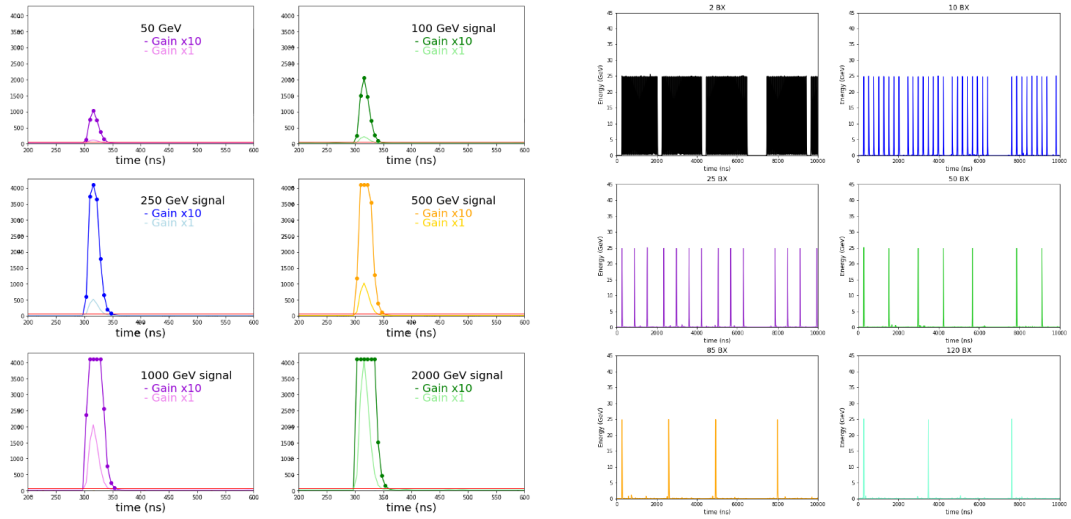
Figure 3.50: The LHC bunch structure lasts 88.924 μs and the number of bunch crossings per orbits is 2808 [94].

The pulse shape has been extracted from test beam measurements. Indeed, the signal shape depends on the responses of APD and CATIA ASIC. The used set of pulse energies are: 5 GeV, 25 GeV, 50 GeV, 100 GeV, 250 GeV, 500 GeV, 1 TeV, 2 TeV, 5 TeV, and the rates of pulse injection are: 20 MHz, 4 MHz, 3.3 MHz, 2.5 MHz, 2 MHz, 1.8 MHz, 1.6 MHz, 0.8 MHz, 0.47 MHz, 0.33 MHz (or a pulse every 2, 10, 12, 16, 20, 22, 25, 50, 85, 120 bunch crossings). Some pulse and injection rates examples are shown in Figure 3.51a and Figure 3.51b, respectively.

In Figure 3.52a and Figure 3.52b there are two examples of plots obtained during the evaluation of the DTU latency. In Figure 3.52a the pulses are injected at the frequency of 1.6 MHz and the latency is below 350 ns for all the pulse energies. In Figure 3.52a the frequency is 4 MHz and the pulse signals of energy up to 25 GeV still have a latency below 350 ns, while for signals of energy exceeding 100 GeV the latency distribution is pushed towards 500 ns. In this case, the compensation memory is full and each generated 32-bit data packet must wait until the whole FIFO has disposed of its content and some of them are lost due to the overwriting process of the memory.

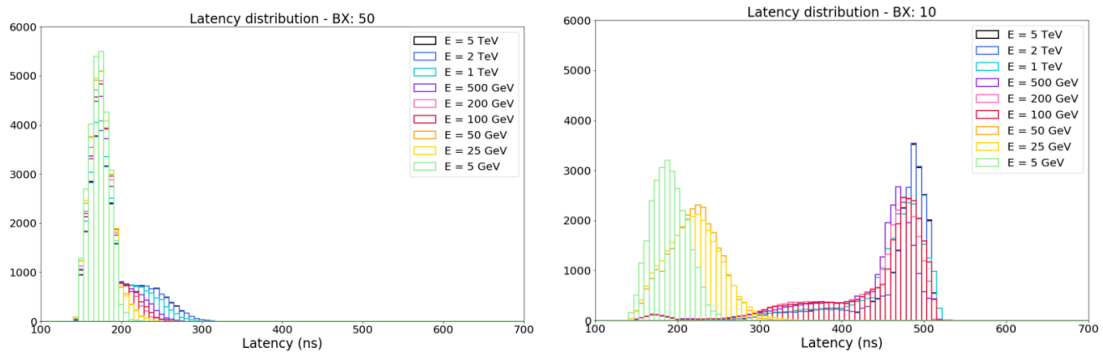
These energy-rate combination scan has highlighted that:

- for energy > 5 TeV, rate = 1.6 MHz, the DTU latency exceeds the allocated budget of 350 ns but no data-loss has been observed;
- for energy $\geq$ 100 GeV, rate = 4 MHz, the DTU latency is higher than the safe



(a) (b)

Figure 3.51: Examples of pulses in the energy range 50 GeV - 2 TeV (left) and examples of rates of pulse injection 20 MHz, 4 MHz, 1.6 MHz, 0.8 MHz, 0.47 MHz, and 0.33 MHz (right).



(a) (b)

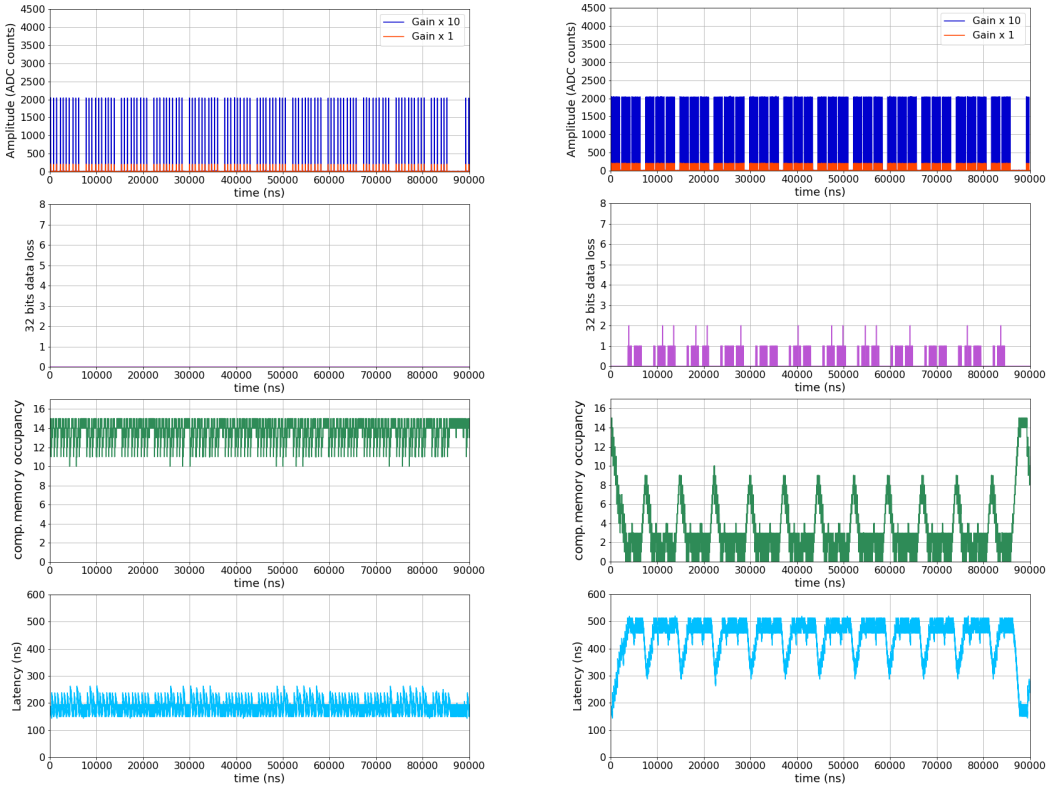
Figure 3.52: Latency plots of pulses with energy range 5 GeV - 5 TeV at 1.6 MHz (left) and 4 MHz (right).

limit of 350 ns but the system starts to lose the 32-bit data packets only after 12 consecutive pulses;

- for energy = 5 GeV, rate = 20 MHz, the DTU behavior is similar to the previous case: the latency is higher than the safe limit of 350 ns but the system starts to lose the 32-bit data packets only after 13 consecutive pulses;

All other cases do not generate a critical condition. However, from the simulations the expected rate of 5 GeV particles is well below 10 kHz, which gives broad margin, and rate of higher energy signals is also well below the observed limits of the system.

During the latency studies the behavior of the DTU structure has been studied in detail by use of several plots generated by the analysis software written in Python. An example of typical used plots are shown in Figure 3.53, which shows from the top the pulses, then the number of dropped samples, the occupancy of the compensation memory, and lastly the sample latency. Both Figure 3.53a and Figure 3.53b are referred to pulses with energy of 100 GeV while the injection rates are 1.6 MHz and 4 MHz, respectively. On the left the DTU system shows normal behavior and no data-loss while on the right after 12 pulses the DTU starts to drop packets, the memory becomes full, and the latency increases.



(a) (b)

Figure 3.53: The plots depict (from the top to the bottom) the input pulses, the number of dropped samples, the occupancy of the compensation memory, and the sample latency. Pulses energy of 100 GeV and injection rates of 1.6 MHz (left) and 4 MHz (right).

Simulating standard running conditions

After the systematic use of the same energy pulse injected at different constant rate into the system, another performed test is the simulation of the DTU behavior using the expected standard running conditions during HL-LHC. The adopted dataset are composed by randomly injected pulses with an energy extracted from the energy spectrum derived from the full simulation. Also in this simulation the spike events have been included and the LHC filling scheme was used. The total number of generated input samples is $1.6 \cdot 10^8$ (1 s) and during the simulation the system never lost samples or exceed the target latency. In Figure 3.54 the latency of the DTU is shown, with an highlight on the three main contributions:

- the green one is the latency distribution of the samples from the input to the end of the packet generation;
- the orange one is the latency distribution which includes also the component due to the CU and compensation memory operations;
- the blue is the total distribution of the DTU system, therefore contains the previous one plus the contribution of the serializers unit.

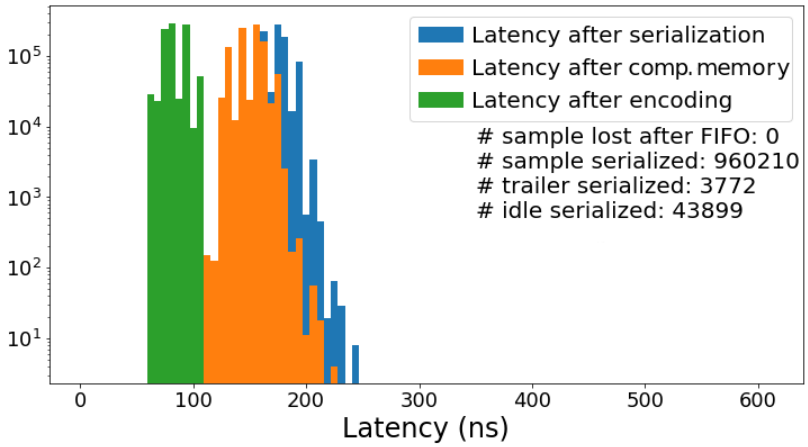


Figure 3.54: The latency distribution of the DTU system obtained in standard running condition simulation.

In Figure 3.55, a portion of the data input and the occupancy state of the compensation memory during the simulation time are shown.

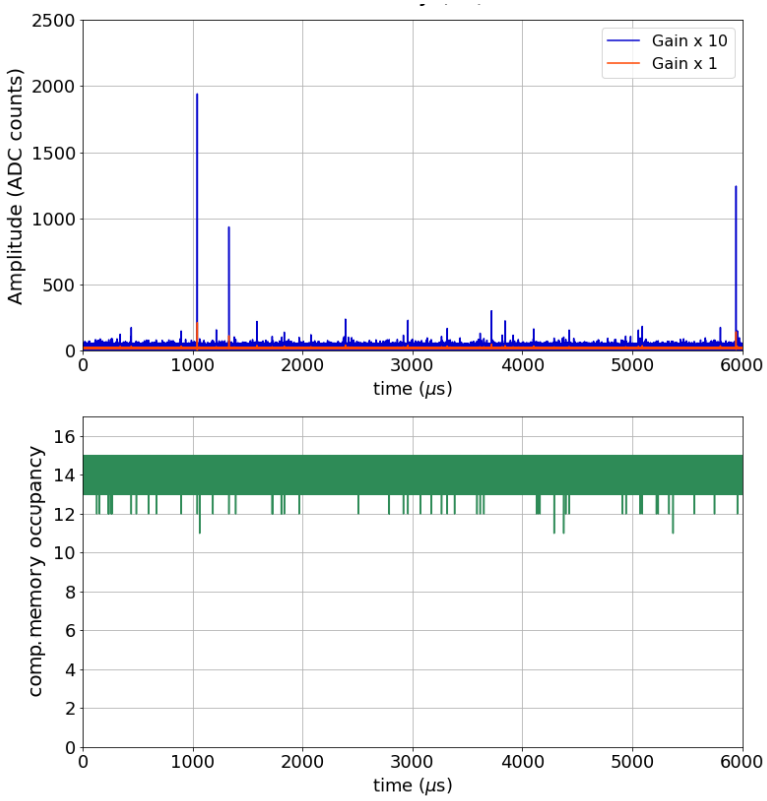


Figure 3.55: A portion of the ADC traces (top) and the compensation memory occupancy trend (bottom) during a DTU simulation in standard running condition.

3.8 Summary

The LiTE-DTU ASIC has been designed in 65 nm CMOS technology and submitted at the end of November 2018 in an Europractice mini@sic submission. The ASIC has a size of 2 × 2 mm^2

The chip has been developed for the upgrade of the VFE board of the EB at CMS. It embeds a commercial ADC designed by an external company, the PLL inherited by the CERN LpGBT project and the digital architecture designed at INFN Torino.

In this chapter, all the blocks present in the first prototype of the LiTE-DTU have been described, detailed explanation along the performed post-layout simulations of the DTU have been presented and the latency studies accomplished to assess the performances of the architecture have been explained. The results obtained showed that the LiTE-DTU latency fits well the trigger requirements for the HL-LHC data taking.

Chapter 4

The LiTE-DTU characterization

The LiTE-DTU ASIC has been submitted at the end of 2018 in a Europractice mini@sic run and the prototypes have been received four months after. 60 LiTE-DTU ASIC have been received as naked dies while 40 dies have been packaged in a 10 mm × 10 mm QFN72 package: 30 of them have a sealed lid and the remaining 10 dies have a taped lid for die inspection and irradiation tests. In Figure 4.1 a microscope photograph of the LiTE-DTU ASIC is shown. The profile of the two ADCs, the PLL and the digital logic can be seen in this picture. Moreover, golden wire bondings connect the IC pads to the package pins.

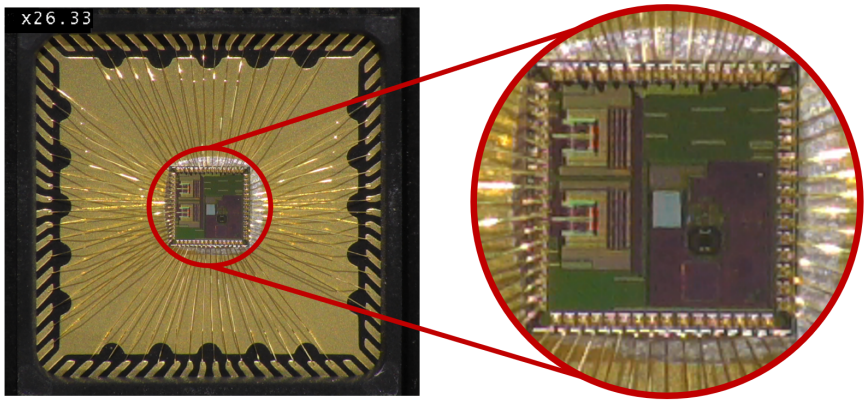


Figure 4.1: Microscope image of the LiTE-DTU.

In the earlier part of this chapter, the experimental setup for the LiTE-DTU characterization is illustrated. Then, the last part is dedicated to the detailed description of test performed on the ADCs, PLL, and DTU blocks. My contribution during the LiTE-DTU tests has been mostly oriented to the data acquisition and the validation of functional

correctness of the LiTE-DTU ASIC. This process has been done initially for the individual features of the chip and then it has involved the whole design.

4.1 Experimental setup

A photo and a scheme of the experimental setup employed for the ASIC characterization at the laboratory of INFN Torino are shown in Figure 4.2 and Figure 4.3, respectively. The experimental setup includes:

1. LiTE-DTU test board
2. Two low jitter clock generators: *Stanford research system CG635*: one is for the CLK_{160} and the other has been used for the $CLK_{1.28\ ext}$ and for the input signal generation (differential). The clock generator random jitter is $\sim$ 1.8 ps and the deterministic jitter is $\sim$ 2.3 ps.
3. Clock splitter *Silicon Labs Si53301*: it has been employed to provide the same CLK_{160} to the LiTE-DTU, the FPGA, and to the oscilloscope.
4. Signal Generator: *Teledyne test tools T3AFG120*: it has been used for the sinewave generation and pulse generation for the LiTE-DTU input signal (single-ended).
5. Power supplies:
   (a) *Rhode & Schwarz NGE100*: its three channels have been used for the analog (3 V), digital (3 V), and drivers (4 V) power supplies.
   (b) *Kenwood PWR18-18Q*: it has been used tor the clock splitter power supply: 3.3 V.
   (c) *Agilent E3631A*: it has been used to generate the two reference voltages for the ADCs calibration procedure.
6. Two oscilloscopes:
   (a) *Tektronix DPO 70604* (6 GHz, 25 GS/s): it has been used to check the $CLK_{1.28}$ generated by the PLL, verify the lock of $CLK_{1.28}$ to the CLK_{160}, and to characterize the $CLK_{1.28}$ jitter.
   (b) *Tektronix TDS 3054B* (500 MHz, 5 GS/s): it has been mostly used during the early stage of the test on the I^2C.
7. Two pairs of high quality bandpass filters mainly used during the ADC tests in order to reduce the harmonic distortion and random noise from the input signal:
   (a) *TTE P1116*: Q70T-500K-10P-50-720A, f_{in} = 500 kHz

(b) *TTE P1119*: Q70T-50M-10P-50-720A, f_{in} = 50 MHz

8. SMA / FMC transition board: it is a custom board used for an easier mechanical connection between the SMA signal cables and the FPGA FMC connector.
9. Logic-Level translator: *Texas Instruments* SN74AXC4T774EVM: it has been used to translate the SDA signal of the I^2C.
10. FPGA - Kintex UltraScale: if has been used to send configuration signals and for the data acquisition. The data have been sent to the PC via Ethernet.
11. PC - OS: Windows 7, software: LabView.

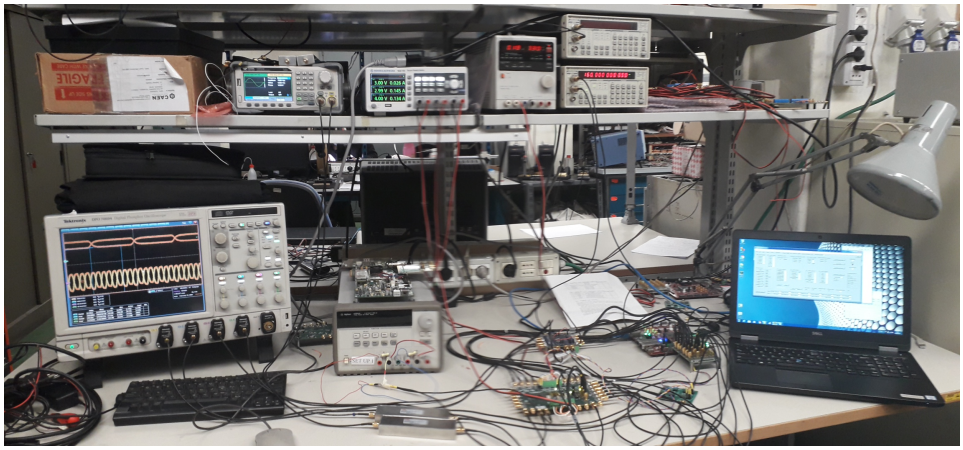


Figure 4.2: Test setup for the LiTE-DTU ASIC in the laboratory of INFN Torino

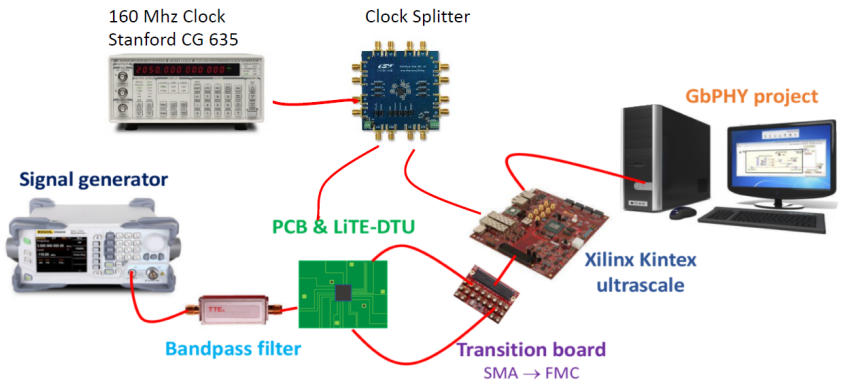


Figure 4.3: Scheme of the test setup for the LiTE-DTU ASIC.

4.1.1 The LiTE-DTU test board

A custom Printed Circuit Board (PCB) has been developed for the LiTE-DTU characterization tests. It has been designed at the Electronics laboratory of INFN Torino. A 3D representation of the PCB is shown in Figure 4.4 while the layout and schematic are shown in Appendix A.

The test board has six-layers with the following organization: the TOP and the BOTTOM are the two external layers, then there are two ground layers (GND_TOP and GND_BOTTOM), both of them have a cut in the planes in order to split the analog and digital grounds, and the two last layers are the power plans (PWR_TOP and PWR_BOTTOM).

The PCB design embeds:

- 34 soldering pads for the SMA connectors to drive the input/output signals;
- two RF Transformers used as baluns in order to convert the ADCs input signals from single-ended to differential;
- two shunt regulators to set precisely the common mode voltage, V_{CM} = 600 V, of the ADCs input;
- a push button switch for the ASIC reset;
- a dip-switch for the I^2C address selection;
- a jumper in order to switch between ATU and DTU operational mode;
- four data drivers capable of translating any level input signal to LVDS. This device can drive data signals up to 1.5 Gb/s;
- a dual bidirectional I^2C bus voltage-level translator;
- three high-speed differential line drivers for the PLL_lock, SEU_A and SEU_D signals;
- several PCB terminal blocks with screw clamps for a quick and simple connection of the power supply cables;
- eight ultralow-noise low-dropout linear regulators in order to maintain a steady voltage in the power planes of the PCB;
- some pins for debug purposes.

4.1.2 DAQ system and GUI control panels

The FPGA board is the core of the DAQ system. It manages the ASIC configuration, performs a first data manipulation and the data transmission to the PC. The communication channel between the FPGA and the PC has been done through an Ethernet link

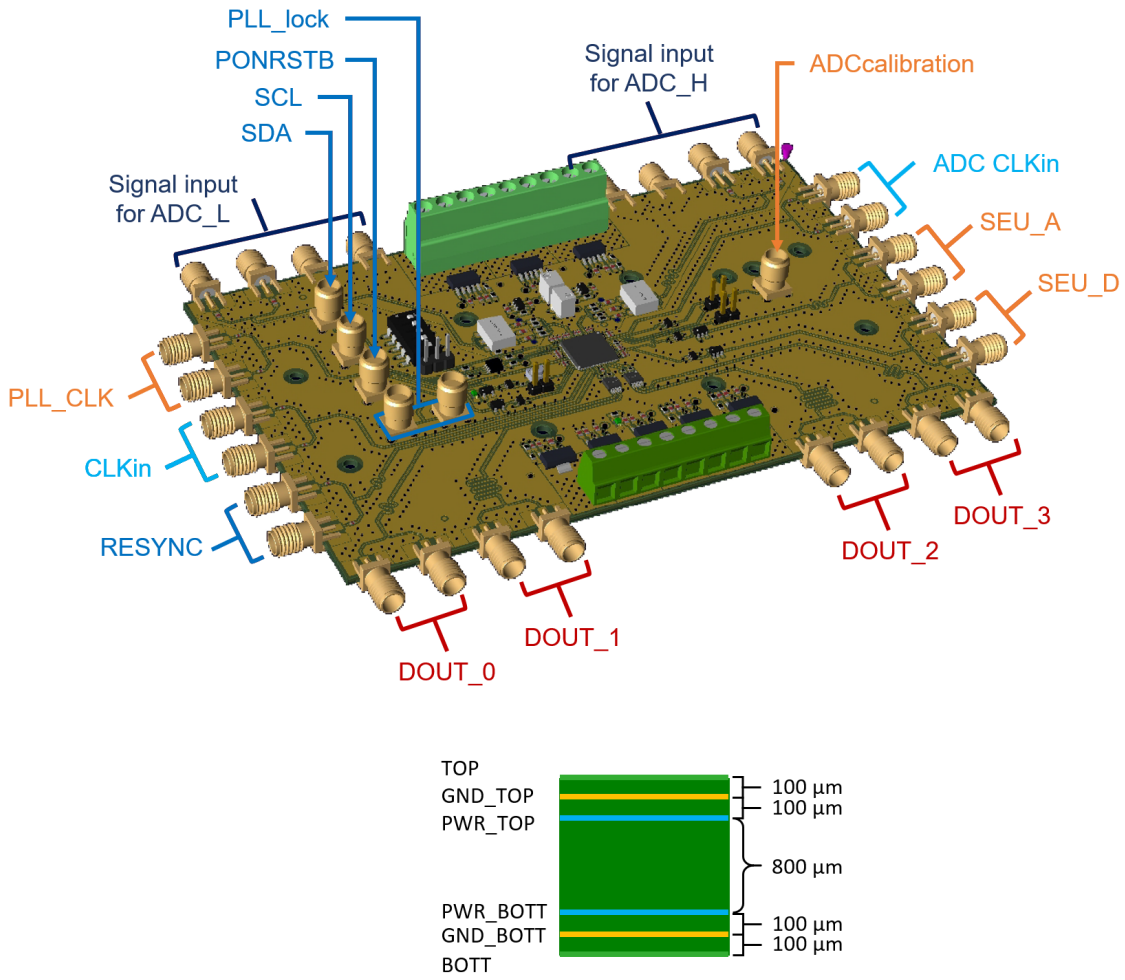


Figure 4.4: The PCB for LiTE-DTU characterization along with the input/output signal labels (top) and the vertical cut view of the PCB layers (bottom).

based on a User Datagram Protocol (UDP) interface provided by Xilinx. The UDP is suitable for applications that require an high bit rate, as in LiTE-DTU case because the output streams have a bit rate of 1.28 Gb/s. The PC has the LabVIEW FPGA software toolkit installed and the data acquisition is managed through a LabVIEW program. The VHDL code for the FPGA and LabView interfaces have been obtained customizing a pre-existing project designed at the Electronics laboratory of INFN Torino [95].

The LabView interface allows to perform several operations that are listed below:

- Reset the LiTE-DTU;
- Check if the PLL $CLK_{1.28}$ is locked to the CLK_{160};

- Send commands to the synchronization unit (see Section3.2), e.g DTU reset, ATU reset, ADC_H calibration, etc.;
- Send and then check the 8-bit configuration registers of the ADCs, DTU, and PLL;
- Switch the polarity of the DOUT channels;
- Perform the data alignment based on the 4-bit labels that are present during the ATU operational mode and they space out the 12-bit ADC samples (Section 3.6);
- Set and check a different delay for each DOUT in order to optimize the data alignment;
- Data display and writing of binary files.

The GUI interface pages are shown in Figures 4.5, 4.6, 4.7, 4.8, and 4.9.

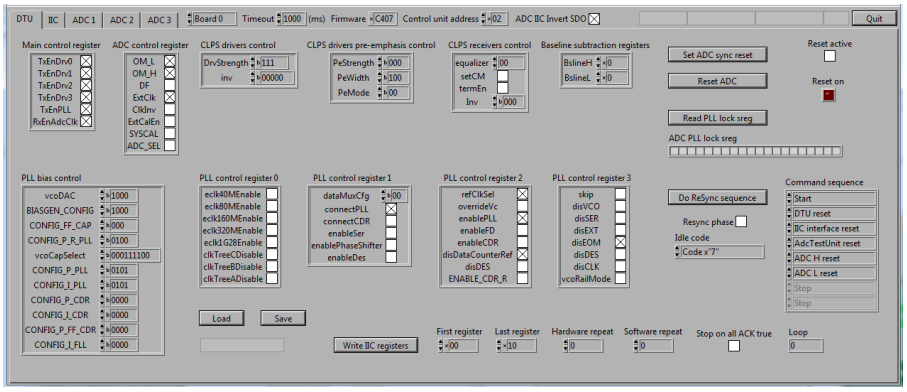


Figure 4.5: GUI control panel for the registers configuration.

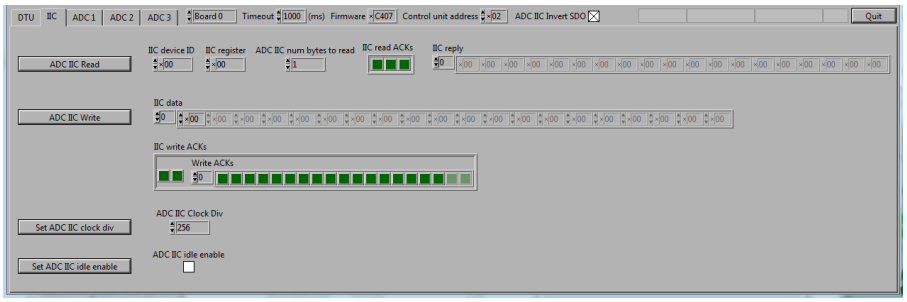


Figure 4.6: GUI control panel for I^2C write and read.

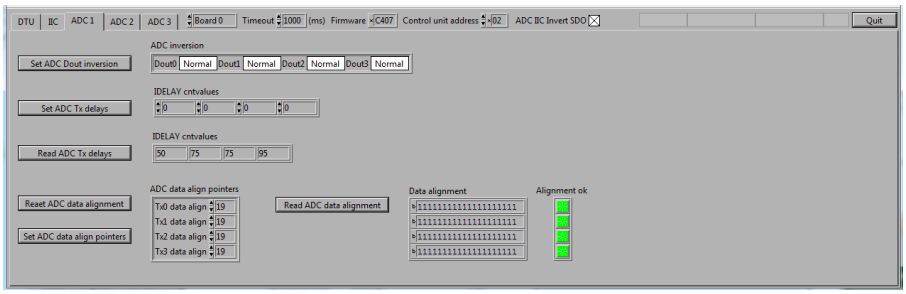


Figure 4.7: GUI control panel for the centering of the eye.

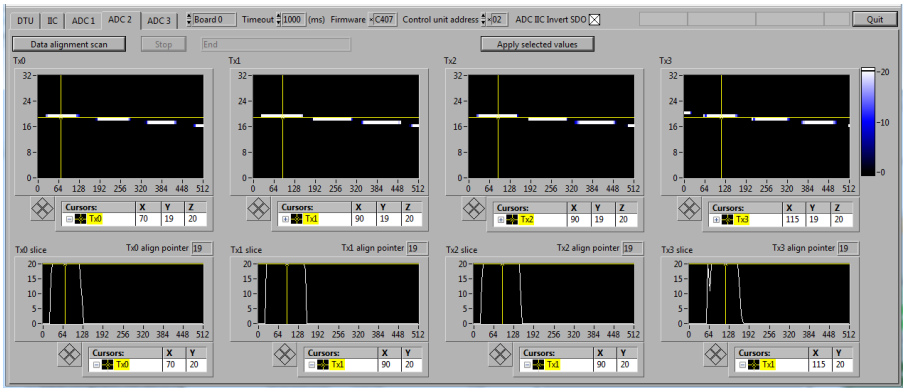


Figure 4.8: GUI control panel for the adjustment of the four channels delays. These settings allow to prevent the misalignment of the data bits. The white lines in the four plots in the top part of the window represents the 4-bit labels for the samples alignment that are present in the 32-bit words during the ATU operational mode (Section3.6).

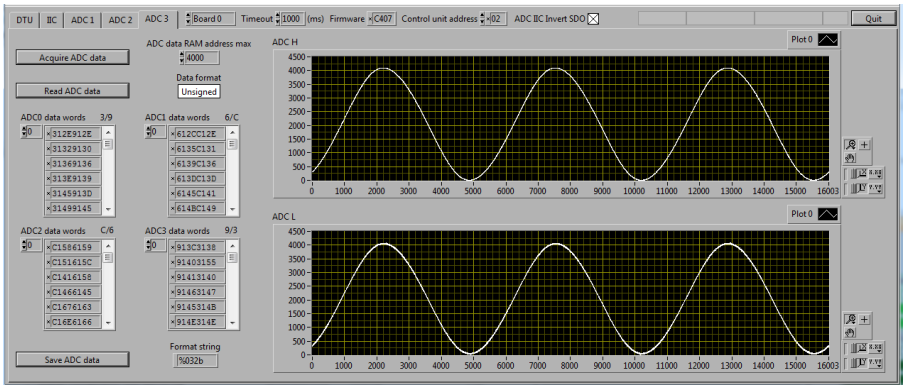


Figure 4.9: GUI control panel for displaying and saving the acquired data. The top plot represents the ADC_H samples while the plot at the bottom shows the output of the ADC_L samples. In this case both the input signals correspond to a sinewave with f_{in} = 500 kHz and amplitude comparable to the full-scale range of the ADCs.

4.2 Characterization tests and results

The first measurements have been focused on the PLL and the ADCs, only after a good comprehension of the entire system, some PCB adjustments and test setup modification the tests have been moved on the DTU block.

The start-up procedure performed at the beginning of every acquisition consists in several steps and at the end of this sequence the system is stable and ready for the data acquisition both in ATU and in DTU operational mode. The sequence is the following:

- power-on the LiTE-DTU ASIC, the clock splitter, and the FPGA;
- distribute the CLK_{160} to the system;
- reset the Data Transmission Unit (DTU), I^2C, ATU, and ADCs;
- upload all the configuration registers via I^2C;
- verify the PLL output lock;
- align the output bit streams via FPGA for the 32-bit words acquisition;
- feed the ADCs with the reference voltages and activate the calibration procedure: 850 mV to the SMA connectors in J1 and J4 and 350 mV to J3 and J6;
- verify the accuracy of the patterns alignment and then start the data acquisition.

Contrary to expectations, at the beginning of the tests a misbehavior of the I^2C interface has been detected. This issue has affected several ASICs integrated on the first batch of PCB boards. Despite the I^2C communication problem, two out of eight boards let us to perform the whole test process and to charcterize the PLL, the ADCs along with the ATU block, the serializers and the DTU block. Therefore, the measurements presented in the following sections and in Chapter 5 have been performed mainly on the board 2 and board 5 that have a sealed lid and a taped lid, respectively.

4.2.1 PLL characterization

The LpGBT PLL has been designed to work with a 40 MHz input clock; therefore a clock divider has been inserted between the 160 MHz system clock and the PLL input. Both the output clock ($CLK_{1.28}$) and the 40 MHz reference clock are externally accessible via the PllClk± and PllRefClk outputs, respectively. Moreover, a PllLock signal is available in order to check the status of the PLL.

The PLL unit contains many functionalities which are not used in the LiTE-DTU. However, most of the control bits can be controlled via the 4 PLL control registers and the 5 PLL bias control registers. The full description of the PLL configuration bits is summarized in Appendix B but the most useful register is the vcoCapSelect[8:0]. This 9-bit register manages the selection of the VCO capacitor bank. By changing the vcoCapSelect register the optimal capacitors configuration can be set in order to center the

VCO frequency at 1.28 GHz. This solution has been adopted in order to be able to use a very low jitter but small lock range LC VCO in presence of PVT variations. The 9-bit register is divided in two parts with different encoding: the first 6 MSBs have a thermometric encoding [4] while the last 3 LSBs are binary values. Therefore the total valid combinations are $7 \times 8 = 56$. Changing the thermometric value implies a broad output frequency variation while the binary codes are used for the fine tuning. An example of output frequency optimization, performed on the board 2 is shown in the Table 4.1 and represented in Figure 4.10.

vcoCapSelect 6-bit _ 3-bit	**vcoCapSelect code value**	**PLL clk frequency** (GHz)
000000_000	0	1.414 ± 0.005
000001_000	8	1.331 ± 0.005
000011_000	16	1.294 ± 0.005
000111_000	24	1.260 ± 0.005
001111_000	32	1.227 ± 0.005
011111_000	40	1.227 ± 0.005
111111_000	48	1.198 ± 0.005
000011_001	17	1.290 ± 0.005
000011_010	18	1.286 ± 0.005
000011_011	**19**	**1.283** ± 0.005
000011_100	**20**	**1.277** ± 0.005

Table 4.1: The vcoCapSelect tuning measurements: firstly a thermometric bits scan has been performed keeping the binary bits at the lowest value. Then, a fine scan has been done in order to center the VCO frequency at 1.28 GHz. The frequency measurements have been performed with the oscilloscope.

In Figure 4.11 the behavior of the locked PLL output $CLK_{1.28}$ is shown and compared to the input CLK_{160}. For this picture the persistence display mode has been activated, when this feature is enabled, the triggered traces overlap continuously on the display. The persistence can reveal occasional lock failures.

The lock frequency range of the PLL can be tested changing the input clock frequency and then checking if the Phase-Locked Loop (PLL) is still in the lock state. Board 2 and board 5 have a different lock frequency range. Indeed the former maintains the lock state in a 4 MHz range around the CLK_{160} while the latter board has a

[4] Thermometer code simulates the output produced by a thermometer. Therefore the number N is represented with the lowermost N bits at the high logic level while the others at the low logic level. Then, in order to move from N to $N+1$ it is necessary to change the rightmost '0' to '1'.

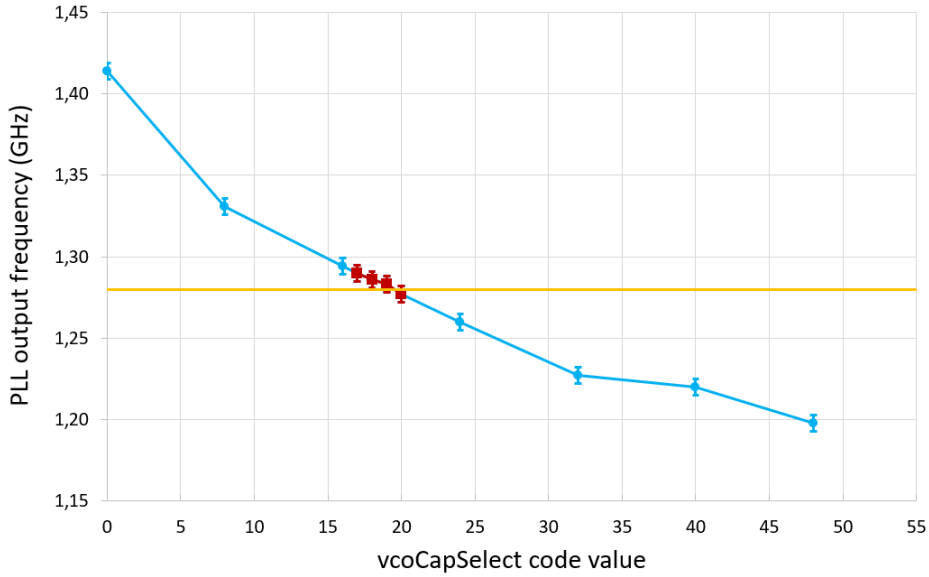


Figure 4.10: The PLL clock frequency as a function of the vcoCapSelect register code value. The measurements have been performed with the oscilloscope, the orange line is the required 1.28 GHz frequency, the cyan points represent the first step of the vcoCapSelect register tuning: from 000000_000 to 111111_000, while the red points are the frequency measurement during the fine tuning through the binary bits.

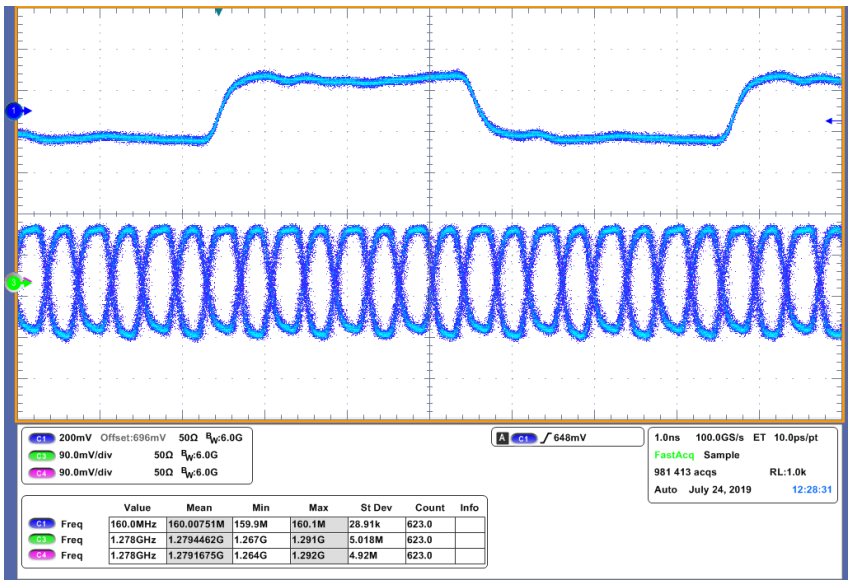


Figure 4.11: Oscilloscope screenshot of the 160 MHz clock on the channel 1 (top) and the PLL_{CLK} locked at 1.28 GHz channel 3 and 4 (bottom).

lock range of ∼1 MHz. In Table 4.2 the measurements performed on board 2 for the lock range evaluation are summarized. Raising or lowering the input clock frequency, the PLL output clock follows the frequency increase or decrease and remains locked to the reference clock.

input clock frequency	PLL output clok frequency
(158.00 ± 0.03) MHz	(1.263 ± 0.005) GHz
(159.00 ± 0.03) MHz	(1.272 ± 0.005) GHz
(**160.00 ± 0.03**) MHz	(**1.279 ± 0.005**) GHz
(161.00 ± 0.03) MHz	(1.287 ± 0.005) GHz
(162.00 ± 0.03) MHz	(1.294 ± 0.005) GHz

Table 4.2: The lock frequency range of the PLL integrated in the board 2.

PLL jitter measurements

Non-Idealities or bad design practices can result in an excessive jitter in the PLL output. The jitter is the time variation of the PLL output signal period [75] [96]. The jitter can be divided into two main classes as follows:

- the **random jitter** is also called gaussian jitter and it derives by stochastic events, e.g. coupling of electrical noise into the VCO input, the digital blocks of the PLL, or the CP architecture [96];
- the **deterministic jitter** is not intrinsic, it is an instantaneous frequency or phase change in the PLL output that can be due to a operation swap in the PLL or in the whole system. For example, a phase spurs in the PLL output can be seen when there is a mismatch in the CP block or when there is crosstalk due to an interfering periodic signal, or a simultaneous output switching [75].

The typical distribution of the random jitter is a bell shaped curve. However, in presence of an evident deterministic jitter source, the Gaussian distribution has a superimposed component which produces a skew in the distribution. The jitter distribution measured at the laboratory is shown in Figure 4.12. The jitter measurements have been performed with the *Jitter and Eye-Analysis Tool* of the oscilloscope [97].

The random jitter is about 1.3 ps while the deterministic jitter is almost 20 ps. The data converters with high sampling frequencies and high resolutions are more sensitive to external conditions as the clock timing quality. A poor quality of the clock applied to an ADC compromises its sampling performance and degrades the signal quality at the

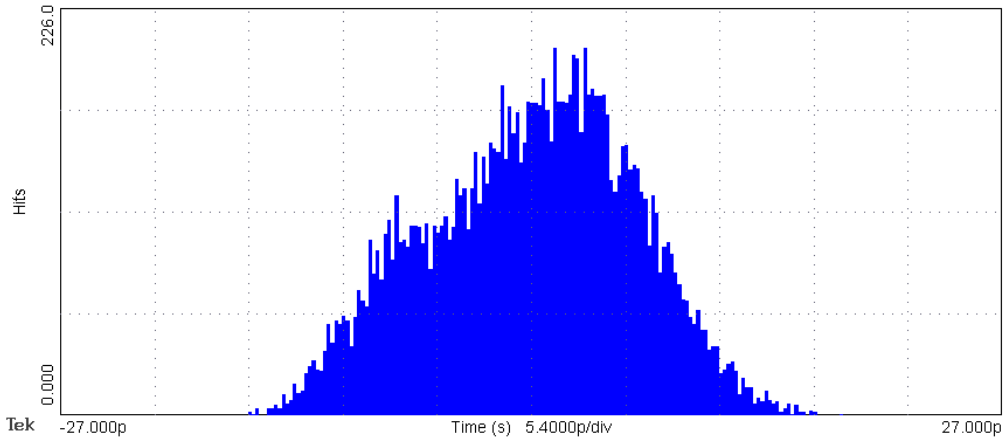


Figure 4.12: The jitter probability density curve measured with the oscilloscope. The distribution shape highlights both a random and deterministic jitter components. [75].

output of the ADC. Equation 4.1 provides the theoretical limit on SNR resulting from clock jitter, where f_{IN} is the input frequency and σ is the jitter of the sampling clock.

$$SNR\,(dB\,FS) \;=\; -20\,log(2\,\pi\,f_{IN}\,\sigma) \tag{4.1}$$

Therefore, the greater the input frequency the more susceptible the ADC is to jitter on the clock source. Indeed, for a 12-bit 160 MS/s ADC with a 30 MHz input signal, a good jitter target is 1 ps.

4.2.2 ADC and ATU characterization

The ADC performance studies have been preceded by the test on the ATU block along with the serializers. These tests have shown that both the ATU block and the serializers unit are working properly. In Figure 4.13, a slice of the four bit streams is shown, the ADCs in this case have no input and the only reference that they receives is the common mode voltage, V_{CM} = 600 V. Indeed, in output there are the 4-bit labels used for the bit streams alignment and sample reordering (see Section3.6) and the 12-bit ADCs samples that have a value near the middle of the FSR.

The serialization of the 32-bit words is correct and the TM_idle pattern is transmitted on the four output channels when there is a reset or the ADC calibration as shown in Figure 4.14. The four streams shown in Figure 4.13 are reported in Table 4.3. If the two's complement coding feature is activated the 12-bit samples become centered on the middle point of the full dynamic and the 12 bits can represent both positive and negative input values. The two's complement coding output are shown in Table 4.4.

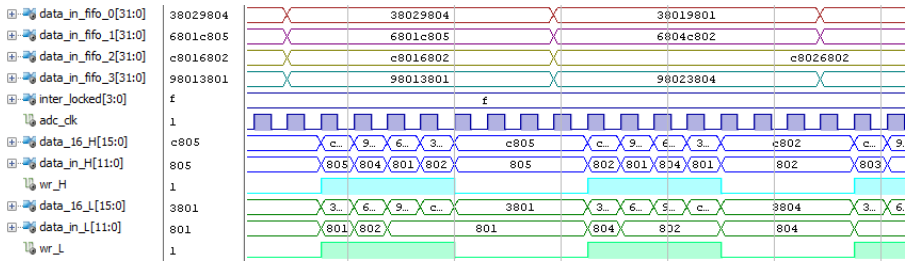


Figure 4.13: Vivado screenshot of the alignment method based on the 4 bits patterns (Figure 3.24) which alternate ADC samples during data transmission.

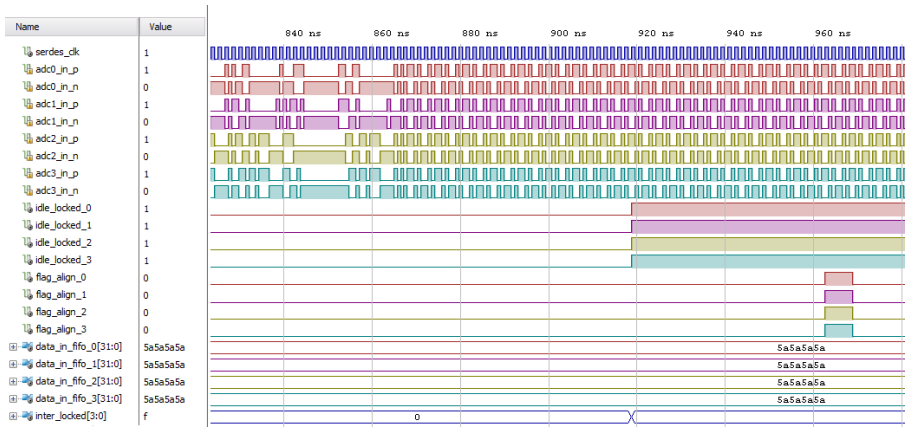


Figure 4.14: Vivado screenshot of the alignment method based on the idles pattern generated during the ADCs calibration.

dout_0	... **0011** 100000000010 **1001** 100000000100 **0011** 100000000001 **1001** ...
dout_1	... **0110** 100000000001 **1100** 100000000101 **0110** 100000000100 **1100** ...
dout_2	... **1100** 100000000001 **0110** 100000000010 **1100** 100000000010 **0110** ...
dout_3	... **1001** 100000000001 **0011** 100000000001 **1001** 100000000010 **0011** ...

Table 4.3: Slice of the four bit stream output with the ATU activated, there is no input signals to the ADCs which receive only the V_{CM}.

dout_0	... **0011** 000000000010 **1001** 000000000100 **0011** 000000000001 1001 ...
dout_1	... **0110** 000000000001 **1100** 000000000101 **0110** 000000000100 1100 ...
dout_2	... **1100** 000000000001 **0110** 000000000010 **1100** 000000000010 0110 ...
dout_3	... **1001** 000000000001 **0011** 000000000001 **1001** 000000000010 0011 ...

Table 4.4: Slice of the four bit stream output with the ATU and two's complement feature activated. There is no input signals to the ADCs which receive only the V_{CM}.

The software for the ADC characterization

The software employed for the analysis and the characterization of the ADCs has been written using C++ and ROOT [98]. The test methods described in *IEEE Std 1241TM-2010* [83] guidelines have been followed and the main approaches are the followings:

- **Fit method:** a 4 parameters sine wave fit is applied to the ADC samples which have to contain at least five cycles of the signal:

$$x[n] = A_0\, cos(2\,\pi\, f_0\, t_n) + B_0\, sin(2\,\pi\, f_0\, t_n) + C_0 \tag{4.2}$$

  Then the fit-sample residuals distribution is reconstructed and used to calculate the ENOB. The sine wave input has to be highly filtered in order to remove as much as possible the distortion and random noise from the input signal. The ENOB is calculated directly from the fit by computing the Noise and Distortion (NAD) and avoiding the direct calculation of the SINAD. Indeed, the SINAD parameter requires a good knowledge of the amplitude of the input signal which is not accessible due to the attenuation of the filter and the PCB components. Consequently the ENOB is given by:

$$ENOB = ln\,(\frac{FSR}{\sqrt{12}\,\cdot\, NAD}) \tag{4.3}$$

$$NAD = \sqrt{\frac{1}{M}\sum_{n=1}^{M}(x[n] - x'[n])^2} \tag{4.4}$$

  The input signal amplitude of between 90% and 100% of FSR should be used for this test. The input signal frequency and the number of the saved samples have been selected in a way that the phases sampled of the input signal are all different. Therefore, the input signal frequency f_{IN} has to be:

$$f_{IN} = \frac{J}{M}\, f_s \tag{4.5}$$

  where J is an integer which is relatively prime to M, M is the number of the samples and f_s is the sampling frequency [83].

- **Fast Fourier Transform method:** the Fast Fourier Transform (FFT) of the signal is computed using the *fftw 3* library [99]. Then, in the frequency domain, the ENOB, SINAD and other noise-related parameters can be measured.

- **Histogram method:** the ADC codes distribution is obtained by non-coherently

sampling the sine wave input. From this distribution, the transition voltages can be derived, and with them the DNL, INL and missing codes.

ENOB characterization at Adesto Laboratory

The study of the ENOB in the frequency range compatible to the specification range (up to 50 MHz) has been performed both in the INFN laboratory and at the laboratory of the *Adesto* company with the ADC IP block designers. The test setup used at the *Adesto* laboratory was nearly identical to the setup in Torino, except for a more precise signal generator and a pair of different bandpass filters. Since that, the study of the ENOB as a function of the input signal frequency is the result of the measurements performed at *Adesto*.

The test setup is shown in Figure 4.15 and it was composed by:

1. 2 LiTE-DTU boards: no. 2 and no. 5;
2. Two clock generators: *Stanford research system CG635*;
3. Clock splitter *Silicon Labs Si53301*;
4. Signal Generator: *Rhode & Schwarz*;
5. SMA RF cables for the input signal and the CLK_{160};
6. Power supplies:
   (a) *Keysight: E3646A*
   (b) *Hewlett packard: E3631A*
   (c) *Agilent: E3631A*
7. Bandpass filters:
   (a) *TTE P1116*: Q70T-500K-10P-50-720A, f_{in} = 500 kHz
   (b) *ALLEN AVIONICS INC*: BPS040P0-S, f_{in} = 10.7 MHz
   (c) *ALLEN AVIONICS INC*: BPS10P7S, f_{in} = 40 MHz
   (d) *TTE P1119*: Q70T-50M-10P-50-720A, f_{in} = 50 MHz
8. SMA / FMC transition board;
9. Logic-Level translator: *Texas Instruments* SN74AXC4T774EVM;
10. FPGA - Kintex UltraScale;
11. PC - OS: Windows 7, software: LabView.

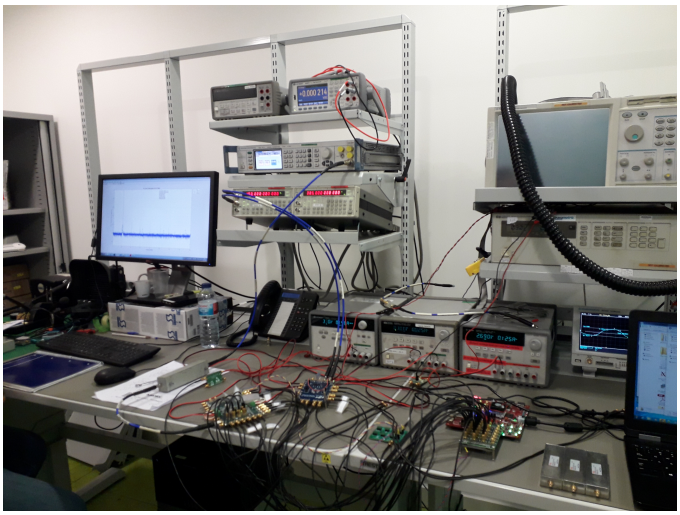


Figure 4.15: Setup used during lab test at Adesto.

It should be observed that the ADCs perform two types of calibration: the first is a calibration that use an internal reference to correct any mismatch between different capacitors, comparators, DNL, etc. This process need only the common mode voltage. The second calibration is for the inter-calibration between the two time interleaving ADCs. In this case, two external voltages are needed: V_{CAL_1} = 850 mV and V_{CAL_2} = 350 mV. These voltages are provided by the Agilent power supply. With the external voltages applied the average ADC counts is about 3754, which is in agreement to the value obtained from simulations.

The first measurement has been performed with the $CLK_{1.28}$ generated internally by the PLL and with a filtered sine wave signal with $f_{IN} \sim 50$ MHz. In the FFT of the output has been observed a spurious component at 10 MHz which is generated by a coupling with the input signal: $f_{IN} \pm f_{10\ MHz}$. The 10 MHz spurious has been removed by shorting the analog and digital grounds on the bottom layer of the PCB. The FFTs before and after the grounds coupling are shown in Figure 4.16.

A second spurious has been observed at 40 MHz, even when the input signal has been switched off. The only component in the LiTE-DTU ASIC that has the 40 MHz frequency is the PLL. Despite the possibility to feed the ADCs with the $CLK_{1.28\ ext}$, the PLL cannot be totally disabled because it sends the 1.28 GHz clock to the serializers. However, using the $CLK_{1.28}$ or the $CLK_{1.28\ ext}$, a different behavior of the 40 MHz spurs occurs. Indeed, when the high frequency clock is generated internally by the PLL, the 40 MHz spurious is coupled to the signal in input and two harmonics at $f_{IN} \pm f_{40\ MHz}$ are present. On the other hand, when the $CLK_{1.28\ ext}$ feeds the ADCs there is the main spurs at 40 MHz but the two coupling peaks there are no longer. A possible explanation

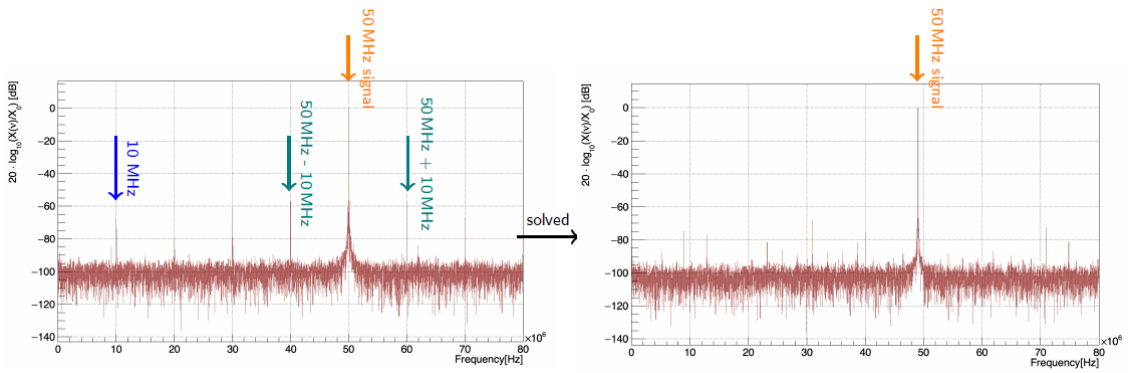


Figure 4.16: The FFT before (left) and after (right) the short between the two PCB grounds. The 10 MHz spurious peak is visible along with the two peaks due to the coupling of the 10 MHz with the input signal at $\sim$ 50 MHz.

is that the 40 MHz is somehow present in the substrate of the LiTE-DTU ASIC and its coupling with the input signal occurs.

The scan of the ENOB as function of the input signal frequency have been performed on board 5 on the low channel, both with the $\text{CLK}_{1.28}$ and $\text{CLK}_{1.28\ \text{ext}}$. The number of recorded samples per measurement has been set to 262140 (see Equation 4.5) and the used f_{IN} are: 498.04687 kHz, 10.71289062 MHz, 40.00976562 MHz, and 50.00976562 MHz. For each frequency a bandpass filter has been inserted between the signal generator and the SMA connector on the PCB board. The FFTs plots are shown in Figures 4.17, 4.18, 4.19, and 4.20. In the FFTs spectrum different peaks are visible:

1. it is the input signal peak;
2. it is the 40 MHz spurs;
3. it is a spurs due to a gain error between the interleaving ADCs and it is given by $f_s/2 \pm f_{IN}$: the interleaving spurious image on the upper end of the Nyquist band $f_s/2 + f_{IN}$ is folded on the $f_s/2 - f_{IN}$;
4. it is a spurs due to the coupling between the signal in input and the 40 MHz spurs: $f_{40\ MHz} - f_{IN}$;
5. it is a spurs due to the coupling between the signal in input and the 40 MHz spurs: $f_{40\ MHz} + f_{IN}$;
6. the remaining peaks are the odd harmonics of f_{IN}.

In Figure 4.19, several peaks are overlapped on the 40 MHz.

Aside from the presence of two harmonics at $f_{IN} \pm f_{40\ MHz}$ when the $\text{CLK}_{1.28}$ is used, another observation about the high-frequency clock jitter can be done looking to

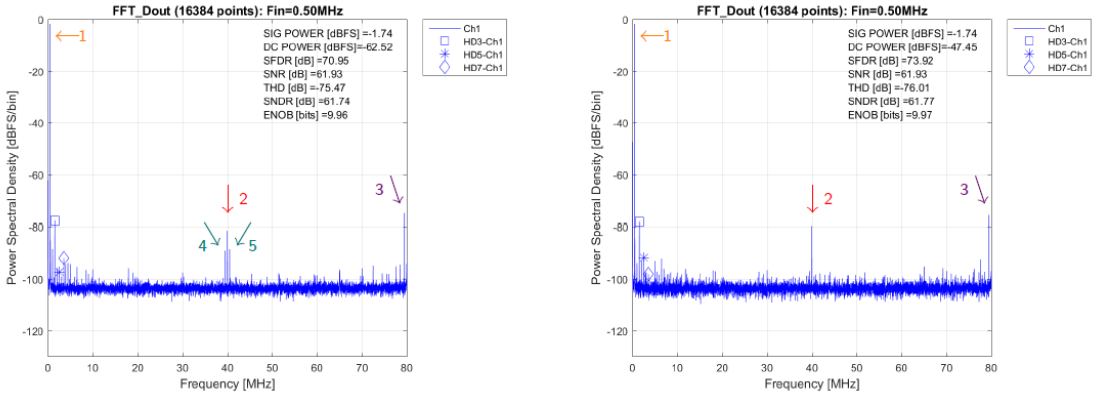


Figure 4.17: FFT with f_{IN} ~ 500 kHz and $CLK_{1.28}$ (left) or $CLK_{1.28\ ext}$ (right).

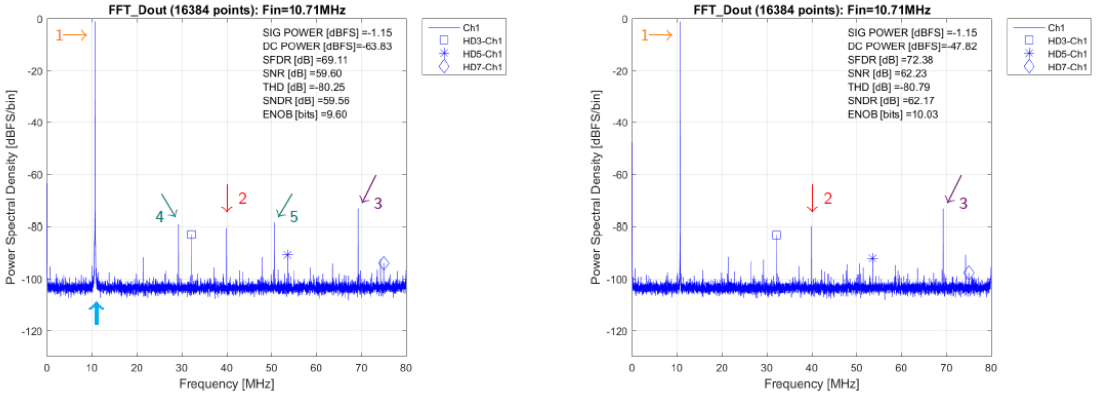


Figure 4.18: FFT with f_{IN} ~ 10 MHz and $CLK_{1.28}$ (left) or $CLK_{1.28\ ext}$ (right).

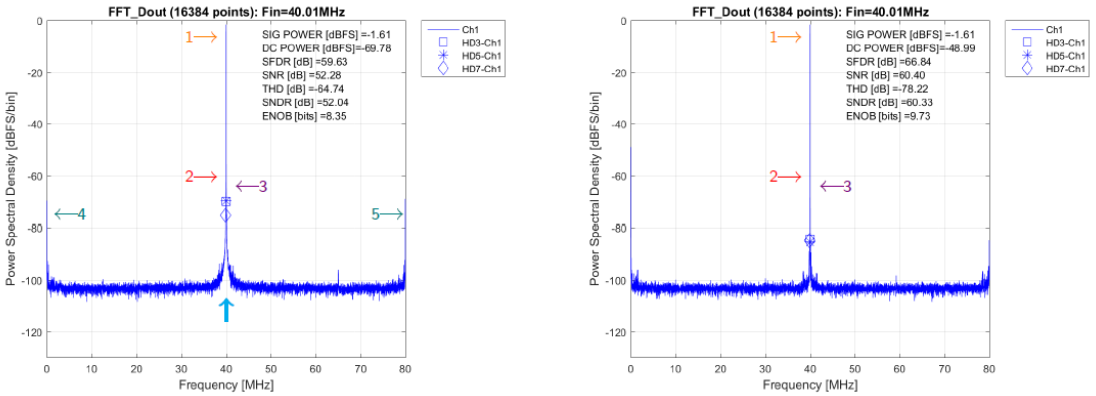


Figure 4.19: FFT with f_{IN} ~ 40 MHz and $CLK_{1.28}$ (left) or $CLK_{1.28\ ext}$ (right).

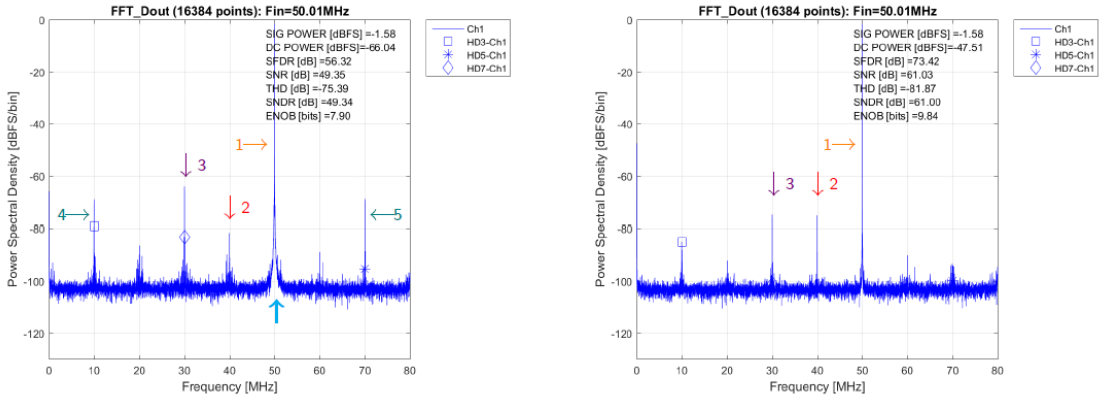


Figure 4.20: FFT with f_{IN} ~ 50 MHz and $CLK_{1.28}$ (left) or $CLK_{1.28\ ext}$ (right).

the previous FFT plots. The sampling with the $CLK_{1.28}$ is affected by the deterministic jitter of the PLL, which is ~ 20 ps (see Section 4.2.1) while the clock generator used for the $CLK_{1.28\ ext}$ has a much lower jitter: < 0.5 ps. The jitter influence can be observed in the FFT plots as a wide spread around the input frequency. The higher is the f_{IN} the wider is the jitter influence and hence the wider is the spread. In the FFT plots with the PLL clock this effect is highlighted by a light blue arrow at the bottom of the main frequency.

The ENOB as a function of the f_{IN} is shown in Figure 4.21. The results obtained by our analysis software are compared to the ones carried out by *Adesto* through a matlab code. The so called *Torino analysis* curves are a comprehensive outcome because the ENOB values obtained with the FFT and fit methods are compatible. On the other hand, the software employed by the *Adesto* company works in a different way with respect to the Torino software. The first is based on the FFT method but it performs an average of 16 FFT spectrum computed with 16384 samples each.

At 500 kHz the ENOB measurements are consistent to each other but they are slightly less then the requirement which is 10.2 in a frequency range from DC to 50 MHz. At the upper bound of the frequency range, the result obtained with the $CLK_{1.28\ ext}$ and the *Torino analysis* is 10.09 while *Adesto* quotes 9.84.

The frequency scan shows an ENOB trend almost flat around the 10 bits but there is a discrepancy between the measurements and the specification value. There are still some unforeseen spurious peaks that affect the results. The most influential are the spurs at 40 MHz and the spurs due to the gain error between the interleaving ADCs. Both of them are still unresolved despite the several attempts to reduce the coupling and to enhance the inter-calibration. Moreover, the internal clock generated by the PLL has a quite large component of deterministic jitter, which degrades as a function of the

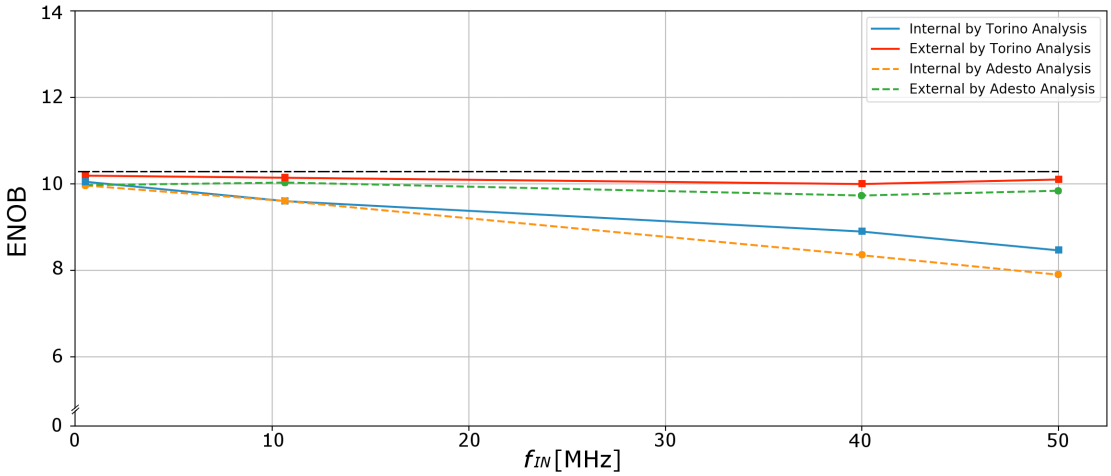


Figure 4.21: ENOB as a function the input signal frequency.

frequency. The $CLK_{1.28}$ jitter takes part to the reduction of the measured ENOB.

ADC calibration characterization

Several tests have been performed in order to enhance the ADC inter-calibration and hence reduce the gain spurious. *Adesto* suggested to change two configuration registers: ADC_CFG_REG0[0] = 1 and ADC_CFG_REG1[7:1] = 1111111. This change is done in order to activate the test mode of the ADCs and increase the number of samples used during the calibration process by a factor of 4. Multiple measurements have been performed both in normal configuration and in modified configuration, using the $CLK_{1.28}$ and the $CLK_{1.28\ ext}$. The input signals employed in this test were sine waves with f_{IN} = 500 kHz and 50 MHz, the results are shown in Figures 4.22, 4.23, 4.24 and 4.25. The blue and light blue markers in the plots represent the measurements performed after a normal calibration, with $CLK_{1.28\ ext}$ and $CLK_{1.28}$, respectively. The red and orange markers depict the measurement after the modified calibration, where the number of the samples employed is 4 times the default value. The red points are related to $CLK_{1.28\ ext}$ and the orange to $CLK_{1.28}$.

The ENOB results and inter-calibration spurs magnitude do not show a clear improvement in the calibration of the interleaving ADCs. Indeed, the magnitude of the spurious at $f_s/2$ - f_{IN} is still significant and it degrades the ENOB.

Another attempt has been done in order to try to reduce the harmonic distortion through the activation of the dithering. The dithering consists in summing a pseudo-random noise with the sine wave in input. The additional noise allows to randomize the ADC errors, the main consequence of the dither signal is to lower the spurious by

distributing the distortion components into several small spurs [100]. However, even in this case the inter-calibration spurs is still considerable therefore the gain mismatch between the two cores in the ADC is still to be fully understood.

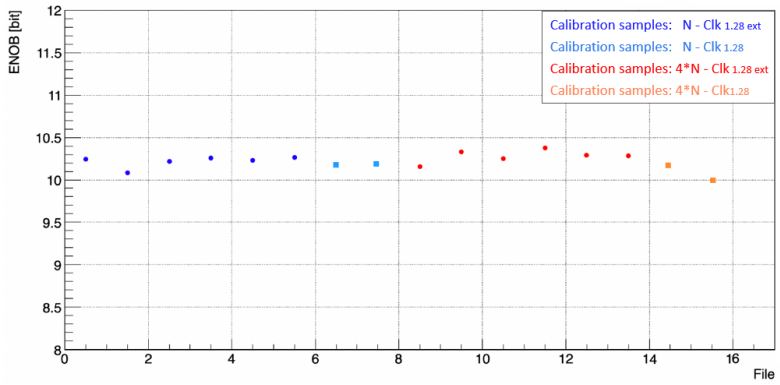


Figure 4.22: The ENOB for f_{IN} = 500 kHz.

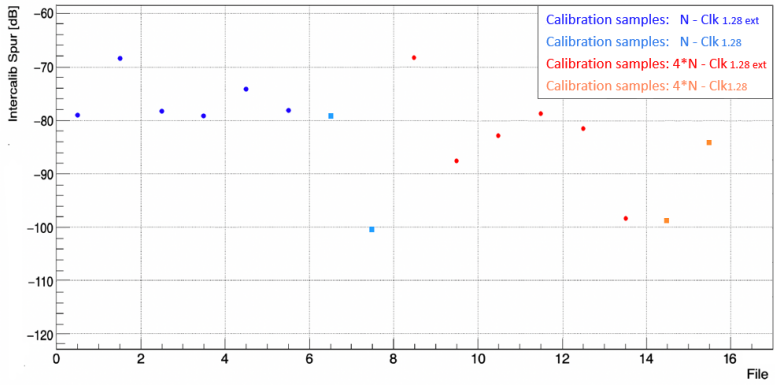


Figure 4.23: The inter-calibration spurs magnitude for f_{IN} = 500 kHz.

ADC linearity measurements

The study of the DNL and INL deviations have been performed feeding the ADCs with a sine wave produced by the *Teledyne* signal generator. The f_{IN} was equal to 500 kHz, the amplitude signal was adjusted to obtain the saturation of the FSR and the measurements have been performed with the $CLK_{1.28}$. The full dataset comprises about $7.8 \cdot 10^6$ samples acquired in 30 cycles and the calculation of the DNL and the INL have been performed after the gain and offset mismatch corrections.

The first check has been done on the ADC code density which is shown in Figure 4.26. From this plot appears that the ADC has some missing codes.

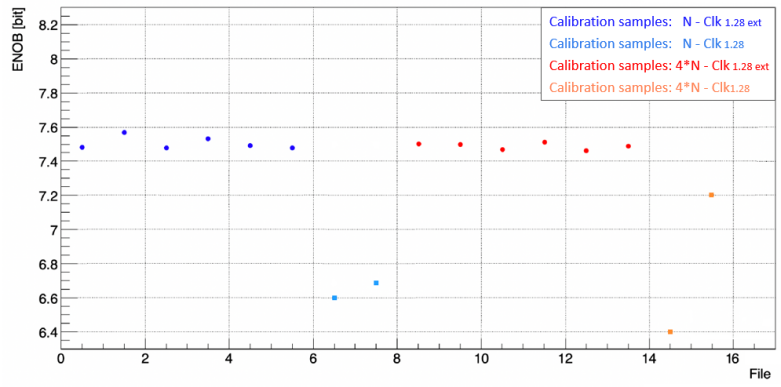


Figure 4.24: The ENOB for f_{IN} = 50 MHz.

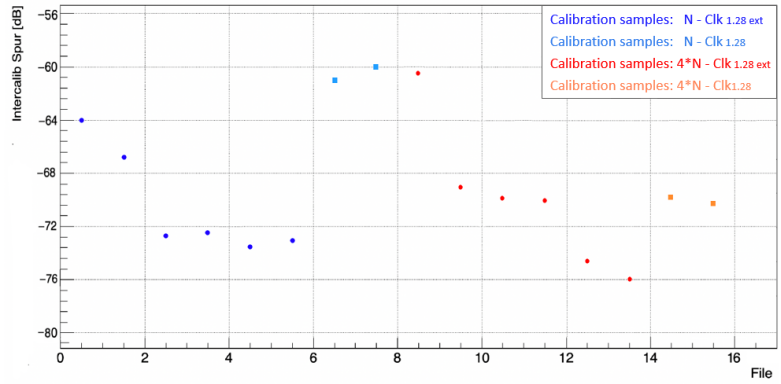


Figure 4.25: The inter-calibration spurs magnitude for f_{IN} = 50 MHz.

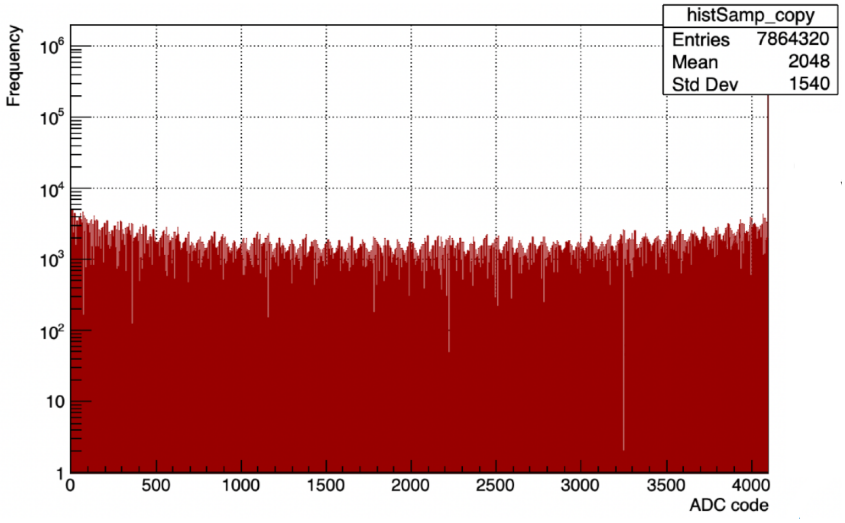


Figure 4.26: Distribution of the ADC codes.

The DNL and INL are shown in Figure 4.27 and Figure 4.28 respectively, the DNL seems to be ∼15% worse with respect to the requirements while the INL is in the range specified in the datasheet.

The observed missing codes and the disagreements between results and specifications can be due to the influence of the signal generator used in our setup. Indeed, another linearity measurement has been performed at CEA, Saclay and in that case there are no missing code observed.

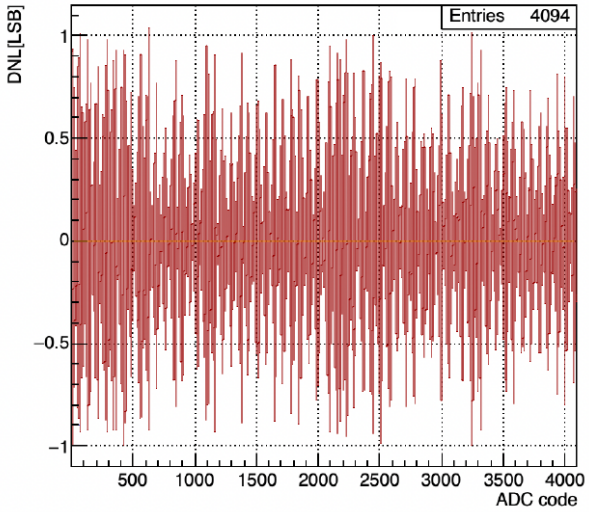


Figure 4.27: Distribution of the DNL deviation as a function of the ADC codes.

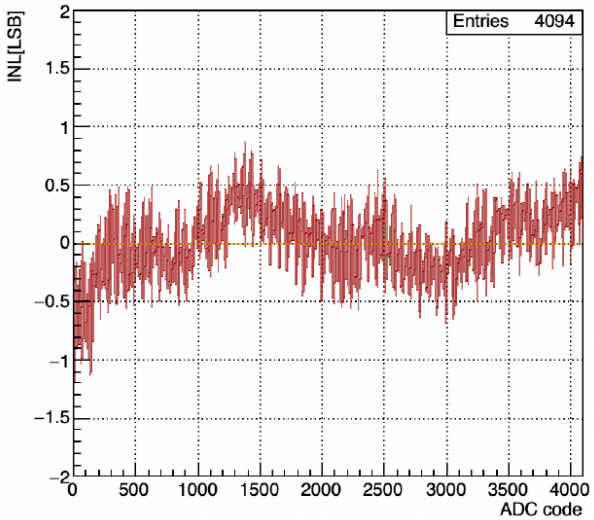


Figure 4.28: Distribution of the INL deviation as a function of the ADC codes.

4.2.3 DTU characterization

In contrast to the design phase, where the debug is straightforward because there are a lot of signals available in output during the test in the laboratory the only way is check accurately the bit stream in output.

After the typical start-up procedure, the PLL lock and the ADCs calibration, DTU block has been activated for the characterization. The switch between the ATU mode and the DTU mode is given by a jumper on the PCB. After the jumper switch, the serialized output change and the only output channel with samples is the dout_0 while the other three channels transmit always consecutive OM_idle patterns.

A sequence of pulses that have a voltage amplitude arranged to produce a saturation in the gain x10 channel has been given as the input of ADC_H. The SMA connectors for the ADC_L input have been left floating, in order to have a distinctive difference between the samples coming from the two channels. Indeed, the ADC_L receives the common mode voltage V_{CM} = 600 mV which produces a digital value centered around the middle of the FSR e.g. ∼2047 ADC counts.

This input choice has been done in order to check the correct operation of the sample selection and to cover all the possible 32-bit data types.

An example of output file is given in Table 4.5. For the sake of simplicity only some 32-bit words transmitted by the dout_0 and dout_1 are shown. The following features have been observed directly from the output data:

- The four data format are present (Figure 3.37) therefore both the switch between channels and between 6-bit and 13-bit samples are verified:
  - baseline word;
  - baseline incomplete word;
  - signal word;
  - signal incomplete word.
- the selection window length of the gain x1 samples in presence of a saturated sample in the gain x10 channel is verified and it is correct. A comparison of a pulse acquired both in ATU mode and in DTU mode is shown in Figure 4.29;
- The OM_idle pattern (Figure 3.47) is present and its occurrence is appropriate;
- The trailers are transmitted after the right number of 32-bit words. The 8-bit for trailer identification increments by a unit at each successive frame and the 8-bit counter of samples stores the right quantity of transmitted words (Figure 3.42).

dout_0		dout_1 / dout_2 / dout_3
01000000000011000010000001000000	,	01011010010110100101101001011010
01001011000110000111000100000011	,	01011010010110100101101001011010
01001111001011001111000101001000	,	01011010010110100101101001011010
01010100010001010010001111001111	,	01011010010110100101101001011010
11101010101010101010101010101010	,	01011010010110100101101001011010
01010111011000010111010000010010	,	01011010010110100101101001011010
01011101011111011110011011011001	,	01011010010110100101101001011010
01100101100011100011100000011111	,	01011010010110100101101001011010
01101010101010100110100011100100	,	01011010010110100101101001011010
11101010101010101010101010101010	,	01011010010110100101101001011010
01101011101110101010101010101010	,	01011010010110100101101001011010
01110101110010110010101110101100	,	01011010010110100101101001011010
11011111111110000000111110011111	,	01011010010110100101101001011010
01000011001000000101000010000011	,	01011010010110100101101001011010
01000001100100000010000001000100	,	01011010010110100101101001011010
01000000000011000010000001000000	,	01011010010110100101101001011010
01001011000110000111000100000011	,	01011010010110100101101001011010
01001111001011001111000101001000	,	01011010010110100101101001011010
01010100010001010010001111001111	,	01011010010110100101101001011010
11101010101010101010101010101010	,	01011010010110100101101001011010
01000000000011000010000001000000	,	01011010010110100101101001011010
00101000000010000100000001000001	,	01011010010110100101101001011010
00101101010101010100000001000110	,	01011010010110100101101001011010
10000001000000000000000000111110	,	01011010010110100101101001011010
00101011000000000101100000000000	,	01011010010110100101101001011010
00101011000000000011100000000000	,	01011010010110100101101001011010
00101011000000000011100000000000	,	01011010010110100101101001011010
00101011000000000011100000000000	,	01011010010110100101101001011010
00101101010101010100000001000100	,	01011010010110100101101001011010
01101010101010100110100011100100	,	01011010010110100101101001011010

Table 4.5: A portion of the LiTE-DTU output in DTU operational mode. The 32-bit data words are serialized at 1.28 Gb/s on the dout_0 channel while the other three output transmit continuously a sequence of OM_idle patterns.

In Figure 4.29, the output acquired in ATU operational mode is compared to the output obtained with the DTU mode. In the former plot both the ADC_H and ADC_L samples are shown. As expected, the ADC_H contains the pulse signal while the ADC_L samples are stable around the ADC counts of the V_{CM}. In the latter plot the majority of the output samples are transmitted through baseline packets, indeed their value is below

the threshold of the 64 ADC counts. The remaining samples have been transmitted by 4 consecutive 32-bit signal packets: they are the result of the channel selection switch due to a saturated sample in the gain x10 channel. The selection window is correctly centered and it has a proper length. Moreover, the samples have been rightly selected from the gain x1 channel, the transitions from gain x10 to gain x1 and vice versa have been handled by the encoder in the right way.

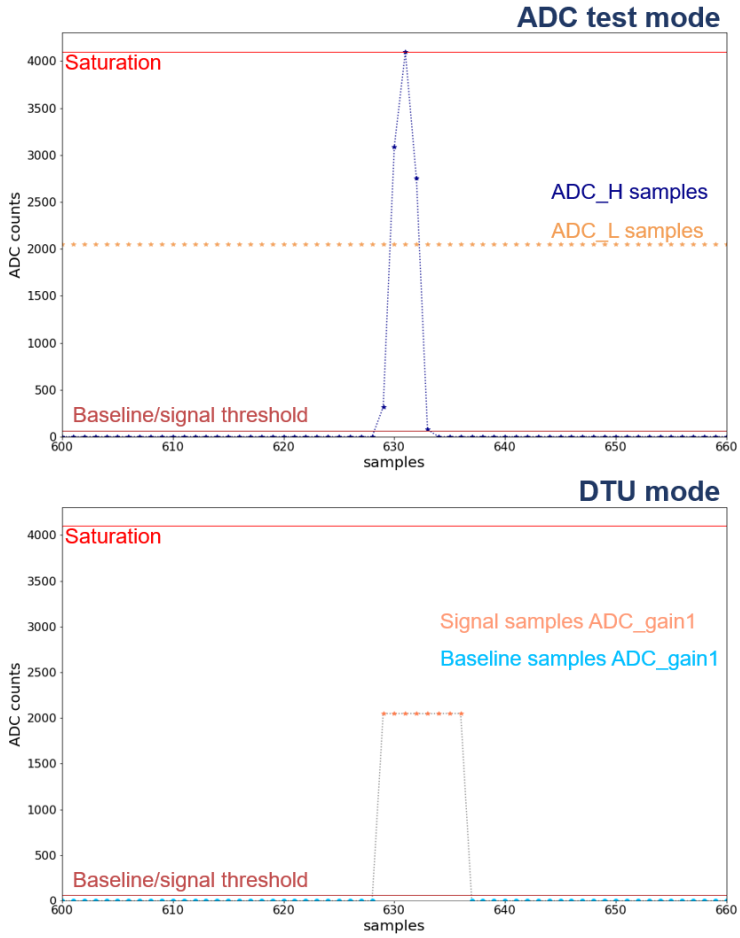


Figure 4.29: Example of direct measurement of a pulse with the LiTE-DTU in ATU mode (top) and in DTU (bottom). There is a saturated sample in the gain x10 channel, thus 8 samples coming from the gain x1 channel are selected and transmitted.

4.3 Summary

In this chapter, the experimental setup employed for the LiTE-DTU characterization has been presented. Unfortunately the number of fully working ASIC mounted on the first batch of PCBs was limited. Indeed, at the beginning of the tests a misbehavior of the I^2C interface has been detected.

Despite this issue, it has been possible to perform several tests on the board no. 2 and no. 5 and the diverse blocks integrated in the first prototype have been fully characterized.

The PLL has shown a low value of random jitter but there is a broad deterministic component affecting the total jitter. Therefore, during the ADC test phase both the internal clock generated by the PLL and the external clock have been used.

Concerning the ADC IP block, the result of the ENOB as a function of the input signal frequency looks very promising. However, there are some concerns about the 40 MHz spurs and the spurious tone due to the slightly inaccurate inter-calibration of the ADC interleaving cores. A series of tests have been done in order to obtain a more precise calibration, such as the increase of samples employed for the calibration or the removal of the dithering noise to the input signal. Unfortunately the changes have not contributed to significant improvement in the inter-calibration procedure.

Lastly, all the digital blocks, such as the ATU, the DTU and the serializers have shown a good behavior and have performed to specifications. Indeed there is satisfactory agreement between the results obtained in the laboratory and the simulations both in ATU and in DTU operational modes.

Chapter 5

Radiation damage test

The LiTE-DTU ASIC is designed to be placed close to detector therefore several radiation-hard design techniques have been implemented in the chip. In Chapter 3, the fault tolerant strategies employed during the LiTE-DTU design phase have been described in details. Considering the harsh radiation environment foreseen for Phase-2, both the total ionizing dose effects on the ASIC performance and the exposure to data corrupted by SEU need to be addressed.

In the earlier part of this chapter, an introduction about the radiation effects on integrated circuits is presented. Then, the TID and SEU qualification tests performed on the first prototype of the LiTE-DTU ASIC are reported along with the results.

5.1 Radiation effects on IC

When a particle hits an electronic device, it deposits energy in the IC, and as a consequence, several different issues can arise: memory bits corruption, glitches in both analog and digital circuits, speed degradation, and increment in power consumption. Lastly, in the most serious cases, a device can lose reliability and its own functionalities. In order to obtain a reliable electronic system and ensure its correct functionality, the operational environment of the device must be taken into account, therefore the radiation effects have to be considered.

There are three main categories of radiation effects: Total Ionizing Dose (TID), Displacement Damage (DD) and Single-Event Effect (SEE). TID and DD are effects due to the continuous hits by particles which entails a degradation of semiconductors and insulators materials, and as a consequence a progressive drift of the IC parameters. On the other hand, SEEs are a stochastic process and are generated when an high energy ionizing particle hits a sensitive region of an electronic system. The TID uniformly affects

the entire device therefore it is characterized by the drifts of the main device parameters. On the other hand, SEE affects only the particle strike spot therefore the sensitivity of a device to single events is determined by the rate of occurrence as a function of the deposited energy.

5.1.1 Cumulative effects: DD and TID

The DD is bulk effects, it occurs when an high energetic impinging particle interacts with the atoms in the silicon lattice, typically through a scattering process, and it causes a displacement of an atom from its lattice position [101]. The displaced atom can cause secondary collisions with other atoms while the nominal lattice points left by the atoms become a vacancy [102]. The crystal lattice damage generates changes of the electrical properties of the device. The DD is a long-term damage and it appears as the increase of the leakage current and of the charge trapping process [103].

Considering CMOS technologies, the DD is not as severe as the TID effects since in these technologies the conductive channel is on the surface only and therefore the volume sensitive to displacement is very small [104]. The TID is a long-term effect due to the exposure of the device to ionizing radiation. TID is the total energy transferred by ionization processes in the device, it is measured in gray: Gy = $\frac{J}{kg}$.

The ionization damage is a surface effect due to the interaction of X-rays, γ-rays and charged particles with an electronic devices. The damage occurs when an ionizing radiation passes through the oxide layer of the device, deposits its energy and ionizes the atoms in the lattice. This process creates free charge carriers, electron-hole pairs, along the track of the impinging particle. The majority of the pairs recombines, while the remaining electrons drift to the anode and the holes goes trough the oxide in the opposite direction [102]. The electrons have an higher mobility in comparison with the holes mobility. The former are pulled away from the oxide over a period of time of the order of picosecond [5], while the latter take a few seconds to move through the oxide. The holes migration is a hopping transport through localized traps in the oxide towards the Si/SiO_2 interface. Then, the holes that manage to reach the interface may be trapped in long-term defect sites due to the interstitial oxygen. The charge accumulated in the interface region causes multiple consequences at transistor level, e.g. increase of leakage current and shift in the threshold voltage, and secondary implications at circuit level, e.g. power increase and timing degradation.

The annealing of the trapped holes in the oxide and in the interface is due to a tunneling or thermal detrapping processes. In the former, the holes can be neutralized

[5] For a typical gate oxide layer thickness $\leq$ 100 *nm* and operating fields > 10^5 V/cm [105].

by electrons that pass through the oxide barrier, therefore thinner potential barriers allow to faster annealing. In the latter, the thermally excited electrons can neutralize the trapped holes, thus a faster annealing is enabled by higher temperatures and shallower traps [102]. The annealing starts immediately but it is not instantaneous, actually the radiation-induced effects can last for a period of some seconds to several years.

However, during the extensive radiation campaign on the 65 nm technology [106], an unforeseen behavior in contrast to the annealing has been reported. The reverse annealing is a significant performance degradation connected to the oxide spacers used to implant the LDD regions[6]. Therefore, a shrunk technology ASIC must be characterized over long time periods after the TID irradiation in order to monitor the potential presence of the reverse annealing.

5.1.2 Single-Event Effect

The SEE is the consequence of the interaction of a highly-energetic single proton or heavy ion with a sensitive device region. SEEs are typically characterized in terms of their cross section σ_{SEE} defined as the ratio between the number of observed upset events and the particle fluence (particle / cm^2). The cross section si a function of the Linear Energy Transfer (LET) of the impinging particle. The SEEs are distinguished among destructive or hard-error and non-destructive or soft errors [102].

The destructive errors are Single-Event Burnout (SEB), where the particle strike causes a localized high-current state that results in a failure, Single-Event Gate Rupture (SEGR), in this case the result is the gate oxide degradation, and the Single-Event Latch-up (SEL) which provokes an overcurrent and, if not mitigated by turning off the power supply, a burnout.

The non-destructive errors do not induce any physical damage, however, they typically cause a loss of information. The soft errors are recoverable by forcing the power shut down, reset or rewriting the corrupted memory, but a low rate of failures is desirable in order to obtain a reliable device. In the category of soft errors there are: Single-Event Transient (SET), Single-Event Upset (SEU) and Multi Bit Upset (MBU).

The SET is a transient signal change induced in a combinatorial or analog part of the device. The SEU is a bit-flip of a sequential element such as a flip-flop or a memory due to the energy deposition in a digital cell. The MBU is a multiple SEU process. It has become more likely as the technology size has been scaled down, indeed with the old technologies the process was confined to a single node while with modern ones SEE

[6]The Lightly-Doped Drain (LDD) regions are deposited next to the channel in order to reduce the electric field responsible for hot-carrier degradation [106].

can involve multiple nodes.

5.2 TID characterization of the LiTE-DTU

The TID testing is commonly performed using radioactive sources, such as cobalt 60 (^{60}Co) and cesium 137 (^{137}Cs). The ^{60}Co is the most used radioactive source, it has a half-life period of 5.27 years and emits two γ photons at 1.173 MeV and 1.333 MeV, while the ^{137}Cs has a half-life period of 30 years and emits two β-rays at 0.51 MeV and 1.17 MeV and a γ photon at 0.662 MeV.

However, the X-ray [7] generating machines have become widely approved for TID tests, in particular when the required total dose values are in the range of hundreds of kGy and for low X-ray energy (10 keV).

The LiTE-DTU has been irradiated at the X-ray facility at INFN Padova. The X-ray machine that has been used is the *Seifert RP-149 Semiconductor Irradiation System* supplied with a standard tube for X-ray diffraction analysis. The tube is placed inside a shielding cabinet, it collimates the X-rays in order to directed the beam towards the sample and it can be moved along the x, y (mechanized) and z (manual) axis. In Figure 5.1a and 5.1b the X-ray machine is shown along with the LiTE-DTU and the test setup.

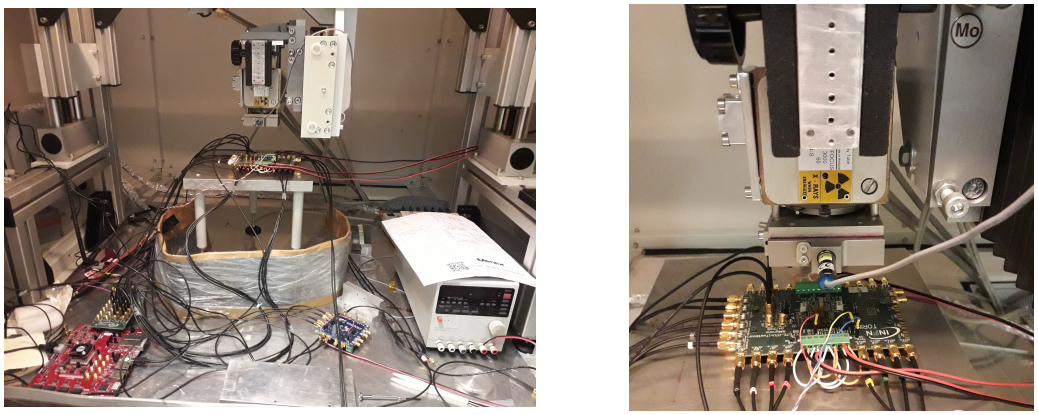
Only the LiTE-DTU placed on the board no. 5 has been exposed to the X-ray beam. The chip has been irradiated without the protective aluminum lid to avoid any photon absorption. The beam spot matched the dimensions of the chip, thus all the other components placed on the PCB were not irradiated.

Unfortunately, after the power-on of the chip an issue on the PCB has been found: during the transportation of the board a soldered resistance connected to the RESYNC+ has been detached. This issue did not allow to properly lock the PLL but it has been decided to proceed with the measurement by restricting the quantity of information.

The X-rays energy has been set to 10 keV and the chip has been irradiated up to 50 kGy with the following total dose steps: 5 kGy, 10 kGy, 20 kGy, 30 kGy, and lastly 50 kGy. At the end of each run the analog, digital and drivers currents were readout in order to monitor the ASIC consumption, Table 5.1 summarizes the measurements.

The ASIC behavior has been stable during the X-ray test, the current levels have

[7] X-rays are generated when an accelerated electron beam interacts with the orbital electrons or nucleus of the target atoms. The target usually is an high-Z metal such as copper or tungsten. The X-rays are generated when the electrons decelerate in the metal, the energy released during the interaction is known as X-radiation. There are two atomic processes that can produce X-ray photons: the Bremsstrahlung and the K-shell emission.



(a) (b)

Figure 5.1: Experimental setup at the X-ray facility at INFN Padova (left) and the LiTE-DTU ASIC, board 5, under X-ray irradiation (right).

Run	X-ray dose [kGy]	Duration [mm:ss]	Analog [mA]	Digital [mA]	Drivers [mA]
0	-	-	26	130	115
1	5	10’ 45”	26	136	115
2	10	10’ 45”	26	131	115
3	20	21’ 30”	26	137	115
4	30	21’ 30”	26	135	115
5	50	43’ 00”	26	137	115

Table 5.1: Current measurements during the X-ray irradiation runs at Padova.

not highlighted significant drifts on the analog and drivers currents. A mild drift in digital consumption has been observed: after an irradiation corresponding to 50 kGy, the maximum deviation from the starting value before irradiation is about 5 %. However, the produced degradation by radiation lies within an adequate range considering that the TID requirement is 20 kGy (see Section 3.1) and during the test the reached level of total dose delivered has been 50 kGy.

A couple of days after the X-ray irradiation, the ENOB scanning in frequency has been repeated in order to compare the performances before and after the irradiation. The scan has been performed on the frequency range between 500 kHz and 50 MHz, using the $CLK_{1.28}$ generated by the PLL. In Figure 5.2 the two ENOB trends as a function of input signal frequency are shown.

The performance of the ASIC before and after the irradiation are comparable, moreover in the successive months no degradation has been observed during the performed

measurements on the board no. 5. Indeed, this board has been used also for the characterization measurements in Lisbon at the *Adesto* laboratory and for the SEU test in Louvain-La-Neuve. Looking at the ENOB measurements obtained at the *Adesto* laboratory (see Section 4.2.2) the ENOB curves before and after the TID irradiation are shifted down to lower values along the full range of f_{IN} but it is clearly visible at higher frequencies. The lack of agreement is due to the wrong ADC calibration, in fact the applied reference voltages were V_{CAL_1} = 900 mV and V_{CAL_2} = 400 mV instead of V_{CAL_1} = 850 mV and V_{CAL_2} = 350 mV.

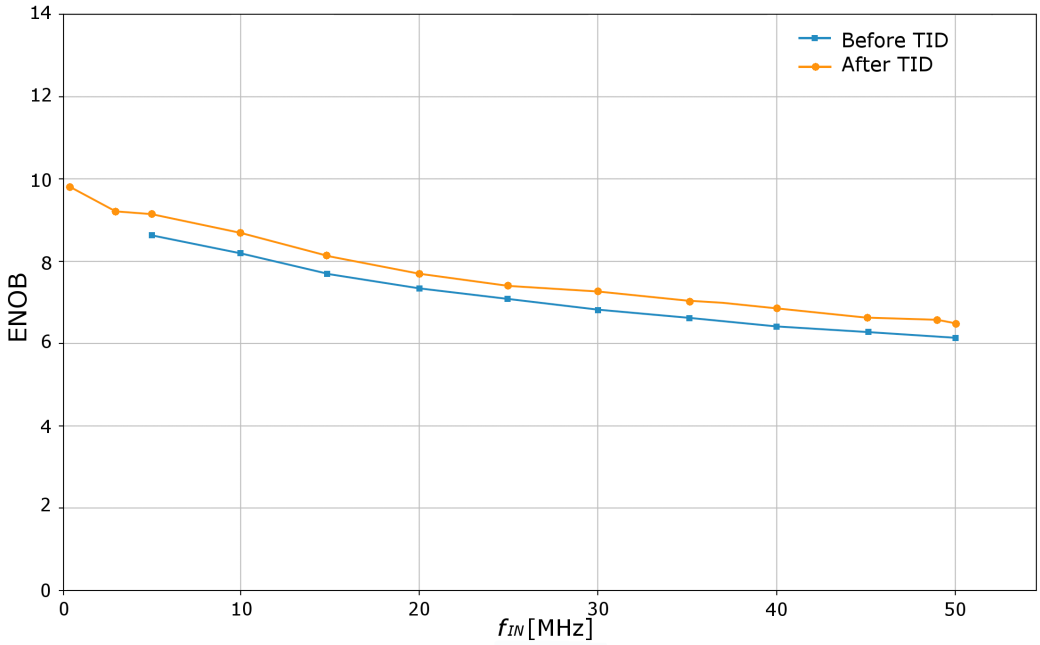


Figure 5.2: ENOB measurements on the board no. 5 before and after the X-ray irradiation at Padova.

5.3 SEU characterization of the LiTE-DTU

In order to fully characterize the LiTE-DTU, two SEU tests have been performed. The first one at National Center of Oncological Hadronterapy (CNAO) in Pavia using proton beam and the second one at Heavy Ion Facility (HIF) in Louvain-La-Neuve with four different ion beams.

In order to study the SEU sensitivity of a device, the heavy ions irradiation tests are more convenient when compared to proton irradiation, because heavy ions feature a charge (Z) greater than unity and at high energies the LET scales approximately as

Z^2 [107]. Moreover, the proton SEUs are mainly caused by an indirect interaction in contrast with the upsets induced by heavy ions. The majoity proton SEUs are generated via ionization of recoiling heavy ions produced by a nuclear reaction with the materials in the device. However, an increased sensitivity to SEU induced directly by a proton has been reported for devices with shrunk technology node [108].

5.3.1 SEU test setup

The experimental setup used to test the radiation hardness of the LiTE-DTU ASIC consisted in a similar setup used in INFN Torino Laboratory. The main difference is that the LabVIEW software has been customized in order to count the occurred SEU. Moreover, for the measurements at the HIF facility, the measurement setup was more complex because the ASIC has to be placed in a vacuum chamber, due to the short mean free path of the heavy ions in air.

A dedicated LabVIEW software has been implemented in order to count the number of occurred SEU on the ADCs I^2C configuration registers. The total number of configuration registers is 76 and each one is 8-bit long therefore the total number of bits is 608. The radiation hardness of these registers has been evaluated by writing, reading, and then checking the received words with the one previously sent. Bytes with a balanced number of 0 and 1 have been written in the configuration registers and readout every 5 s. If there is a match between the two sequence of commands, a "no errors" message is written on the log file while when at least a bit-flip due to a SEU is detected both the written command and the corrupted word are saved for offline data analysis. The DAQ system calculates the number of occurred bit-flip and continuously update the plots in the GUI. The two possible transitions due to an upset are considered separately: 0→1 and 1→0, these transitions have different probabilities while, as reported above, the configuration registers receives balanced commands.

Moreover, the contents of ADC0 FF_register, ADC1 FF_register, SEUA signal, and SEUD signals have been monitored. The first two registers contains the value of two SEU counters embedded in the LiTE-DTU design while the SEUA and SEUD are two SEU outputs of the analog and digital LiTE-DTU blocks, respectively. Figure 5.3 shows the SEU DAQ GUI, on the left there are the counter plots while on the right side there are some settings buttons and the output console.

5.3.2 SEU test at CNAO

CNAO is an Italian center for the treatment of tumors with hadrons [109]. Carbon ion beams and proton beams are generated by a ionized plasma source exposed to magnetic fields and radio frequency pulses. After that the particle beams are accelerated by

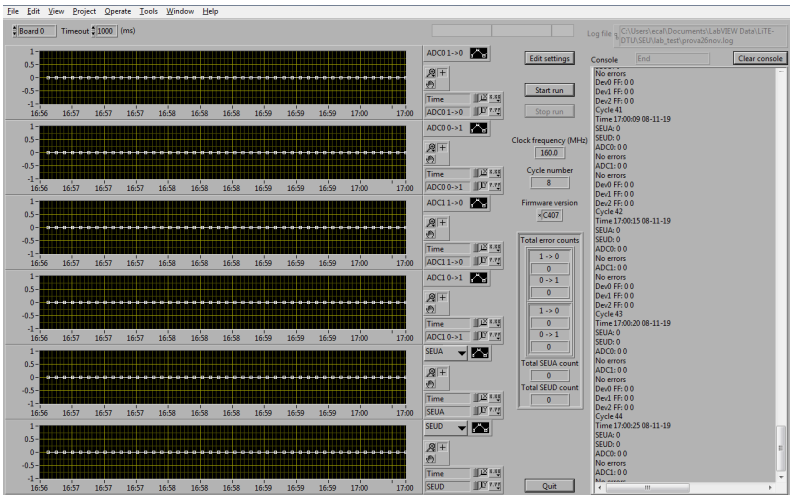
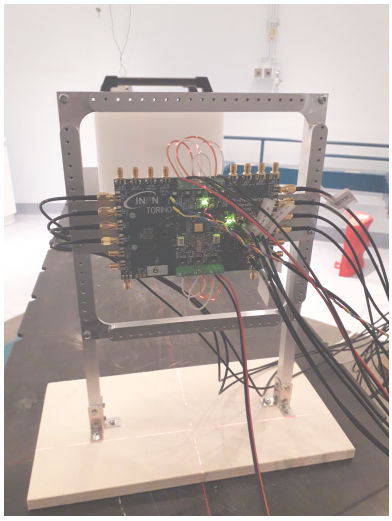


Figure 5.3: GUI of the DAQ system for the SEU test.

the synchrotron, a circular accelerator with a diameter of 25 m. The maximum energy reached by protons is 250 MeV while carbon ions can reach 480 MeV. Then the beam can be guided to one of the three treatment rooms where a magnet bends the beam and focus it on the target. In Figure 5.4a, the experimental setup in the treatment room before the LiTE-DTU irradiation is shown. The PCB has been fixed to a metal plate holder and positioned on the treatment bed as can be seen in Figure 5.4b.

(a)



(b)

Figure 5.4: Experimental setup at CNAO (left) and LiTE-DTU ASIC before proton irradiation (right).

The beam flux values have been continuously monitored by the facility operators,

the DAQ allows automatic runs with user predefined irradiation criteria. The irradiation test has been carried out in the following conditions:

- beam: protons with energy = 226 MeV;
- irradiation in air and at room temperature;
- beam profile: gaussian form, the fraction of proton on the chip is 20%;
- total duration of irradiation: $1.75 \cdot 10^4$ s (almost 5 hours);
- total number of irradiated protons: $4.95 \cdot 10^{12}$;
- total number of protons on the chip area: $9.9 \cdot 10^{11}$;
- proton rate on the chip area: $5.67 \cdot 10^7$;
- flux: $1.42 \cdot 10^9$ protons/ s cm^2;
- fluence: $2.47 \cdot 10^{13}$ protons/ cm^2;
- LET$_{proton}$ = $1.67 \cdot 10^{-3}$ MeV cm^2 / mg.

The runs performed during the irradiation are summarized in Table 5.2. During the whole data acquisition no upset has been observed.

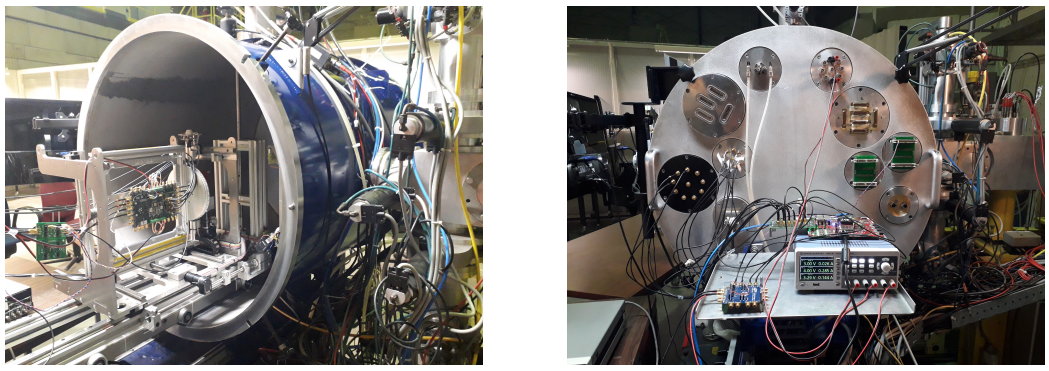
Run	**Duration** [mm:ss]	**N proton**	**N proton on chip**	**SEU**
1	00:06	$1 \cdot 10^{11}$	$2 \cdot 10^{10}$	0
2	00:14	$2.25 \cdot 10^{11}$	$4.5 \cdot 10^{10}$	0
3	00:14	$2.23 \cdot 10^{11}$	$4.45 \cdot 10^{10}$	0
4	00:24	$4 \cdot 10^{11}$	$8 \cdot 10^{10}$	0
5	00:25	$4 \cdot 10^{11}$	$8 \cdot 10^{10}$	0
6	00:24	$4 \cdot 10^{11}$	$8 \cdot 10^{10}$	0
7	00:23	$4 \cdot 10^{11}$	$8 \cdot 10^{10}$	0
8	00:23	$4 \cdot 10^{11}$	$8 \cdot 10^{10}$	0
9	00:23	$4 \cdot 10^{11}$	$8 \cdot 10^{10}$	0
10	00:23	$4 \cdot 10^{11}$	$8 \cdot 10^{10}$	0
11	00:23	$4 \cdot 10^{11}$	$8 \cdot 10^{10}$	0
12	00:23	$4 \cdot 10^{11}$	$8 \cdot 10^{10}$	0
13	00:23	$4 \cdot 10^{11}$	$8 \cdot 10^{10}$	0
14	00:23	$4 \cdot 10^{11}$	$8 \cdot 10^{10}$	0

Table 5.2: List of measurements made at CNAO.

5.3.3 SEU test at HIF

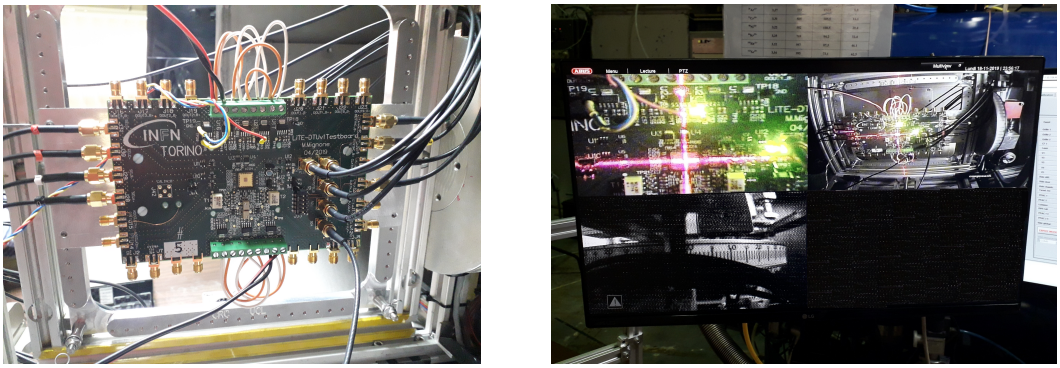
The second test has been performed at the HIF of UCLouvain (Université Catholique de Louvain) in Belgium. The HIF facility allows to use heavy ions accelerated by a cyclotron in order to characterize electronics devices. The beam flux can be chosen between few particles/(s cm^2) up to 1.5×10^4 particles/(s cm^2). During the irradiation, the flux is integrated in order to give the delivered total fluence on the device. The beam flux can be modified by the operator as well as the selected ion specie. The beam parameters are controlled by a dosimeter box placed in front of the chamber. The beam flux homogeneity is $\pm$ 10 % on a 25 mm diameter and its measurement is performed with a collimated surface barrier detector. The full list of the available particles can be found in the HIF website [110].

The LiTE-DTU PCB has been mounted on the metal plate holder which is positioned on a mechanical slide that allows to insert the target inside the vacuum chamber. In Figure 5.5a, the cylindrical vacuum chamber with the slide and the metal plate holder are shown. The power supply, clock generator, clock splitter and FPGA have been positioned on a desk next to one of the vacuum chamber endcap, as can be seen in Figure 5.5b. Consequently, all the cables have to be coupled to the connectors on the flanges present on the vacuum chamber endcap in order to supply and communicate with the ASIC inside the chamber. In Figure 5.6a the LiTE-DTU board no. 5 fixed to the holder is shown, the lid of the ASIC package has been removed in order to expose the 2×2 mm^2 silicon area to the beam. Figure 5.6b shows the remote calibration of the beam position on the target that have been performed before the start of measurements.



(a) (b)

Figure 5.5: The vacuum chamber open with the slide, the metal plate and the LiTE-DTU mounted on it (left). Vacuum chamber endcap with flanges for cable connection between the clock generator, power supply, and DAQ system (outside the chamber) and the ASIC (right)



(a) (b)

Figure 5.6: PCB board with LiTE-DTU, with no package lid, mounted on the metal plate holder before the irradiation (left). The webcam view of the LiTE-DTU ASIC in the vacuum chamber during the position calibration of the beam spot on the target (right).

Four heavy ions have been used in 9 runs with different flux and fluence: Krypton (Kr), Xenon (Xe), Nickel (Ni), and Chromium (Cr). The ions characteristics are reported in Table 5.3 while in Table 5.4 the different irradiation runs are summarized.

The experimental cross section of the device is defined as $\sigma_{SEU} = N_{SEU} / (\phi \times N_{bit})$, where N_{SEU} is the number of observed upsets, ϕ is the particle fluence and N_{bit} is the total number of bits that can be involved in the SEU. In Table 5.3 there are two cross sections: σ_{reset} and σ_{SEU}. The former is referred to the transitory errors that have provoked a bit-flip of hundreds of cells simultaneously, this error has been associated to a SEU that has involved a sensitive node in the reset network. The latter is the cross section referred to a single bit-flip.

Ion	M / Q	Energy on device [MeV]	Range on device [µm Si]	LET on device [MeV cm ^{2} / mg]
$^{53}Cr^{16+}$	3.31	505	105.5	16.1
$^{58}Ni^{18+}$	3.22	582	100.5	20.4
$^{84}Kr^{25+}$	3.35	769	94.2	32.4
$^{124}Xe^{35+}$	3.54	995	73.1	62.5

Table 5.3: List of used ions at HIF facility in Louvain-La-Neuve.

The cross sections, σ_{reset} and σ_{SEU}, versus LET are shown in Figure 5.7a and Figure 5.7b, respectively.

The experimental data obtained in the heavy ion irradiation can be used to predict the SEU cross section for proton [107]. The direct ionization SEU cross section data have to be fitted with the Weibull function which is given in Equation 5.1. The Weibull

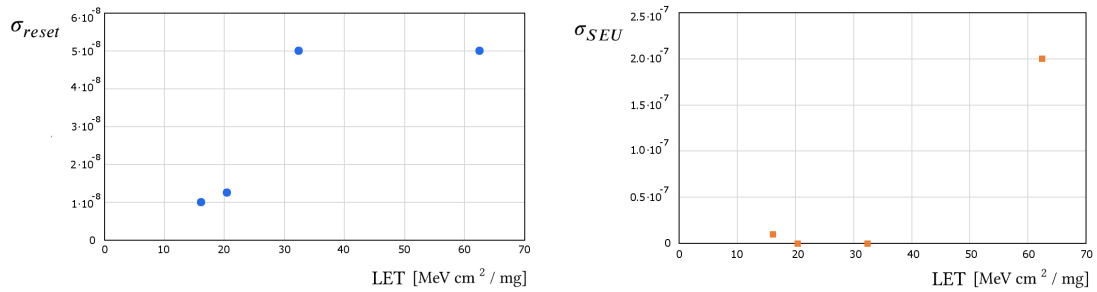
Run	Ion	Duration hh:mm:ss	Fluence particles/cm^2	N_{reset}	N_{SEU}	σ_{reset}	σ_{SEU}
1	$^{84}Kr^{25+}$	00:17:14	2.0×10^7	1	0	5.0×10^{-8}	0
2	$^{84}Kr^{25+}$	00:16:28	2.0×10^7				
3	$^{124}Xe^{35+}$	00:16:47	2.0×10^7	1	4	5.0×10^{-8}	2.0×10^{-7}
4	$^{124}Xe^{35+}$	00:16:33	2.0×10^7				
5	$^{58}Ni^{18+}$	01:04:43	8.0×10^7	1	0	1.25×10^{-8}	0
6	$^{58}Ni^{18+}$	01:02:46	8.0×10^7				
7	$^{53}Cr^{16+}$	01:03:30	1.0×10^8	1	1	1.0×10^{-8}	1.0×10^{-8}
8	$^{53}Cr^{16+}$	01:02:34	1.0×10^8				
9	$^{53}Cr^{16+}$	00:29:57	1.0×10^8				

Table 5.4: List of measurements made at HIF at UCLouvain with Krypton, Xenon, Nickel and Chromium.

curve describes a phenomenon characterized by a threshold activation, where E_{dep} is the energy deposited in the chip and E_0, σ_0, W and S are the fit parameters. E_0 represents the minimum energy required to trigger a SEU, σ_0 indicates the value of cross section to which all the sensitive volumes triggers a SEU, and lastly W and S are width and shape parameters, respectively.

$$\sigma = \sigma_0 \left[1 - e^{-\left(\frac{E_{dep} - E_0}{W} \right)^S} \right] \tag{5.1}$$

Unfortunately, the performed data acquisition is statistically poor, the chosen ions where in the right range of LET but the measure do not allow to highlight properly the expected Weibull features and perform an accurate fit. However, taking into account the order of magnitude of the obtained σ_{reset} and σ_{SEU} reported in Table 5.4, these cross sections highlight a sufficiently small SEU sensitive area compared to the LiTE-DTU area. Indeed, the sensitive node can be associated to an area of about 1 - 2 μm^2. This mean that the nodes sensitive to upset in the circuit are of the order of few units. These nodes will have to be identified in order to provide a full SEU protection.



(a) (b)

Figure 5.7: σ_{reset} and σ_{SEU} as a function of the LET.

5.4 Summary

In this chapter, the TID and SEU qualification tests performed on the first prototype of the LiTE-DTU ASIC have been presented. The LiTE-DTU have been successfully tested at the X-ray facility in Padova, with a proton beam at CNAO and with heavy ions at HIF.

The TID test has shown an optimal behavior of the ASIC, the performances before and after the irradiation are comparable, moreover in the successive months no degradation has been observed.

The SEU characterization performed at CNAO through a proton beam with fluence of 2.47×10^{13} particles/cm^2 has shown zero upset events during almost 5 hours of data acquisition. On the contrary, during the SEU test with the heavy ion beams at HIF several upsets have been observed. Four different ions have been used to irradiate the LiTE-DTU: Krypton, Xenon, Nickel, and Chromium and two different varieties of SEU have been detected. The first upset event involves hundred bit-flips and is related to the reset network while the second is the typical SEU that involves only one node. However, in order to obtain a definitive SEU characterization additional measurements are required. The foreseen SEU irradiation tests with heavy ion beams will have an extended duration and will cover the ranges of LET below 16 MeV cm ^{2} / mg and between 30 / 60 MeV cm ^{2} / mg.

Chapter 6

Conclusions and future perspectives

In this thesis the development and the characterization of a novel mixed signal ASIC for the on-detector electronics upgrade of CMS EB have been described.

The main requirement of the EB upgrade is to preserve the physics performance of the Run 1 during the HL-LHC conditions. Therefore, the EB electronics have to be adapted and refurbished for the new Level-1 trigger requirements on latency and rate. Moreover the upgraded on-detector electronics must ensure a more precise timing resolution and boost the APD noise mitigation. Therefore the legacy VFE boards will be substituted with enhanced boards and each readout channel will integrate two new custom chips: CATIA and LiTE-DTU ASICs.

The Ph.D. research activity has been entirely focused on the development and characterization of the LiTE-DTU ASIC. The device has been developed in order to obtain a reliable architecture for the readout of the analogue signals coming from the CATIA ASIC during the HL-LHC phase. The LiTE-DTU chip embeds two custom ADCs designed by an external company, a PLL developed for the CERN LpGBT project and adapted to the LiTE-DTU requirements, a digital architecture designed at INFN Torino. The chip fabrication has been done in a 65 nm CMOS technology, the first prototype has been submitted at the end of the 2018 (LiTE-DTU_v1) while a revised version (LiTE-DTU_v1.2) will be submitted in the first quarter of 2020.

The LiTE-DTU allows to improve the signal information through a fourfold increase of the sampling rate from 40 MS/s to 160 MS/s. Moreover, after the samples digitization the ASIC performs an online data selection and lossless compression mechanism, and lastly the serial data transmission at 1.28 Gb/s to the FE system.

A comprehensive characterization of the LiTE-DTU_v1 prototype has been performed and each embedded block has been fully tested. During the ASIC characterization some weakness and issues have been found, e.g. in the I^2C block, in the inter-calibration procedure between the time-interleaving ADCs, and a non negligible deterministic jitter component of the PLL. However, these weakness have not affected the LiTE-DTU characterization and all the digital blocks have shown a good behavior and have performed to specifications. Indeed there is satisfactory agreement between the results obtained in the laboratory and the simulations both in ATU and in DTU operational modes.

Radiation testing campaign results are very promising and show a good overall behavior of the chip. In particular, the TID test performed with X-rays ($E_{X\text{-}ray}$ = 10 keV) up to a total dose of 50 kGy has shown that the ASIC performance before and after the irradiation are comparable and no degradation has been observed. The SEU characterization has been performed both with protons and heavy ions. During the former test, a proton beam with fluence of 2.47×10^{13} particles/cm^2 has been used and the results have been shown zero upset events during almost 5 hours of data acquisition. On the contrary, during the latter SEU test with the heavy ion beams several upsets have been observed but the obtained cross section indicated that there is a small SEU sensitive area compared to the ASIC area. However, in order to obtain a definitive SEU characterization additional measurements will be performed extending the duration of the data acquisition and investigating the LET range below 16 MeV cm ^{2} / mg and between 30 / 60 MeV cm ^{2} / mg. All these results are considered an important step in the development of a reliable and robust design architecture for an on-detector electronic device suitable for HEP experiments.

In the next future it is foreseen to accomplish the characterization of the LiTE-DTU_v1.2 prototype and to test the ASIC along with the whole VFE system. The final version (LiTE-DTU_v2) will integrate an updated version of ADC IP block and PLL block. Moreover a fallback solution of the selection and compression algorithms will be added in the DTU. The fallback mechanism will implement an automatic reduction of sample selection in order to lower the sample rate to 80 MHz in case of high-energy events with occurrence higher than expected. This mechanism will allow to avoid data-loss due to potential system overflow.

Appendix A

PCB layout and schematic

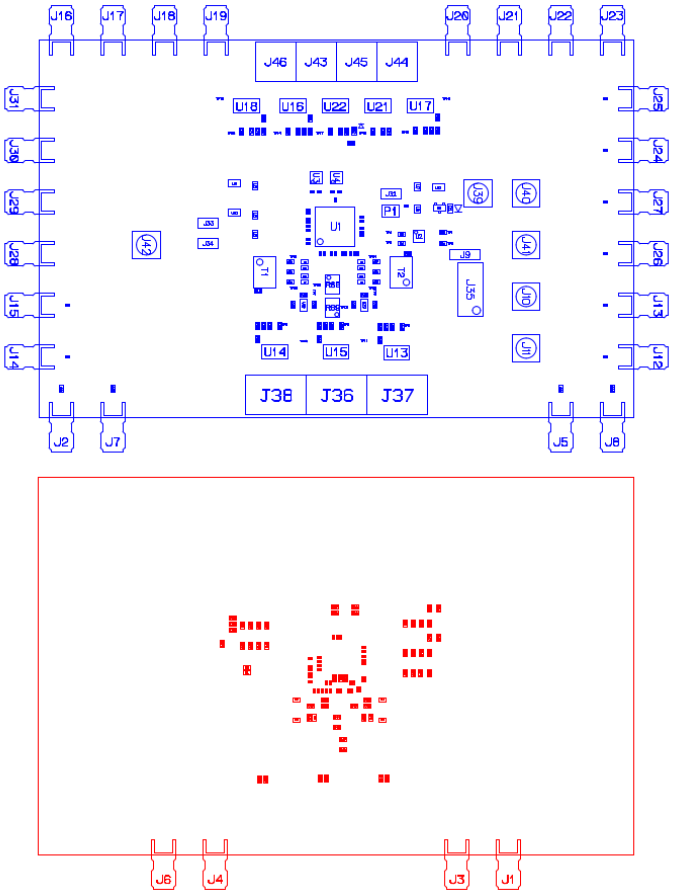
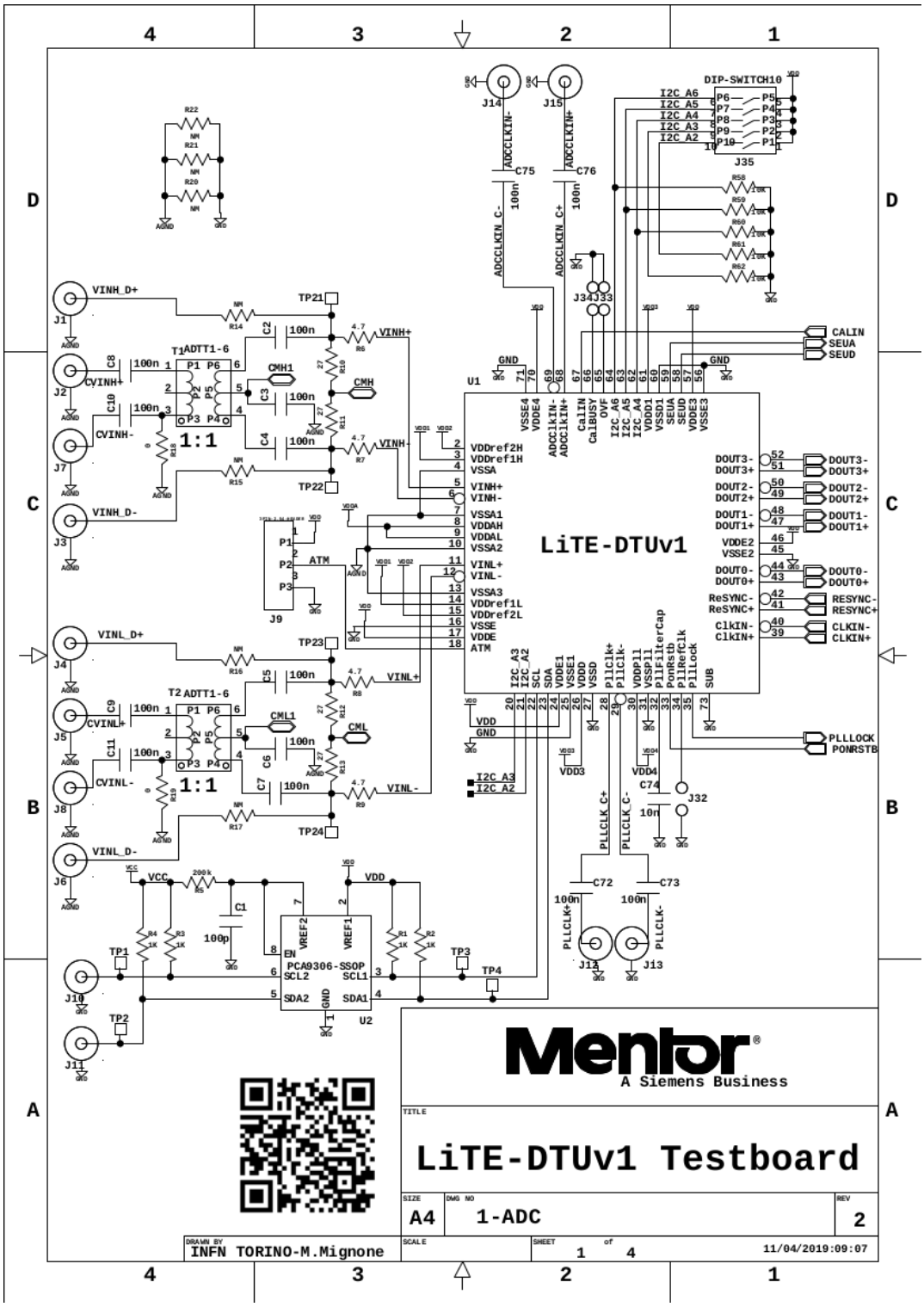


Figure A.1: LiTE-DTU PCB layout, top (blue) and bottom (red) views.


LiTE-DTUv1
Mentor
A Siemens Business
LiTE-DTUv1 Testboard
A4
1-ADC
2
INFN TORINO-M.Mignone
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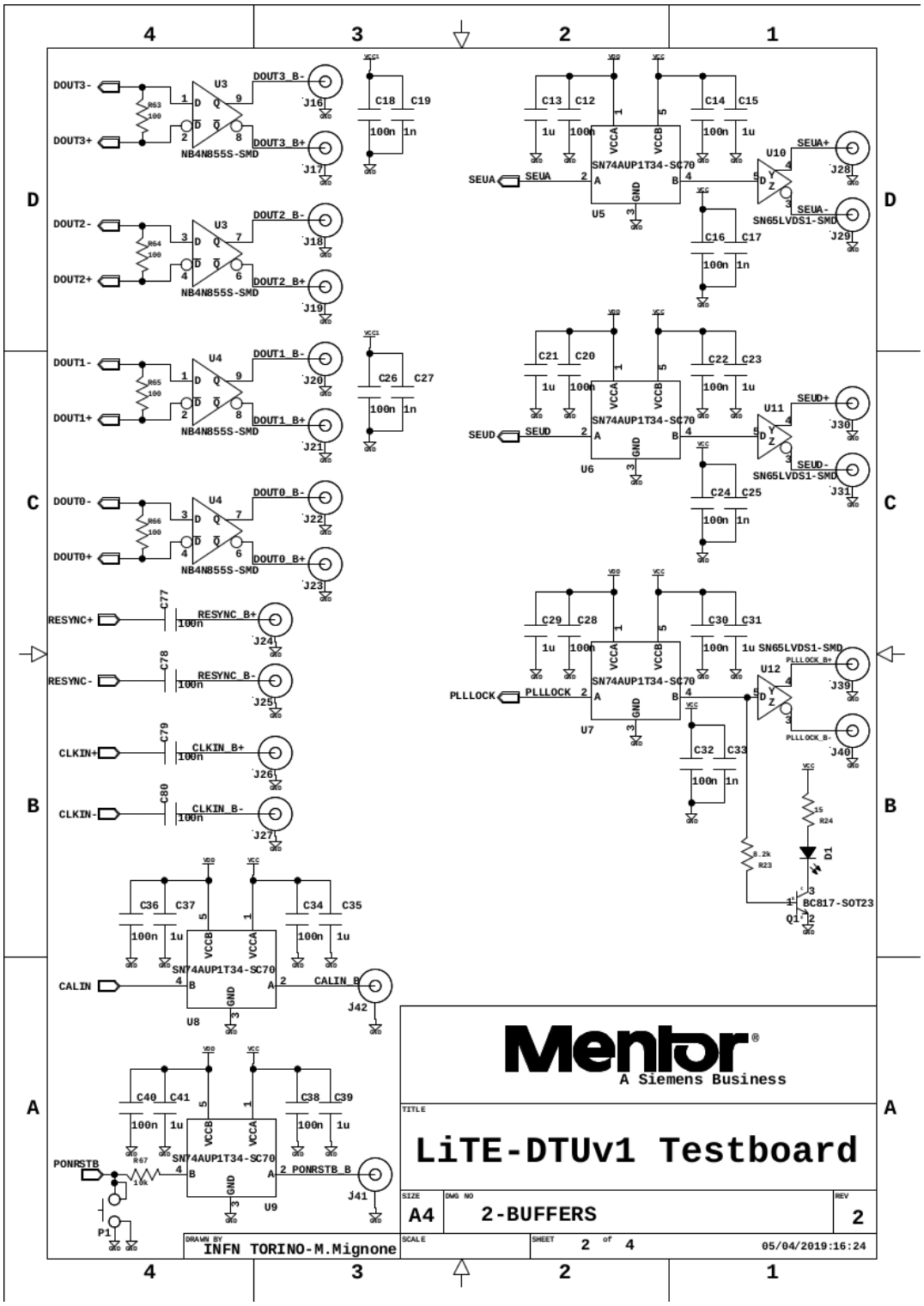
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DOUT3+
DOUT3_B-
DOUT3_B+
NB4N855S-SMD
DOUT2-
DOUT2+
DOUT2_B-
DOUT2_B+
DOUT1-
DOUT1+
DOUT1_B-
DOUT1_B+
DOUT0-
DOUT0+
DOUT0_B-
DOUT0_B+
RESYNC+
RESYNC-
RESYNC_B+
RESYNC_B-
CLKIN+
CLKIN-
CLKIN_B+
CLKIN_B-
SEUA
SEUA+
SEUA-
SEUD
SEUD+
SEUD-
SN65LVDS1-SMD
PLLLOCK
PLLLOCK_B+
PLLLOCK_B-
CALIN
CALIN_B
PONRSTB
PONRSTB_B
SN74AUP1T34-SC70
BC817-SOT23
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LiTE-DTUv1 Testboard
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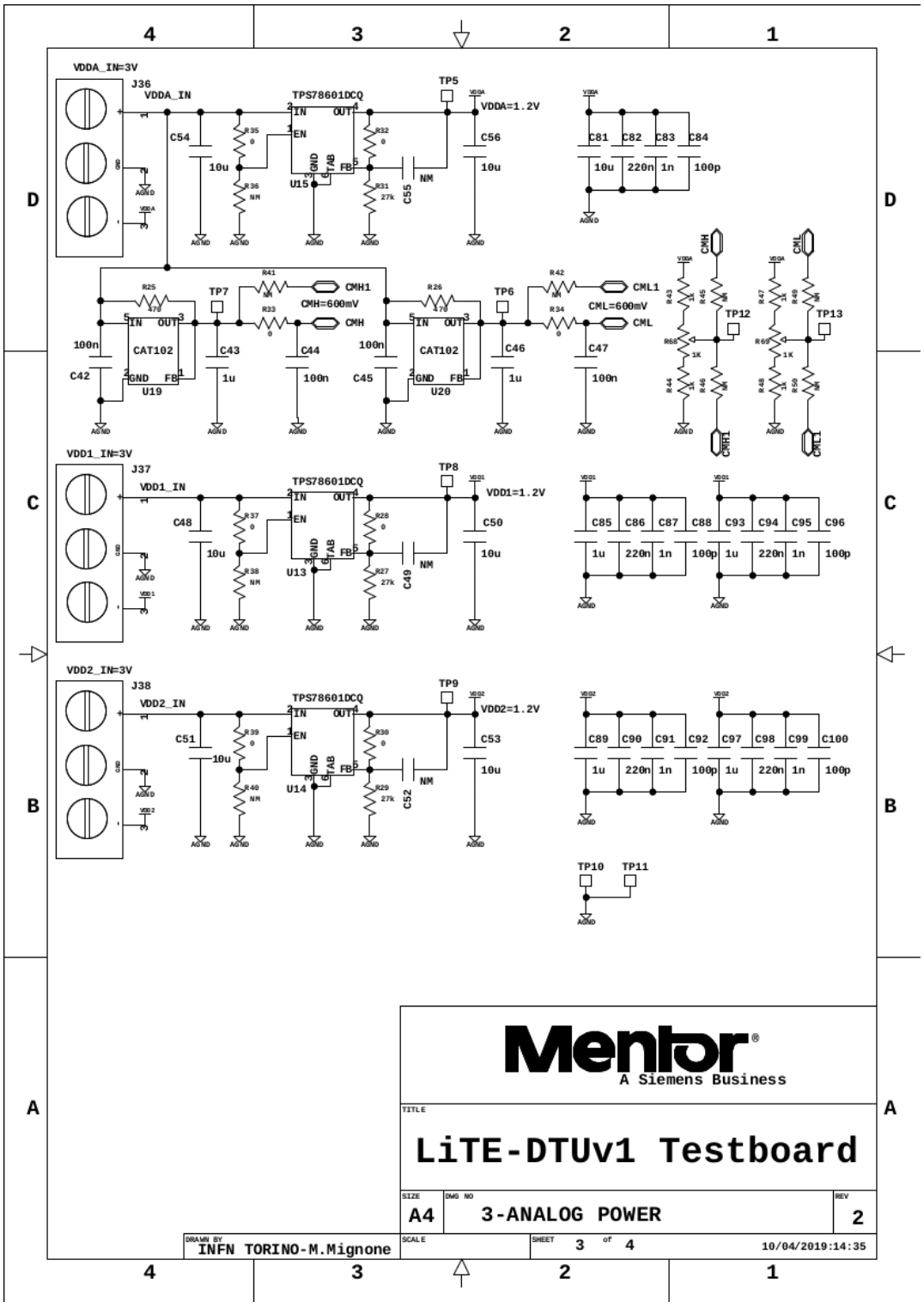
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VDDA_IN
TPS78601DCQ
TP5
VDDA=1.2V
C54
10u
C56
10u
C81
C82
C83
C84
10u
220n
1n
100p
U15
C55
NM
CMH1
CMH=600mV
CML1
CML=600mV
TP7
TP6
TP12
TP13
CAT102
U19
U20
C42
C43
C44
C45
C46
C47
100n
1u
VDD1_IN=3V
J37
VDD1_IN
VDD1=1.2V
C48
C50
C85
C86
C87
C88
C93
C94
C95
C96
U13
C49
VDD2_IN=3V
J38
VDD2_IN
VDD2=1.2V
C51
C53
C89
C90
C91
C92
C97
C98
C99
C100
U14
C52
TP8
TP9
TP10
TP11
Mentor
A Siemens Business
TITLE
LiTE-DTUv1 Testboard
SIZE
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DWG NO
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2
DRAWN BY
INFN TORINO-M.Mignone
SCALE
SHEET
3 of 4
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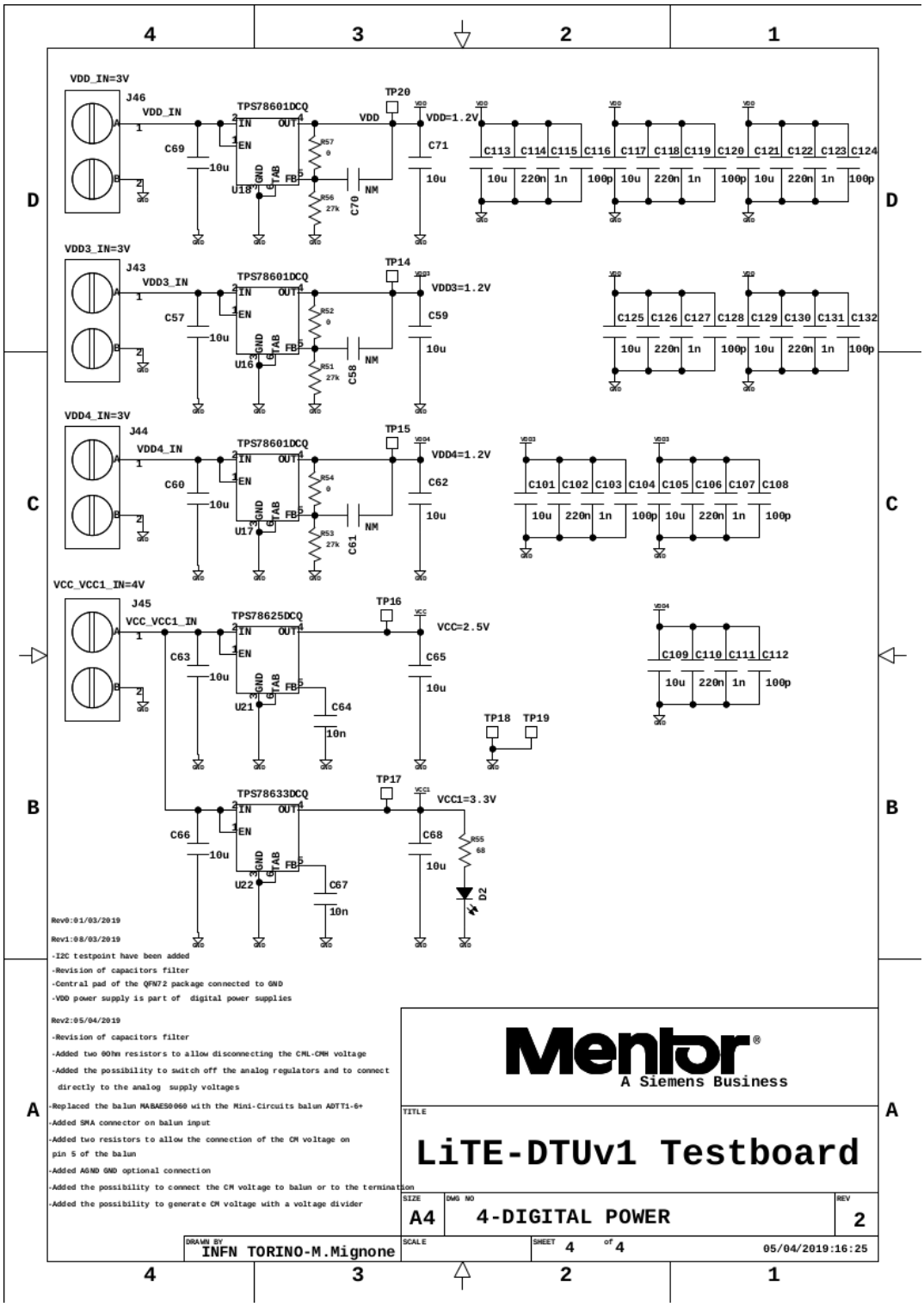
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VDD_IN
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TP20
VDD
VDD=1.2V
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10u
C71
10u
U18
R57
0
R56
27k
C70
NM
C113 C114 C115 C116 C117 C118 C119 C120 C121 C122 C123 C124
10u 220n 1n 100p 10u 220n 1n 100p 10u 220n 1n 100p
VDD3_IN=3V
J43
VDD3_IN
TPS78601DCQ
TP14
VDD3=1.2V
C57
10u
C59
10u
U16
R52
0
R51
27k
C58
NM
C125 C126 C127 C128 C129 C130 C131 C132
10u 220n 1n 100p 10u 220n 1n 100p
VDD4_IN=3V
J44
VDD4_IN
TPS78601DCQ
TP15
VDD4=1.2V
C60
10u
C62
10u
U17
R54
0
R53
27k
C61
NM
C101 C102 C103 C104 C105 C106 C107 C108
10u 220n 1n 100p 10u 220n 1n 100p
VCC_VCC1_IN=4V
J45
VCC_VCC1_IN
TPS78625DCQ
TP16
VCC=2.5V
C63
10u
C65
10u
U21
C64
10n
C109 C110 C111 C112
10u 220n 1n 100p
TP18
TP19
TPS78633DCQ
TP17
VCC1=3.3V
C66
10u
C68
10u
U22
R55
68
D2
C67
10n
Rev0:01/03/2019
Rev1:08/03/2019
-I2C testpoint have been added
-Revision of capacitors filter
-Central pad of the QFN72 package connected to GND
-VDD power supply is part of digital power supplies
Rev2:05/04/2019
-Revision of capacitors filter
-Added two 00hm resistors to allow disconnecting the CML-CMH voltage
-Added the possibility to switch off the analog regulators and to connect directly to the analog supply voltages
-Replaced the balun MABAES0060 with the Mini-Circuits balun ADTT1-6+
-Added SMA connector on balun input
-Added two resistors to allow the connection of the CM voltage on pin 5 of the balun
-Added AGND GND optional connection
-Added the possibility to connect the CM voltage to balun or to the termination
-Added the possibility to generate CM voltage with a voltage divider
Mentor
A Siemens Business
TITLE
LiTE-DTUv1 Testboard
SIZE
A4
DWG NO
4-DIGITAL POWER
REV
2
DRAWN BY
INFN TORINO-M.Mignone
SCALE
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Appendix B

LiTE-DTU I^2C registers

Main control registers

Name	Bit	Value	Note
Not used	7	0	-
Not used	6	0	-
RxEnAdcClk	5	0	ADC external clk input enable
TxEnPLL	4	0	PLL output driver enable
TxEnDrv3	3	0	dout_3 output driver enable
TxEnDrv2	2	0	dout_2 output driver enable
TxEnDrv1	1	0	dout_1 output driver enable
TxEnDrv0	0	1	dout_0 output driver enable

Table B.1: Main control register: address 00h

Name	Bit	Value	Note
ADC_SEL	7	0	ADC selection: 0 ADC_H, 1 ADC_L
SYSCAL	6	0	System calibration mode
ExtCalEn	5	0	Enable calibration from external pin
ClkInv	4	0	ADC clock inversion
ExtClk	3	0	ADC clock from external pins
DF	2	0	ADC output data format
OM_H	1	0	Operation Mode Control ADC_H
OM_L	0	0	Operation Mode Control ADC_L

Table B.2: ADC control register: address 01h

Name	Bit	Value	Note
inv	7:3	00000	Tx invert data
DrvStrngth	2:0	100	Driver current

Table B.3: CLPS drivers control: address 02h

Name	Bit	Value	Note
PeMode	7:6	00	Pre-emphasis mode
PeWidth	5:3	100	Pre-emphasis width
PeStrength	2:0	000	Pre-emphasis current

Table B.4: CLPS drivers pre-emphasis control: address 03h

Name	Bit	Value	Note
Not used	7	-	-
Inv	6:4	000	Invert data
termEn	3	0	Line termination enable
setCM	2	0	Set input commom mode
equalizer	1:0	00	Input line equalizer

Table B.5: CLPS receivers control: address 04h

Name	Bit	Value	Note
BaselineH	7:0	00000000	Baseline subtraction value gain x10

Table B.6: Baseline subtraction register, gain x10: address 05h

Name	Bit	Value	Note
BaselineL	7:0	00000000	Baseline subtraction value gain x01

Table B.7: Baseline subtraction register, gain x01: address 06h

Phase-Locked Loop registers

Name	Bit	Value	Note
BIASGEN_CONFIG	7:4	1000	Set bias current generator
vcoDAC	3:0	1000	Set the VCO current

Table B.8: PLL bias control register: address 07h

Name	Bit	Value	Note
CONFIG_P_R_PLL	7:4	0100	Set PLL loop filter resistance
CONFIG_FF_CAP	3:1	000	Not used
vcoCapSelect[8]	0	0	MSB for the VCO capacitors bank selection

Table B.9: PLL bias control register: address 08h

Name	Bit	Value	Note
vcoCapSelect[7:3]	7:3	00111	VCO capacitors bank selection
vcoCapSelect[2:0]	2:0	100	nominal value: 00111100

Table B.10: PLL bias control register: address 09h

Name	Bit	Value	Note
CONFIG_I_PLL	7:4	0101	Set PLL charge pump current - I path
CONFIG_P_PLL	3:0	0101	Set PLL charge pump current - P path

Table B.11: PLL bias control register: address 0Ah

Name	Bit	Value	Note
CONFIG_I_CDR	7:4	0000	Not used
CONFIG_P_CDR	3:0	0000	Not used

Table B.12: PLL bias control register: address 0Bh

Name	Bit	Value	Note
CONFIG_I_FLL	7:4	0000	Not used
CONFIG_P_FF_CDR	3:0	0000	Not used

Table B.13: PLL bias control register: address 0Ch

Name	Bit	Value	Note
clkTree[A|B|C]Disable	7:5	0	Clock tree disable
eclk1G28Enable	4	0	Not used
eclk320MEnable	3	0	Not used
eclk160MEnable	2	0	Not used
eclk80MEnable	1	0	Not used
eclk40MEnable	0	0	Not used

Table B.14: PLL control register 0: address 0Dh

Name	Bit	Value	Note
Not used	7	0	
enableDes	6	0	Not used
enablePhaseShifter	5	0	Not used
enableSer	4	0	Not used
connectCDR	3	0	Connect the CDR to the VCO
connectPLL	2	1	Connect the PLL to the VCO
dataMuxCfg[1:0]	1:0	00	Not used

Table B.15: PLL control register 1: address 0Eh

Name	Bit	Value	Note
ENABLE_CDR_R	7	0	Not used
disDES	6	1	Not used
disDataCounterRef	5	1	Not used
enableCDR	4	0	Not used
enableFD	3	0	Not used
enablePLL	2	1	enable the PLL PFD buffers
overrideVc	1	0/1	Force the VCO control voltage to VDD/2
refClkSel	0	1	select PFD input from reference clock

Table B.16: PLL control register 2: address 0Fh

Name	Bit	Value	Note
vcoRailMode	7	0	Set the VCO output in rail-to-rail mode
disCLK	6	0	Disable the internal clock logic
disDES	5	1	Not used
disEOM	4	1	Not used
disEXT	3	1	Not used
disSER	2	1	Not used
disVCO	1	0	disable the VCO internal clock logic
skip	0	0	Not used

Table B.17: PLL control register 3: address 10h

Acronyms

ACK Acknoledge. xvi, 38

ADC Analog to Digital Converter. iii, xiii, xvi–xx, 14–16, 21, 22, 24, 25, 31, 32, 34–36, 42–60, 64, 74, 76, 77, 82–84, 86, 88–90, 93–99, 101–103, 106–109, 116, 117, 125, 126

AFC Automatic Frequency Calibration. 39, 40

ALICE A Large Ion Collider Experiment. 1

APD Avalanche PhotoDiode. iii, xv, xvi, 7, 11, 13, 14, 16, 18–23, 25, 62, 76, 78, 125

ASIC Application-Specific Integrated Circuit. iii, iv, xiii, xvi, xix, 9, 13, 14, 17, 21–25, 29, 31–34, 37, 39, 42, 58, 64–66, 68, 69, 78, 82–86, 90, 98, 99, 109, 111, 113–115, 117, 123, 125, 126

ATCA Advanced Telecommunications Computing Architecture. 28

ATLAS A Toroidal LHC ApparatuS. 1

ATM ADC Test Mode. 54, 58, 74

ATU ADC Test Unit. xiii, xvii, xx, xxi, 32, 34, 54–59, 74, 86, 88–90, 94, 95, 106–109, 126

BCP Barrel Calorimeter Processor. xvi, 28, 29, 64

CATIA CAlorimeter Trans-Impedance Amplifier. iv, xvi, 13, 21–25, 27, 29, 31, 42, 59, 78, 125

CCS Clock and Control System. 17, 28

CERN European Council for Nuclear Research. xv, 1–3, 31, 82, 125

$CLK_{1.28\ ext}$ Clock at 1.28 GHz - external, only for ADCs. xx, 32, 43, 84, 98–102

$CLK_{1.28}$ Clock at 1.28 GHz. xx, 32, 34, 40, 43, 57, 59, 74, 75, 84, 87, 90, 91, 98–103, 115

CLK_{160} Clock at 1.60 MHz. 32, 34, 40, 42, 54, 57, 59, 60, 65, 70, 72, 74, 84, 87, 90, 91, 97

CMOS Complementary Metal-Oxide Semiconductor. iii, 14, 24, 25, 31, 32, 39, 42, 82, 112, 125

CMS Compact Muon Solenoid. iii, xv, xvi, 1, 4–8, 10, 11, 13, 20, 21, 25, 26, 28, 31, 39, 77, 82, 125

CNAO National Center of Oncological Hadronterapy. xiii, 116, 117, 119, 123

CP Charge-Pump. 40, 41, 93

CP-PLL Charge-Pump Phase-Locked Loop. 39, 40

CRC Cyclic Redundancy Check. 34, 71

CSA Charge Sensitive Amplifier. xv, 14, 15, 21

CSC Catode-strip-chambers. 8

CU Control Unit. xix, 70–76, 81

DAC Digital to Analog Converter. xvii, 15, 39, 44, 45

DAQ Data Acquisition System. xxi, 9, 17, 18, 54, 56, 71, 86, 117, 119, 120

DCC Data Concentrator Card. 17, 18, 28

DD Displacement Damage. 111, 112

DNL Differential Non-Linearity. xvii, xx, 42, 48, 97, 103, 105

DT Drift-tube. 8

DTU Data Transmission Unit. iii, iv, xiii, xvi–xix, xxi, 24, 31–35, 54, 57–62, 64, 65, 69–74, 76–83, 86, 88, 90, 106–109, 126

E_T Transverse Energy. 17, 28

e-link electrical link. 27, 65, 66, 68, 74

EB ECAL Barrel. iii, iv, xiii, xv–xvii, 6, 7, 11, 13, 14, 16, 18–21, 24, 27, 29, 31, 43, 69, 78, 82, 125

ECAL Electromagnetic Calorimeter. xv, 6–8, 11, 17, 18, 43, 66

ECC Error Correction Coding. 33

ED Error Detector. xvi, 40, 41

EE ECAL Endcap. 6

ENOB Effective Number of Bits. xx, 42, 49, 50, 96, 97, 99, 101–104, 109, 115, 116

FE Front-End. xv, xvi, 14, 16–18, 21, 27–29, 31, 32, 64–66, 125

FFT Fast Fourier Transform. xx, 96, 98–101

FIFO First-In First-Out. xviii, 61–63, 71–74, 78

FPGA Field Programmable Gate Array. 9, 11, 28, 29, 84–87, 90, 97, 120

FSM Finite State Machine. xvi, xviii, 33, 36, 54, 66, 67

FSR Full Scale Range. xvii, 44–46, 48–50, 94, 96, 103, 106

GBT GigaBit Transceiver. 39

GEM Gas Electron Multiplier. 11

GOH Gigabit Optical Hybrids. 14, 17

GOL Gigabit Optical Link. 17

GUI Graphical User Interface. xix–xxi, 88, 89, 117, 118

HCAL Hadron Calorimeter. 6, 8, 11

HDVL Hardware Description and Verification Language. 31

HGCAL High Granularity Calorimeter. 11

HIF Heavy Ion Facility. xiii, 116, 117, 120, 122, 123

HL-LHC High Luminosity LHC. iii, iv, xv, 1, 3, 10, 11, 13, 18–20, 22, 24, 27, 29, 31, 39, 66, 76, 77, 81, 82, 125

HLT High-Level Trigger. 9

I^2C Inter-Integrated Circuit. xvi, xix, 32, 34, 37, 59, 60, 84–86, 88, 90, 109, 117, 126

IC Integrated Circuit. 83, 111

IL Interleaving spurs. xvii, 51–53

INL Integral Non-Linearity. xvii, xx, 42, 48, 97, 103, 105

IP block semiconductor intellectual property core. xvii, 32, 42, 43, 51, 53, 54, 97, 109, 126

L1 Level-1. xvi, 9–11, 16–19, 27, 28, 125

LET Linear Energy Transfer. xxi, 113, 116, 119, 121–123, 126

LF Loop Filter. 40, 41

LHC Large Hadron Collider. iii, xv, xix, 1, 3, 9–11, 13, 27, 78, 81

LHCb Large Hadron Collider beauty. 1

LiTE-DTU Lisbon-Turin Electronics Data Transmission Unit. iii, iv, xiii, xvi, xix, xxi, 1, 7, 13, 21, 22, 24, 25, 27, 29, 31, 32, 34–37, 39, 40, 42, 53, 54, 58, 61, 62, 64–66, 68, 69, 74, 75, 82–87, 90, 97–99, 107–109, 111, 114, 116–118, 120–123, 125–127

LpGBT Low power GigaBit Transceiver. xvi, 24, 27, 29, 31, 39, 64, 65, 82, 90, 125

LS Long Shutdown. xvi, 3, 11, 20

LSB Least Significant Bit. 24, 38, 42, 45, 48, 76, 91

LVR Low Voltage Regulator. 14, 16

MBU Multi Bit Upset. 25, 113

MC Monte Carlo. xix, 77

MGPA Multi-Gain Pre-Amplifier. xv, 14–16

MSB Most Significant Bit. 16, 38, 44, 56, 59, 66, 91

NACK Not-Acknoledge. xvi, 38

NAD Noise and Distortion. 96

OM_idle pattern Operational Mode idle pattern. xiii, xix, 58, 59, 73–75, 106, 107

P&R Place & Route. 25

PCB Printed Circuit Board. xix–xxi, 86, 87, 90, 96, 98, 99, 106, 109, 114, 118, 120, 121, 127

PFD Phase-Frequency Detector. 39–41

PLL Phase-Locked Loop. iii, xiii, xvi, xx, 31, 32, 34, 35, 39–41, 43, 57, 82–84, 87, 88, 90–93, 98, 101, 106, 109, 114, 115, 125, 126

PVT variations Process, Voltage and Temperature variations. 91

RCG Regulated Common-Gate. xvi, 22

RPC Resistive-plate-chambers. 8, 11

RTL Register Transfer Level. 31

S/H Sample-and-Hold. 44

SAR Successive Approximation. xvii, 42, 44

SCL Serial Clock. 37, 38

SDA Serial Data. 37, 38, 85

SEB Single-Event Burnout. 113

SEE Single-Event Effect. 33, 111–113

SEGR Single-Event Gate Rupture. 113

SEL Single-Event Latch-up. 113

SET Single-Event Transient. 113

SEU Single-Event Upset. iv, 24, 25, 32, 34, 42, 43, 111, 113, 116, 117, 121–123, 126

SINAD Signal-to-noise-and-distortion ratio. xvii, 49, 50, 96

SLB Synchronization and Link Board. 17, 18

SLVR Switching Low Voltage Regulator Card. 27, 29

SNR Signal-to-Noise Ratio. xvii, 49–51, 94

SRP Selective Readout Processor. 17, 18

TCC Trigger Concentrator Card. 17, 18, 28

THD Total Harmonic Distortion. xvii, 50

TIA Trans-Impedance Amplifier. xvi, 21, 22

TID Total Ionizing Dose. iv, 32, 42, 111–116, 123, 126

TM_idle pattern Test Mode idle pattern. 54, 56, 58, 59, 94

TMR Triple Modular Redundancy. 33, 36, 39, 54, 60, 65, 70, 72, 74

TMRG Triple Modular Redundancy Generator. 33

TPG Trigger Primitive Generation. 16, 17, 27, 28

TT Trigger Tower. 14, 16–18, 27

UDP User Datagram Protocol. 87

VCO Voltage Controlled Oscillator. xiii, 34, 39–41, 90, 91, 93

VFE Very Front-End. iii, xv–xvii, 14–19, 21, 22, 24, 27, 29, 31, 32, 43, 65, 66, 82, 125, 126

VHDL VHSIC Hardware Description Languag. 87

VL+ Versatile Link+. 27

VPT Vacuum PhotoTriode. 7

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