Testing Heatsink Faults in Power Transistors by means of Thermal Model

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***Abstract* — In safety-critical systems, power electronics is widely used, e.g., for driving actuators. High currents and high voltages are often used in power electronics, which may cause considerable heating of the power devices. Hence, different mechanisms for heat dissipation and cooling of power devices are adopted. An excessive temperature increase in the power devices may lead to considerable electrical and mechanical stresses, and overheated electrical devices are subject to more rapid ageing. Therefore, an incorrect behaviour of the dissipation system can seriously damage or even block a safety-critical system. Hence, it is necessary to introduce test mechanisms to check the correct behaviour of the heatsinks. In this paper, we propose a strategy to quantitatively evaluate the effectiveness of a test for the dissipation system. The proposed approach is based on an electro-thermal model of the cooling system. It allows one to identify the maximum size of the thermal fault tolerated by the dissipation system before the electrical device break down.**

Keywords — Power electronics; Thermal Faults; Safety-Critical applications; End-manufactory test

I. INTRODUCTION

High voltages and currents in power circuits inevitably cause their heating, unless proper dissipation solutions are adoped. The junction temperature increase has a significant impact on the device characteristic parameters [1], and causes numerous drifts of the main parameters of the power devices: for example, in several devices the body resistance increases considerably with the junction temperature increase. All these aspects have a considerable impact on the power systems, which may be particularly critical for power devices used in safety-critical applications. Moreover, in power devices the temperature increase may introduce considerable mechanical stress [2], typically due to the different materials that compose the devices. Different materials may have different thermal expansion coefficients and they may expand differently when the temperature changes. As discussed in [3], thermal cycles may cause a rapid ageing of the semiconductor devices. The main parameters of semiconductor devices degrade permanently due to the ageing of the devices [4][5]; the drift of these parameters bring the component to a premature break. Usually, some dissipation systems are introduced to dissipate the heat produced by the power devices. Typically, the use of passive heatsinks is preferred. The passive heatsinks are composed of opaque radial metal surfaces designed to rapidly diffuse the heat produced. In general, these dissipation systems, reliable because they are passive, but their reliability and their ability to disperse the heat considerably depend on their correct assembly on the power devices. The dissipation systems assembly phase is often underestimated in industrial applications; a wrong assembly of a passive heatsink can lead to a considerable increase of the temperatures in the semiconductor devices. Typically, passive heatsinks are inexpensive but they occupy a large physical volume; they often significantly affect the final weight of the product. Therefore, different heatsinks with fans are sometimes used to force a continuous passage of fresh air. These active heatsinks are considerably smaller with respect to the previous ones. The assembling phase of the heatsinks with fan is even more critical due to the mechanical vibrations of the fan itself. For example, the heatsink can move away from the power device due to the continuous small movements caused by the vibrations. Therefore, it is important to introduce an end-of-production test to verify the correct assembly of the heatsinks. Moreover, in some applications, an in-field test must be periodically performed to check the behaviour of the dissipation system. Other external factors may affect the in-field operation of the heat sink, e.g., the heatsink can be clogged with dust or dirt reducing its ability to disperse heat.

This paper proposes a strategy for testing the heatsinks assembled on discrete power devices, such as Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) or Insulated Gate Bipolar Transistors (IGBTs). The proposed strategy can be replicated with an Automatic Test Equipment (ATE) for board testing at the end of the production (e.g., In-Circuit ones [6]). Currently, the ATEs are equipped with numerous probes able to perform voltage or current measurements; on the other side, the modern ATEs are not equipped with efficient thermal probes able to measure the surface temperatures on the heatsinks or the surface temperature on the transistors packages [7]. The test proposed in this paper is performed resorting to some voltage and current electrical measurements, while temperature measures are not considered, in accordance with the ATE limitations.

In this paper, with respect to the work proposed in [8], we assess the effectiveness of the proposed test approach resorting to a thermal model of the dissipation system. In the proposed thermal model, different faults are considered and simulated. A methodology for generating the thermal fault list in a thermal model is newly proposed in this paper. Moreover, the proposed approach allows to estimate the maximum thermal fault tolerated by the dissipation system; in other words, it is possible to establish the mechanical tolerances accepted during the assembling phase of the heatsink, such as the minimum contact surfaces between the power device and the heatsink, or the force that the heatsink must impose on the transistor for correctly contacting it. A MOSFET transistor in a TO-220 package with a passive heatsink assembled is considered as a case study.

This paper is organized in different sections: Section II introduces the basic theory about the electrothermal models and illustrates the effects of temperature on the power devices.

Section III introduces the concept of thermal faults and outlines the proposed approach. The case study is outlined in Section IV, while the experimental results obtained on it are reported in Section V. Finally, Section VI closes this paper with some conclusions.

II. Background

This section first introduces the reader to the main thermal effects affecting semiconductor power devices, later describes the concepts of the thermal models used in this paper. Finally, the in-circuit test used for testing the heatsinks assembling is described.

A. Thermal effects on power devices

The junction temperature (Tj) is one of the most important parameters of a power device because it significantly impacts on the device performance and reliability. In the power transistors, most of the failure mechanisms are due to thermally activated processes [2]. A higher junction temperature accelerates these failure mechanisms and reduces the lifespan of the devices due to ageing [4]. The failure mechanisms activated by the junction temperature increase [2] include the hot electron effects and the increase of the on resistance when the power transior is in ohmic region [4]. The hot electron effect [9] is a dangerous phenomenon present in most semiconductor devices. Some electrons gain sufficient kinetic energy to overcome a potential barrier or an oxide barrier; the kinetic energy depends on the junction temperature of the device. Due to the hot electron effects, a transistor can always work in an active conduction state.

The causes of device breakage are not limited to electrical problems, but also to physical and mechanical ones [2]. The junction temperature fluctuations create, inside of the power devices, some mechanical stresses [2]. The mechanical stresses are the main causes of the break of the solder connection of the devices on the board. Other important issues connected to the mechanical stresses are related to the wire bonding connections between the die and the external contacts of the devices. All these aspects reduce the reliability of the device in the long term: this is one of the key aspects for many critical systems.

B. Thermal network model

In this subsection, the thermal model of a system is introduced. When considering thermal issues, systems can be modelled using electrical networks; this approach to model the systems for thermal analysis is broadly used by different electrical and electronic companies [9][10][11] and it is widely discussed in [2][12]. Some electronic companies provide thermal models for their power devices [11][13][14]. These models are normally used to correctly design the heatsink, possibly resorting to thermal simulations.

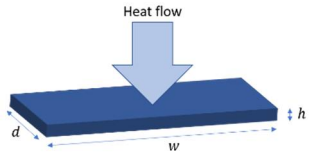
Heat propagation in a system can take place in three different ways: convection, radiation, and conduction. In electronic Printed Circuit Boards (PCBs), heat propagation occurs mainly due to the conduction phenomenon. In the network modelling, it is assumed that the heat propagation occurs in one direction only, and in a homogeneous isotropic material [2]. These assumptions simplify the differential equations of traditional thermal models. The new simplified differential equations have the same mathematical structure of the equations used for the propagation of signals in the transmission lines, as discussed in [2] and [10]. Considering the Kirchhoff principle [2][10][11] ("*Two different forms of energy behave identically when the basic differential equations which describe them have the same form, and the initial and boundary conditions are identical*") it is possible to identify an analogy between the electrical and the thermal models. This allows to create an electrical network that models the thermal aspects. The equivalent parameters between the two different models are shown in Table 1. In these thermal networks, the known electrical principles (e.g., the Ohm law, the two laws of Kirchhoff, the Superposition Theorem**,** and so on) can be used to evaluate the temperatures and the heat flows.

Electrical model		Thermal model	
Physical quantity	Symbol and unit of measurement	Physical quantity	Symbol and unit of measurement
Voltage	U [V]	Temperature	T [K]
Current	I [A]	Heat Flow	P [W]
Resistance	R [Ω]	Thermal resistance	R_{th} [K/W]
Capacitance	C [F]	Thermal capacitance	C_{th} [J/K]

Table 1: Equivalent thermal and electrical quantities

In thermal networks, the electrical components represent the thermal quantities; resistances, capacities and electrical generators assume a different physical meaning than the electrical ones. In a thermal network, the generators are used to model the sources of heat, as the junction temperature of the power devices or the ambient. The voltage generator models the temperature source, while the current generator models the heat flow source. In electrical networks, the electrical resistance opposes the passage of the electrical charges. Similarly, in the thermal networks the thermal resistance is opposed to the passage of the heat flow [2]. It is possible to estimate the value of the thermal resistance of a physical object with a mathematical approach. The mathematical approach considers the form, the material and the thermal conductivity of the object. Often, as an alternative to the complex mathematical approach, the thermal resistance is measured experimentally. The thermal resistance of a parallelepiped of homogeneous material can be calculated using the equation (1) shown in Figure 1, as discussed in [9]. Equation (1) is valid only if the material is crossed homogeneously by a constant heat flow; this assumption can be considered valid internally to the transistor package where the dimensions are comparable with those of the silicon die [9]. Considering the dimensions of the heatsinks with respect to those of the transistor, the equation (1) cannot be used to estimate the thermal resistance of the heatsinks. In a thermal network, the thermal capacitance of an object describes the amount of heat that the object can store. The heat capacitance is a physical property of the matter; it is defined as the amount of heat to be supplied to a given mass of a material to produce a unit change in its temperature [2]. Therefore, the temperature of an object increases when the heat flows into the object and decreases when the heat comes out. The thermal capacitance is determined by the mass of the object and by its specific heat, as shown by the equation (2) of Figure 1. Often, the thermal capacitance is measured experimentally. Therefore, in a circuit simulator, it is possible to perform simulations of electrical networks considering also the thermal effects. In these simulations, in addition to the electrical network, the thermal network is also simulated. In the

models of the power devices that consider the thermal aspects, two additional ports are available to monitor the thermal network [14]. The first thermal port can be used to monitor the junction temperature of the power device, while the second thermal port corresponds to the case package temperature. To the second thermal port, it is possible to connect the electrical network that models the thermal aspects of the heatsink.



$$R_{th} = \frac{h}{d \cdot w} \cdot \frac{1}{\lambda_{th}} \quad \left[\frac{K}{W}\right] \quad (1)$$

$$C_{th} = c \cdot m = c \cdot \rho \cdot d \cdot w \cdot h \quad \left[\frac{J}{K}\right] \quad (2)$$

Symbol	Physical quantity
R_{th}	Thermal resistance of the parallelepiped
C_{th}	Thermal capacitance of the parallelepiped
λ_{th}	Thermal conductivity of the parallelepiped material [W·m^{-1}·K^{-1}]
c	Heat capacity of the parallelepiped material [J·g^{-1}·K^{-1}]
m	Mass of the parallelepiped [g]
ρ	Specific weight of the parallelepiped material [g/cm^3]
d	Depth of the parallelepiped [cm]
w	Width of the parallelepiped [cm]
h	Height of the parallelepiped [cm]

Figure 1: Thermal resistance and thermal capacitance equations

C. Cauer and Foster thermal network

In the previous subsection, the concepts of thermal resistance and capacitance have been introduced; in this subsection, these thermal components are used to create a thermal network.

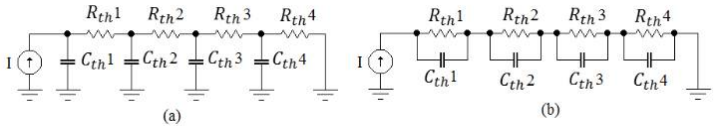


Figure 2: a) Cauer thermal network; b) Foster thermal network

Figure 2 shows two different approaches typically used for building the thermal model of physical systems [15]. In the Cauer approach, the thermal model is derived from a physical analysis of the system; each thermal element is associated with a physical element present in the system. Figure 3 analyzes the thermal model of a series of parallelepipeds of different materials (M1, M2, M3, M4) crossed by a heat flow; it is possible to see how each physical element that opposes the passage of heat is modelled by a R_{th}-C_{th} Cauer cell. The values of each thermal resistance and of each thermal capacitance depend on the material and the thickness of each layer, as described by the equations (1) and (2) of Figure 1. The Cauer thermal model is obtained studying the physical system to be modelled.

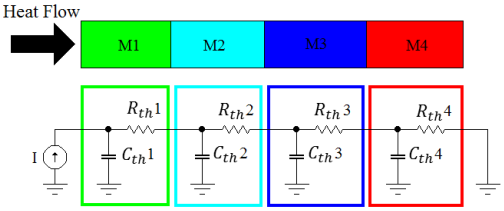


Figure 3: Cauer thermal model approach

In the Cauer model, the succession of the physical elements present in the system is analysed with respect the heat propagation direction considered. Typically, the different layers of oxide, semiconductor, plastic, and metal present in the system are considered. Therefore, this approach requires an excellent knowledge of the physical system under analysis. Figure 2 shows also the Foster model approach; in this case, the model is composed of a succession of Foster R_{th}-C_{th} cells. The Foster model is obtained experimentally by measuring the thermal trends in different points of the system [16].

D. The proposed thermal test

In this subsection, the test procedure used to test the heatsinks assembling is outlined. The proposed approach, described in [8], is performed in-circuit with an Automatic Test Equipment (ATE). The ATE is able to contact different points of a PCB by means of small needle probes. The probes are moved with precision automatically by the ATE itself in order to contact the points of interest used to perform the test. Through the probes, the ATE can force some voltages or currents in the circuit, and perform different voltage or current measurements. The ATE directly contacts the transistor under test realizing the circuit shown in Figure 4. The test is performed on the final Printed Circuit Board (PCB) at the end of production. In Figure 4, the test circuit realized by the ATE is shown in blue. The ATE forces the Vgs and the Vtest chosen in accordance whit the technical specifications of the transistor under test, as discussed in [8]. The values of Id and Vds are measured during the test, the value of Ron(Tj) is derived using the relation Ron(Tj)=Vds/Id. Knowing the Ron(Tj) characteristic of the transistor, it is finally possible to obtain the junction temperature of the transistor. Using the equation (3), it is possible to derive the R_{th}ja of the whole system. If this value differs from the expected value, considering a tolerance range, the test has detected a thermal fault in the dissipation system.

$$R_{th,ja} = \frac{Tj - Ta}{Vds \cdot Id} \quad (3)$$

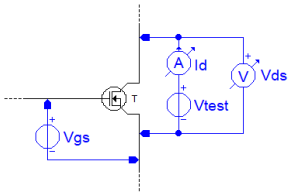


Figure 4: Heatsink thermal test

III. Proposed Approach

This section introduces the concept of thermal fault and proposes a method for generating the list of thermal faults in a thermal model. Afterwards, the proposed methodology for simulating the thermal faults is shown.

A. Thermal faults

In this paper, we define the concept of thermal fault as an alteration of the dissipation ability of a heatsink [8]. In accord with the thermal model network described in Section II, a thermal fault is an increase of the thermal resistance value. All possible thermal faults are modelled by inserting additional thermal resistors. For each thermal resistance in the thermal model, a further thermal resistance placed in series is added. These new thermal resistors represent, from a physical point of view, an additional obstacle to the passage of the heat. These obstacles identify, for example, the incorrect contact between the various elements of the dissipation chain. In the simplest

case, the dissipation structures is composed only of a pair of elements: the package of the transistor and the heatsink. In more complex chains further elements can be present, as the electrical insulation foils between the transistor and the heatsink. The new thermal resistors added to model the thermal faults can be used to model the physical alterations of the heatsink itself. If one or more cooling fins of the heatsink are physically damaged, the available dissipation surface decreases. This leads to an increase of the thermal resistance of the heatsink. The value of the thermal fault resistance is identified using the thermal model of the system. The value of the thermal resistance is calculated imposing Tj = Tjmax in the thermal network (i.e., the value of the thermal fault resistance is chosen in order to maximize the device junction temperature). In other words, Tj is brought to the maximum value tolerated by the power device. The thermal network model is considered in steady state: this is possible assuming a constant heat flow produced by the power device.

To better explain the algorithm used to identify the value of the thermal fault resistance, a simple example is proposed. Figure 5.a shows the Cauer model of a transistor without the heatsink. The model is composed of two thermal resistances and one thermal capacitance; the physical meaning of the thermal components is shown in Table 2. In absence of a heatsink, the circuit that describes the propagation of heat from the component to the air is composed of a single thermal resistance ($R_{th,ca}$). The current generator $Vds \cdot Id$ models the heat flow produced by the transistor, which depends on the electrical power absorbed by the transistor. The voltage generator Ta models the ambient temperature. Assuming that the two generators are constant over time, it is possible to analyze the electrical network in steady state. The circuit shown in Figure 5.b is considered; in this circuit it is possible to consider an additional thermal resistance ($R_{th,F}$) that models a possible thermal fault. From a physical point of view, the $R_{th,F}$ resistance identifies an occlusion of the heat flow from the transistor to the air. This occlusion may be due to the presence of unwanted material on the transistor, such as processing residues or dust.

Thermal components	Description
$R_{th,jc}$	Junction to case thermal resistance
$R_{th,ca}$	Case to air thermal resistance
$C_{th,d}$	Transistor die thermal capacitance

Table 2: Thermal components description

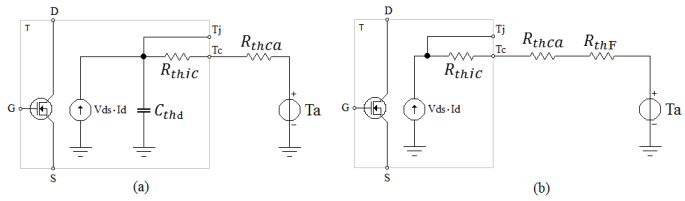


Figure 5: a) Cauer model of a transistor without the heatsink; b) Cauer model of a transistor without the heatsink with assembling thermal fault

The value of the $R_{th,F}$ is identified imposing Tj = Tjmax and resolving the network with the superposition theorem. The equation (4) is obtained.

$$R_{th,F} = \frac{Tjmax - Ta}{Vds \cdot Id} - R_{th,jc} - R_{th,ca} \qquad (4)$$

B. *Thermal fault simulation*

The approach we propose to assess the effectiveness of the thermal test is discussed in this subsection. The thermal model of the physical system under analysis is derived. The thermal model is based on the paradigms of the thermal networks as described in Section II. The thermal resistors, thermal capacitances, and thermal sources are measured experimentally or they are obtained from the datasheets of the power device and the heatsink. The validation of the thermal model is performed comparing the junction temperature experimentally measured with the simulated one. The junction temperature of the physical system is measured on the tab of the transistor, as shown in [16]. During the validation phase, the power transistor is turned-on in a fixed working point and the case temperature is measured. The thermal model passes the validation check if the results obtained with the model simulation and experimentally are similar, with a defined tolerance value. When the validation procedure is completed, it is possible to execute an electro-thermal fault-free simulation of the test procedure proposed. The test procedure considered is described in subsection D of Section II. Afterwards, a new set of simulations is performed in a faulty scenario. In each simulation, a single thermal fault is considered in the thermal network. The value of the thermal fault resistor is chosen as shown in subsection A of Section III. The injected thermal faults are labelled as detected if the difference between the $R_{th}jc$ performed in the faulty and fault-free scenarios is different from the expected value, considering an acceptable maximum difference. Generally, the acceptable range is defined as very wide, so that the fault is detected only if a wide variation is observed.

IV. CASE STUDY

In this section, the thermal model of a circuit made up of SPP07N60C3 transistor is presented and analyzed. The physical system is composed of a MOSFET transistor in a TO-220 package and a passive heatsink assembled on the power device by means of a screw. The first subsection shows the proposed thermal model, and the second subsection describes the transistor used.

A. *The proposed thermal model*

This subsection describes the proposed thermal model. Figure 6 shows the Cauer model considered [9][17]. On the left part of Figure 6, the physical system is shown. The system is composed of a transistor with a passive heatsink assembled. On the right part of Figure 6, the proposed Cauer network that models the system is shown. Three different Cauer cells were considered in the heat flow propagation direction. In this model, only the main heat flow is considered: this flow is generated in the transistor die. The heat flow propagates towards the air passing through the transistor package and the heatsink. This model is an approximation because the heat propagates in all possible directions. Therefore, the proposed model is pessimistic because it does not consider the secondary heat flows. The secondary heat flows contribute to the dispersion of the heat produced, even if to a lesser extent with respect to the main heat flow considered. Table 3 shows the physical meaning of each thermal component considered in the model.

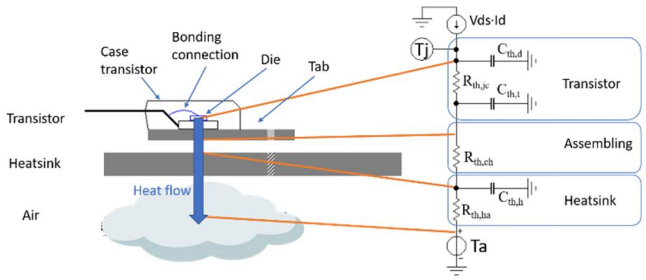


Figure 6: Proposed thermal model

Thermal component	Description
$R_{th,jc}$	Junction to case thermal resistance of the transistor
$R_{th,ch}$	Case to heatsink thermal resistance; it depends on the heatsink assembling
$R_{th,ha}$	Heatsink to air thermal resistance; it depends on the form, size and material of the heatsink
$C_{th,d}$	Thermal capacitance of the transistor die
$C_{th,t}$	Thermal capacitance of the transistor tab
$C_{th,h}$	Thermal capacitance of the heatsink

Table 3: Thermal components descriptions

B. The considered device

The SPP07N60C3 [18] transistor is a power N-MOS device belonging to the Infineon CoolMOS family. The thermal model of the device [19] allows to simulate the behaviour of the transistor considering possible variations of its junction temperature. Moreover, it allows us to simulate the trend of the junction and case temperatures as described in Section II. The device, available in package TO-220, supports a maximum voltage of 650V and maximum currents of 7.3A. Its nominal Ron at 25°C is 0.6Ω. The maximum junction temperature tolerable by the transistor is 150°C. Table 4 reports some thermal parameters of the transistor considered; these values are read from the datasheet of the transistor [18]. The $R_{th,ca}$ value must be considered only in absence of a heatsink; this value shows the intrinsic ability of transistors to dissipate the heat without the aid of an external dissipation system.

Thermal component	Value
$R_{th,jc}$	1.5 K/W
$R_{th,ca}$	62 K/W
$C_{th,d}$	0.045 J/K
$C_{th,t}$	0.14 J/K

Table 4: Thermal model parameters

The thermal model of the considered transistor, provided by the manufacturer, is a Cauer network with six cells. The parameters of each cell are shown in Table 5 [19], these values are extracted from the SPICE model of the transistor.

#Cauer cell	R_{th}	C_{th}
1	26.17 mK/W	62.34 µJ/K
2	36.1 mK/W	375.9 µJ/K
3	202.59 mK/W	530.7 µJ/K
4	265.21 mK/W	3 mJ/K
5	257.75 mK/W	6.86 mJ/K
6	400 mK/W	140 mJ/K

Table 5: SPP07N60C3 Cauer parameters

The heatsink chosen in this work consists of a single alumina (Al_2O_3) fin. The heatsink is assembled to the transistor by means of a screw-nut fixing system. The features of the heatsink are shown in Table 6.

Physic parameters	Value
d	3.6cm
w	3.6cm
h	1.6mm
c	0.8 $J \cdot g^{-1} \cdot K^{-1}$
ρ	3.8 g/cm^3
λ_{th}	24 $W \cdot m^{-1} \cdot K^{-1}$

Table 6: Heatsink features

V. EXPERIMENTAL RESULTS

This section presents the parameters of the proposed thermal model. The model is validated comparing the model simulation with a real case experimentally measured. Finally, some possible thermal faults are considered and the fault simulation results are reported.

A. Model parameters estimation

The parameters of the thermal components ($R_{th,jc}$; $R_{th,ch}$; $R_{th,ha}$; $C_{th,d}$; $C_{th,h}$) of the Cauer model proposed in Figure 6 are estimated considering the proposed case study. The junction–to-case thermal resistance ($R_{th,jc}$) and the thermal capacitances ($C_{th,t}$; $C_{th,d}$) of the transistor are read from the transistor datasheet: these values are shown in Table 4. The thermal resistance of the heatsink is measured experimentally as shown in [16]; in [16] the transistor is heated bringing it in the saturation region, and then switched to interdiction by measuring the Tj in the cooling phase. From the definition of the thermal resistance ($R_{th} = (Tj-Ta)/P_{dis}$) it is possible to obtain the value of the thermal resistance of the heatsink. P_{dis} is the power dissipated by the transistor, which is equal to P_{dis}=Vds·Id. The value of the thermal resistance of the heatsink is shown in Table 7. The thermal contact resistance depends on the force exerted by the screw on the heatsink, as discussed in [20]. Considering a minimum contact force of 20N there is a thermal contact resistance ($R_{th,ch}$) of 1.2K/W. The heatsink thermal capacitance is estimated by its physical features using equation (2) with the values shown in Table 6. The values obtained is reported in Table 7.

Physic parameters	Value
$R_{th,ha}$	23.44 K/W
$R_{th,ch}$	1.2 K/W
$C_{th,h}$	6.3 J/K

Table 7: Thermal model parameters

The proposed model has been experimentally validated; the transistor is heated imposing a current Id = 1.85A for 200s, and then it is cooled imposing a current Id = 0.5A. During the heating and cooling phases, the junction temperature is measured using a thermocouple on the device tab, as explained in [8]. The trend of the Tj measured and simulated is shown in Figure 7. The proposed thermal model represents a good approximation of the measured physical trend, as shown in Figure 7.

B. Fault simulation results

The effectiveness of the test procedure proposed in Subsection II.D is assessed on the case study. In the fault-free scenario, imposing a Vtest of 1.5V, a Vds of about 1.24V and a Id of about 2A are measured with a Tj simulated of 80°C. A thermal fault resistance ($R_{th,F}$) is added in series to the $R_{th,ch}$. The $R_{th,F}$ resistance modelled a possible assembling fault in the heatsink.

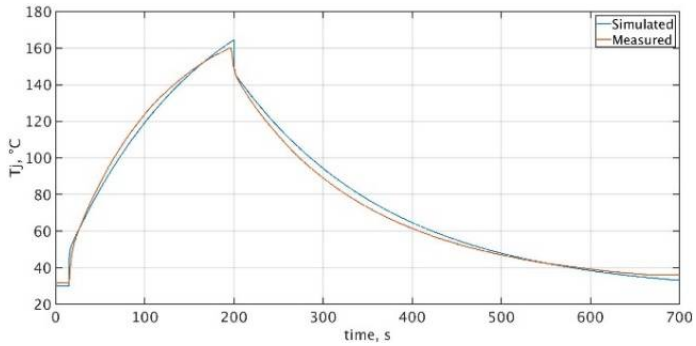


Figure 7: Thermal model validation

The value of the $R_{th,F}$ is calculated by imposing Tj = Tjmax = 150°C as discussed in the proposed approach. The value of the fault resistance is $R_{th,F}$ = 11.28 K/W. In presence of the injected fault the voltage Vds measured is approximately 1.79V whit a Tj of 149.7°C. The $R_{th,F}$ thermal resistance identified by the proposed approach identifies the maximum thermal fault tolerated by the transistor. In the presence of an incorrect assembling of the heatsink that introduces a thermal fault resistance greater than 11.28K/W, the junction temperature of the transistor exceeds the maximum temperature supported. Figure 8 shows a thermal simulation in which the $R_{th,F}$ is varied from 1K/W to 50K/W. It is possible to note that for thermal resistance values higher than 11K/W the junction temperature exceeds the operating parameters of the device. The simulations were performed using the free version of the TINA SPICE simulator [21] produced by Texas Instruments.

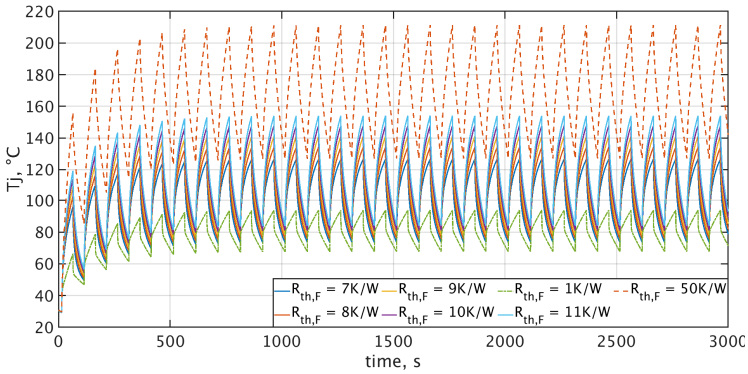


Figure 8: Thermal fault impact on Tj

VI. Conclusions

In this paper, a strategy to evaluate the effectiveness of a test procedure for checking the correct assembling and behaviour of heatsinks for power devices is proposed. Moreover, the proposed approach allows to identify the maximum thermal fault resistance value tolerated by the transistor. The proposed approach has been evaluated on an industrial MOSFET transistor used for high voltage applications. This work is preparatory to a study of the stress tests for power devices from which it is possible to obtain an estimate of the lifetime of the device considering the thermal faults in the heatsinks. The Coffin-Manson model [22] can be used to estimate the average life of a power device introducing the thermal fault concept outlined in this work.

VII. Acknowledgements

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VIII. References

[1] J. Jose, A. Ravindran, K. Nair, ”Study of Temperature Dependency on MOSFET Parameter using MATLAB,” International Research Journal of Engineering and Technology (IRJET) Volume: 03 Issue: 07, July-2016.

[2] Thermal and Power Management of Integrated Circuits, Vassighi, Arman, Sachdev, Manoj, Springer, 2006, ISBN 978-1-4419-3832-9

[3] H. Chen, B. Ji, V. Pickert, and W. Cao, ”Real-Time Temperature Estimation for Power MOSFETs Considering Thermal Aging Effects,” in IEEE Transactions on Device and Materials Reliability, vol. 14, no. 1, pp. 220-228, March 2014

[4] S. Dusmez, H. Duran and B. Akin, "Remaining Useful Lifetime Estimation for Thermally Stressed Power MOSFETs Based on on-State Resistance Variation," in IEEE Transactions on Industry Applications, vol. 52, no. 3, pp. 2554-2563, May-June 2016.

[5] T. Lin, C. Su, C. Hung, K. Nidhi, C. Tu and S. Huang, "Package and Chip Accelerated Aging Methods for Power MOSFET Reliability Evaluation," 2019 Design, Automation & Test in Europe Conference & Exhibition (DATE), Florence, Italy, 2019, pp. 1661-1666.

[6] Clyde F. Coombs, Jr.Happy T. Holden, "Printed Circuits Handbook", Seventh Edition, McGraw-Hill Education book, 2016, ISBN 9780071833950

[7] M. L. Bushnell, V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer book, 2002, ISBN 978-0-7923-7991-1

[8] Matteo V. Quitadamo, Davide Piumatti, Matteo Sonza Reorda, and Franco Fiori, "Faults Detection in the Heatsinks Mounted on Power Electronic Transistors," International Journal of Electrical and Electronic Engineering & Telecommunications (IJEETC), Doi: 10.18178/ijeetc.191001

[9] “Thermal Modeling of Power-electronic Systems,” Dr. Martin März, Fraunhofer Institute for integrated circuits IIS-B, Erlangen Paul Nance, Infineon Technologies AG, Munich, Document available on https://www.iisb.fraunhofer.de

[10] “Thermal System Modeling,” Dr. Martin März, Paul Nance, Infineon Technologies AG, Munich, Document available on https://www.infineon.com

[11] “Introduction to Infineon’s Simulation Models Power MOSFETs” Application Note AN 2014-02 V2.0 Feb. 2014, Document available on https://www.infineon.com

[12] “Power Electronics: Circuits, Devices & Applications,” Muhammad H. Rashid, University of Florida, ISBN 9788871924595

[13] “Dynamic thermal behavior of MOSFETs,” Infineon application note: AN_201712_PL11_001, available on https://www.infineon.com

[14] “PSpice Libraries for OptiMOS n-Channel Power Transistors,” available on www.infineon.com/

[15] J. Altet, Antonio Rubio, “Thermal Testing of Integrated Circuits”, Springer book, 2002, ISBN 978-1-4419-5287-5

[16] NXP, “Using RC Thermal Models,” AN11261 Rev. 2, 19 May 2014, http://www.iet.unipi.it/f.baronti/didattica/CE/Files/AN11261.pdf

[17] Recommendations for Assembly of Infineon TO Packages, Additional Information, DS1, March 2008, Infineon https://www.infineon.com/dgdl/Infineon-Package_recommendations_for_assembly_of_Infineon_TO_packages-AN-v01_00-EN.pdf?fileId=db3a30431936bc4b011938532f885a38

[18] “SPP07N60C3”, Infineon N-MOS datasheet available on https://www.infineon.com/dgdl/Infineon-SPP_A_I07N60C3-DS-v03_02-en%5B1%5D.pdf?fileId=db3a304412b407950112b42de18b490c

[19] “SPP07N60C3”, Infineon N-MOS thermal SPICE model available on https://www.infineon.com/dgdl/Infineon-SimulationModel_CoolMOS_PowerMOSFET_PSpice_600V_C3-SM-v01_00-EN.zip?fileId=db3a30433d346a2d013d4484ce694a88

[20] Mounting Guidelines for the Super-247, International Rectifier Application Note AN-997

[21] TINA-TI SPICE simulator by Texas Instruments, tool available in https://www.ti.com/tool/TINA-TI

[22] S. Dusmez, H. Duran and B. Akin, "Remaining Useful Lifetime Estimation for Thermally Stressed Power MOSFETs Based on on-State Resistance Variation," in IEEE Transactions on Industry Applications, vol. 52, no. 3, pp. 2554-2563, May-June 2016.