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Three-Legs Interleaved Boost Power Factor Corrector for High-Power LED Lighting Application

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Abstract: In this article, a three-leg interleaved boost Power Factor Corrector (IBPFC) converter for energy-efficient LED lighting systems connected to the main grid was discussed. This IBPFC circuit presented features 60 kHz of commutation frequency and up to 3 kW of power rating. The controlled rectifier front-end boost PFC supplied a DC/DC converter to drive power LEDs suitable for street lighting or a lighting system for a stadium, etc. The IBPFC operated in continuous current mode (CCM). The ripple impact of the IBPFC converter was analyzed and a novel methodology of inductance design was presented. In the proposed design approach, the derivative calculation of the current ripple peak compared with the derivative of the input current was used to define a critical inductance value to ensure the CCM condition. Experimental validation was provided on a 3kW prototype.

Keywords: interleaved converters; power factor correction (PFC); three-phase boost converter; ripple analysis; continuous current mode (CCM); high-power LED lighting; IGBT

1. Introduction

Nowadays, LED lights are gradually replacing other sources of lighting not only in households and public places, but also where the required lighting power is high, such as in street lighting, in industrial buildings, and in locations for sporting events and musical concerts [1–3].

The LEDs must be driven by a controlled DC current. However, they are usually connected to the AC electrical network [4]. Therefore, an energy conversion structure consisting of an AC/DC conversion and then a DC/DC conversion is required. The DC/DC converter supplies the correct current required for the operation of the LED array [5,6]. The AC/DC front-end is a Power Factor Corrector (PFC).

Power-factor correction is necessary to mitigate power quality problems due to reactive loads connection into the grid in order to comply with the LED performance standard IEC61000-3-2. Several PFC converter topologies are used to achieve this goal [7,8]. The boost converter is a versatile and simple circuit used to build compact, non-isolated, PFC solutions. As the required power increases, the converter efficiency and size can be optimized by adopting the interleaved boost circuit topology [9]. Interleaved PFC solutions are based on Microcontroller Units (MCUs) or specialized Integrated Circuits (ICs) regulating the current absorbed from the AC grid to maximize the Power Factor (PF) and optimize the harmonic contents [10]. For these reasons, IBPFC converters are aimed to emulate a resistor behavior from the grid side.

Since PFC converters introduce additional power losses compared to a simple diode rectifier, and therefore reduce the overall converter efficiency, the choice of the topology and electronic components must be accurate [11]. The IBPFC topology with two or more interleaved legs ensures the reduction of the Root-Mean-Squared (RMS) current value on the semiconductor switches and the maximum current

ripple. The IBPFC leads to advantages on both the power devices and the inductor-legs size [12]. The interleaved topologies provide further advantages, such as:

- Magnetics components size can be reduced;
- Reduced electromagnetic contents and Electromagnetic Interference (EMI) filter;
- RMS current rating decrease in the output capacitance;
- Suitable tailoring of power semiconductor devices;
- Reduction of conduction losses thanks to the parallel structure.

As a drawback, the complexity of the control circuit increases by increasing the number of boost legs in parallel.

In this article, a three-leg IBPFC converter operating in CCM was presented and described with the advanced Insulated Gate Bipolar Devices (IGBT) as switches. The IBPFC circuit was applied in a grid-connected, high-power LED lighting. The LED drive global system was composed as described in the block diagram of Figure 1. The AC grid voltage was rectified into DC by a bridge diode rectifier and a PFC circuit. The EMI filter was necessary to reduce high frequency electromagnetic interference [13]. The DC voltage and current were then regulated through an insulated DC/DC converter to supply the LED light correctly. The PFC converter presented in this paper was a flexible circuit solution for LED light system up to 3 kW.

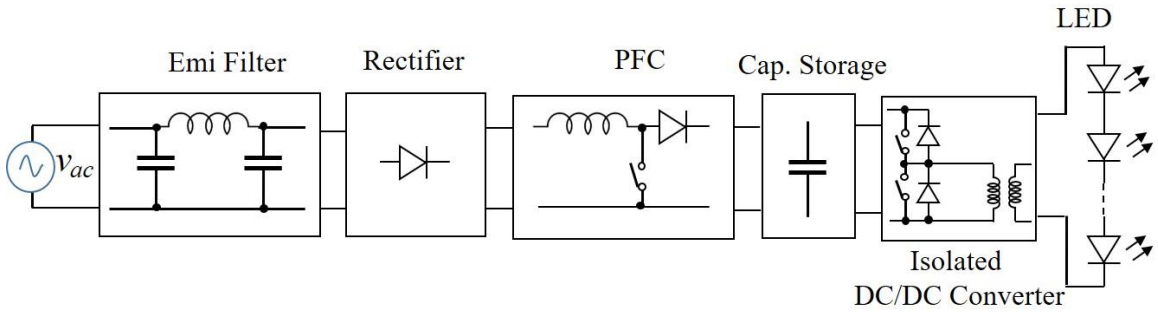

Figure 1. Block scheme of AC/DC and DC/DC conversion system for high power LED lighting.

In this article, we focused on the impact of the input current ripple in the IBPFC on CCM operation. The current ripple was investigated considering a buck-type equivalent converter as shown in the next sections. The envelope of the peak of current ripple was used to design the inductance values. From Kolar et. al. [14,15], the inductance design was based on the peak-to-peak amplitude of the input current ripple. In calculating the inductance, the ripple amplitude must not exceed the average value of the output current of the single leg of the converter to remain in CCM operation. In the design methodology presented, instead the derivative of the peak of the current, the ripple was used. The critical inductance value was found by comparing the derivative of the input current with the derivative of the peak of the current ripple, as shown in the appropriate section. The methodology presented is an alternative to the solutions proposed by the authors of [14,15] with equally valid results. The article starts with a description of the three-legs IBPFC operation. The design issues of the PFC converter are analyzed. Finally, the experimental evaluation of the described PFC circuit up to 3 kW of rated power is illustrated.

2. Three-Stage Interleaved PFC Converter Operation

In a PFC circuit, the goal is to draw the input current in phase with the input sinusoidal voltage and to arrange for a constant DC output voltage. The input current and input voltage must have a PF very close to unity using a suitable control circuit.

The topology implemented as the PFC circuit is a unidirectional boost converter with IGBTs as switches and fast diodes. In power system applications ≥ 1 kW, several boost converter modules

are connected in parallel obtaining an interleaved solution. The boost interleaved PFC increases the power capability and the current ripple variation both in the input and output converter stage [14]. The command signals of the switches are supplied in out of phase mode according to

$$phase\ shift = \frac{360}{N_C} \tag{1}$$

where N_c is the quantity of legs in the interleaved boost circuit. In the proposed IBPFC application, a three-leg boost is considered to arrange a relatively higher-power circuit optimizing the size of the power devices and reactive components, such as single-stage inductors. The adopted circuit scheme of a three-legs boost converter is depicted in Figure 2a. The power devices are driven by a proper phase-regulator circuit (with the correct phase-shift). In the following analysis, it was supposed that the converter circuit worked in a steady state. Moreover, the converter was in CCM operation. From the classic analysis of the boost converter, one can derive the basic law that links the input voltage v_{in}, the duty cycle of the single controlled switch d_{sw}, and the output voltage v_{out}.

$$v_{out} = \frac{v_{in}}{1 - d_{sw}} \tag{2}$$

where the on period $t_{on,sw}$ of the controlled switch is equal to

$$t_{on,sw} = d_{sw} \cdot T_{sw} \tag{3}$$

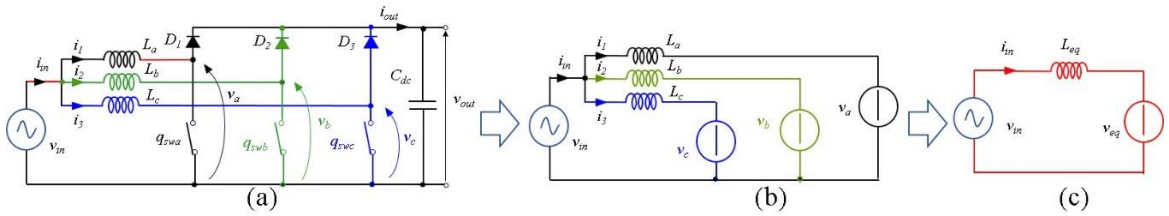

Figure 2. (**a**) Three-stage interleaved boost PFC circuit schematic, (**b**) equivalent averaged-circuit model circuit, (**c**) Thevenin equivalent circuit.

For the analysis of the current ripple on the input side, it is easier to use the conventions of the buck converter. Moreover, the current ripple (Δi_{pk}) does not depend on the average current transferred, but only on the integral of the voltage applied to the inductance.

Based on this choice, the duty cycle D is defined as

$$D = \frac{v_{in}}{v_{out}} \tag{4}$$

where $d_{sw} = 1 - D$.

In the three-leg arrangement, three diverse operating zones can be recognized in relation of the duty cycle variation [16].

1. $D < \frac{1}{3}$
2. $\frac{1}{3} < D < \frac{2}{3}$
3. $\frac{2}{3} < D < 1$

To simplify the analysis, the equivalent circuit adopting the averaged-circuit model of the three phase PFC topology is considered, as depicted in Figure 2b. Considering the input converter stage, the Thevenin equivalent circuit is obtained and described in Figure 2c. The analysis is oriented to know the behavior of the input current, i_{in}. For this reason, the equivalent voltage v_{eq}, related to Figure 2c is introduced.

$$v_{eq} = \frac{v_a + v_b + v_c}{3} \tag{5}$$

where v_a, v_b, and v_c are the voltage across the switches, respectively, q_{swa}, q_{swb}, q_{swc} (Figure 2a).

Considering the equivalent circuit of Figure 2c, an equivalent inductor L_{eq} is also presented:

$$L_{eq} = \frac{L}{3}, \quad v_{Leq} = v_{eq} - v_{in} \tag{6}$$

where L is the single stage inductor ($L = L_a = L_b = L_c$ of Figure 2a).

The methodology adopted can be extended to n switching cells, considering, respectively:

$$v_{eq} = \frac{\sum_{i=1}^{n} v_i}{n}, \; L_{eq} = \frac{L}{n} \tag{7}$$

2.1. D < 1/3 Control Condition

The case of D less than one-third the qualitative waveforms is reported in Figure 3. Figure 3a shows a time spacing of the gate signal commands of the active switches present in the circuital topology. In Figure 3b, the three-leg voltages v_a, v_b, and v_c, are reported and compared with the ideal input voltage v_{in}. In Figure 3c, the voltage stimulus v_{eq} has a frequency $3{\cdot}f_{sw}$ (f_{sw} is the switching frequency) and an amplitude of one-third. The equivalent voltage is in the range of

$$v_{eq} = \left[0, \; \frac{1}{3} v_{out}\right] \tag{8}$$

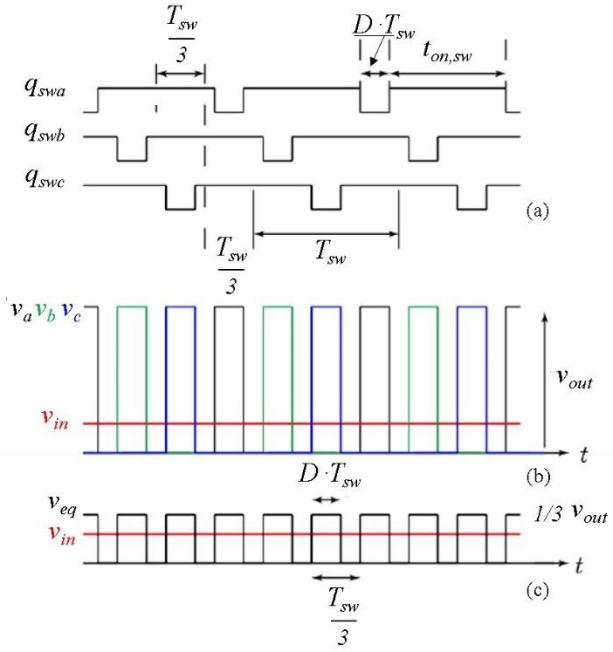

Figure 3. Switching waveforms behavior in the case of $D < 1/3$. (**a**) Gate control signal, (**b**) single-stage voltage behavior compared with the input voltage v_{in}, (**c**) equivalent voltage behavior. It shows a frequency $3{\cdot}\, f_{sw}$ compared to the v_a, v_b, and v_c voltages, while the amplitude is one-third.

Taking into account the equivalent voltage, it is feasible to compute the variation of the total equivalent magnetic flux related to Figure 2c. It is calculated through the voltage across of the equivalent inductance above mentioned by means of a mathematical integration. In this way, the magnetic flux peak is achieved:

$$\Delta\psi_{pk,eq} = \frac{1}{2} \cdot T_{sw} \cdot D \cdot \left(v_{eq} - v_{in}\right) \tag{9}$$

Processing (9), the following is obtained:

$$\Delta\psi_{pk,eq} = \frac{1}{2}\cdot T_{sw}\cdot v_{out}\cdot D\cdot\left(\frac{1}{3}-D\right) \tag{10}$$

In D = 1/6, the maximum peak flux ripple is achieved, from which:

$$\Delta\psi_{pk,eq} = \frac{1}{2}\cdot T_{sw}\cdot v_{out}\cdot\frac{1}{6}\cdot\left(\frac{1}{3}-\frac{1}{6}\right) = \frac{1}{72}\cdot T_{sw}\cdot v_{out} \tag{11}$$

2.2. 1/3 < D < 2/3 Control Condition

Figure 4 shows the generic situation with duty cycle between 1/3 and 2/3. In this case, the equivalent voltage is in the range:

$$v_{eq} = \left[\frac{1}{3}v_{out},\ \frac{2}{3}v_{out}\right] \tag{12}$$

Using the same computational approach of the previous case, the flux equivalent ripple variation is:

$$\Delta\psi_{pk,eq} = \frac{1}{2}\cdot T_{sw}\cdot v_{out}\cdot\left(D-\frac{1}{3}\right)\cdot\left(v_{eq}-v_{in}\right) \tag{13}$$

Taking into account the extreme value of the range of v_{eq} in Equation (12), the peak of the equivalent flux is given by:

$$\Delta\psi_{pk,eq} = \frac{1}{2}\cdot T_{sw}\cdot v_{out}\cdot\left(D-\frac{1}{3}\right)\cdot\left(\frac{2}{3}-D\right) \tag{14}$$

The maximum flux peak occurred for $D = \frac{1}{2}$ and is equal to the value found in Equation (11).

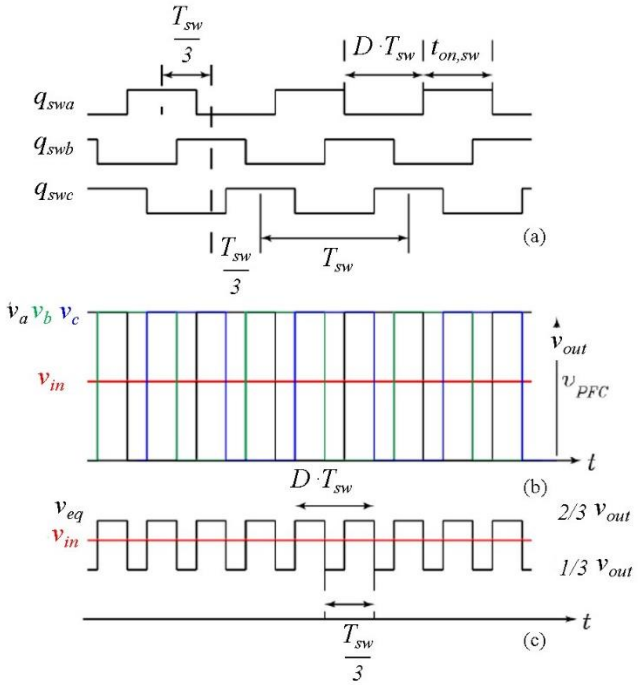

Figure 4. The qualitative waveforms for 1/3 < D < 2/3. (**a**) The device control signal, (**b**) the devices switching voltage, (**c**) the equivalent voltage behavior.

2.3. $D > 2/3$ Control Condition

Qualitative waveforms in the operative conditions with $D > 2/3$ are depicted in Figure 5. In this case, the equivalent voltage is in the range:

$$v_{eq} = \left[\frac{2}{3}v_{out},\ v_{out}\right] \tag{15}$$

By means the same approach as in the previous cases, the peak flux is obtained as:

$$\Delta\psi_{pk,eq} = \frac{1}{2}\cdot T_{sw}\cdot v_{out}\cdot\left(D-\frac{2}{3}\right)\cdot(1-D) \tag{16}$$

The maximum peak for the magnetic flux is obtained with $D = 5/6$, similarly to Equation (11). As shown in Figures 3–5, this control mode guarantees five levels of the input voltage modulation.

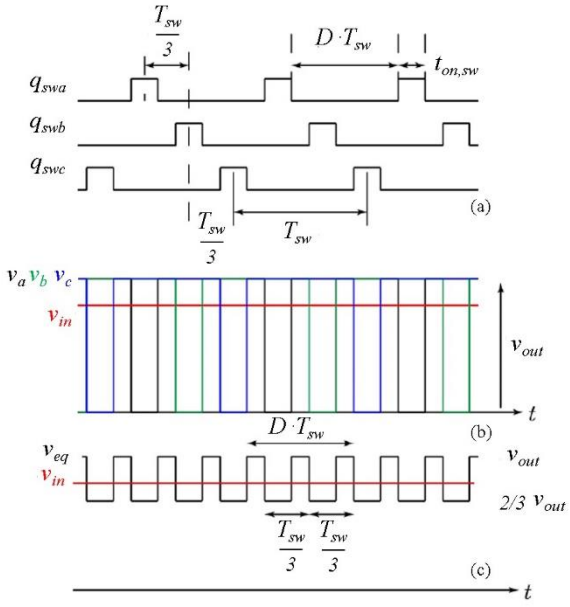

Figure 5. The qualitative switching waveforms in the case of $D > 2/3$. (**a**) The gate signal control, (**b**) the devices switching voltage, (**c**) the equivalent voltage variation.

2.4. Converter Behavior within the Whole Operating Range

From Equations (10), (14), and (16), equivalent peak of the flux ripple versus D can be graphed. The input peak of current ripple is:

$$\Delta i_{pk,Leq} = \frac{\Delta\psi_{pk,eq}}{L_{eq}} \tag{17}$$

Assuming a concrete case of study with T_{sw} = 1/60 kHz, an output voltage v_{out} = 400 V, and a leg inductance L = 900 µH, the ripple curves obtained for the three-leg IBPFC are depicted in Figure 6a (magnetic flux), while the peak of the input current ripple is reported in Figure 6b. The maximum peak value from Equation (11) is $\Delta\psi_{pk,eq\_max}$ = 92.59 µVs. In Figure 6b, the maximum current peak obtained by Equation (17) is $\Delta i_{pk,Leq}$ = 0.309 A.

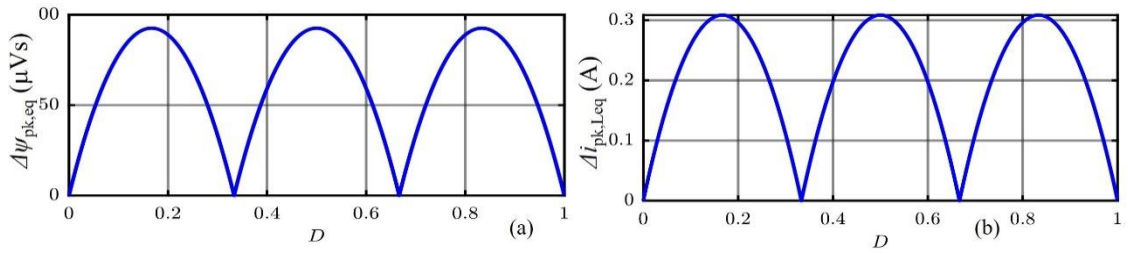

Figure 6. (**a**) Ripple of magnetic flux behavior for the three-leg IBPFC, (**b**) total ripple current behavior. Design parameters f_{sw} = 60 kHz, v_{out} = 400 V and L = 900 μH.

In Figure 6a, three peak points for the flux for the three control conditions with two ripple free points in D = 1/3 and D = 2/3 are observable. The same qualitative considerations can be made for current ripple. It must be noted that the three boost legs are subject to the same stress in terms of ripple, even changing the number of parallel legs. The advantage of paralleling legs consists in reducing the equivalent ripple stress on the grid side and the DC side. The only stress reduction in the single boost legs is represented by the reduction of the processed power by every single leg, which is equivalent to the entire power divided by the number of legs.

The input current ripple is influenced by the factors that shape its variation, such as the output current and both input and output voltage. In specific operating conditions, the current can move from the CCM condition to the Discontinuous Conduction Mode (DCM). The DCM can present control issues, especially with digital controllers. Critical operating conditions are useful for designing the value of the inductor L to maintain the CCM for the interleaved boost converter and therefore avoiding risks of loss of control. In the following section, the same design issues for the actual PFC converter are discussed.

3. Interleaved Boost PFC Design Issues

The design procedure of the L_{eq} inductor starts by considering the PFC in ideal operating conditions. The input voltage is sinusoidal. It is given by

$$v_{in}(t) = V_{max} \cdot \sin(\omega t) \tag{18}$$

In the ideal case, the input current is

$$i_{in}(t) = I_{max} \cdot \sin(\omega t) \tag{19}$$

The correct design of the inductor L_{eq} must guarantee that the PFC converter works in CCM within the operating power range. The critical value of the inductance design is related to the worst working conditions. In this case, the DCM operation may be reached. The worst condition occurs at a maximum input voltage, $V_{in,max}$ at minimum input current $I_{in,min}$ and maximum current ripple amplitude $I_{pk,Leq}$. In the case study considered, the main project constraints are shown in Table 1.

Table 1. Main inductor design constraints.

$V_{in,max}$ [V]	$P_{out,min}$ [W]	V_{out} [V]	f_{sw} [kHz]	η_{min}
264.5	1000	400	60	0.95

The critical inductance computation depends on the input current peak value. To understand the trend of the peak of the current ripple an inductance of L_{eq} = 300 μH is taken into account. From Equation (17), the peak of current ripple can be estimated, as shown in Figure 7. By means of the peak

current ripple, the upper and lower envelopes of the actual current flowing in the equivalent inductor can be plotted. The current i_{up} (t) and i_{low} (t) are given by

$$i_{up}(t) = i_{in} + \Delta i_{pk,Leq} \tag{20}$$

$$i_{low}(t) = i_{in} - \Delta i_{pk,Leq} \tag{21}$$

During working conditions, the instantaneous current of the inductor was included within the peak ripple envelopes.

By comparing the trend of the input current and the peak of the ripple current flowing in L_{eq}, it is possible to find a design condition to obtain the value of the critical inductance. In Figure 8, the view of the input current and the current peak trended very close to zero in the case of two inductance values L_{eq} = 900 µH, Figure 8a and L_{eq} = 300 µH, Figure 8b at the output power of 400 W. From the inspection of Figure 8, it is observable that as the inductance decreased, the slope of the $i_{pk,Leq}$ increased, becoming greater than the one of the input current. From the observation of the waveforms related to the i_{low} shown in Figure 9a,b, it can be seen that when the slope of the ripple peak of the current flowing in L_{eq} was greater than the one of the input current, the converter operated in DCM. On the other hand, when the slope of the peak of the ripple of the current is lower than that of the input current, the i_{low} is always positive, resulting in CCM condition.

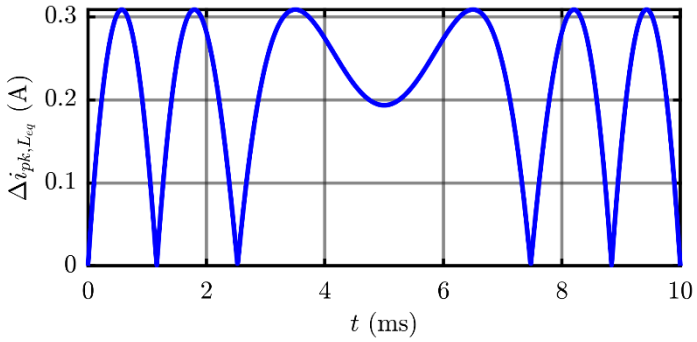

Figure 7. Current ripple peak behavior in the case of L_{eq} = 300 µH.

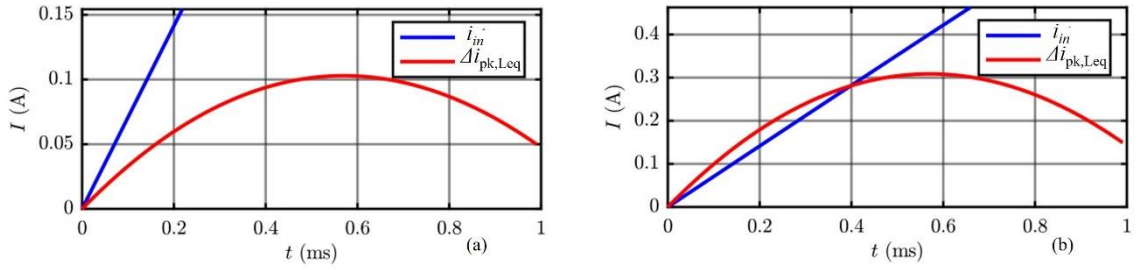

Figure 8. (**a**) Peak current ripple and input current comparison for L_{eq} = 900 µH, (**b**) Peak current ripple and input current comparison for L_{eq} = 300 µH.

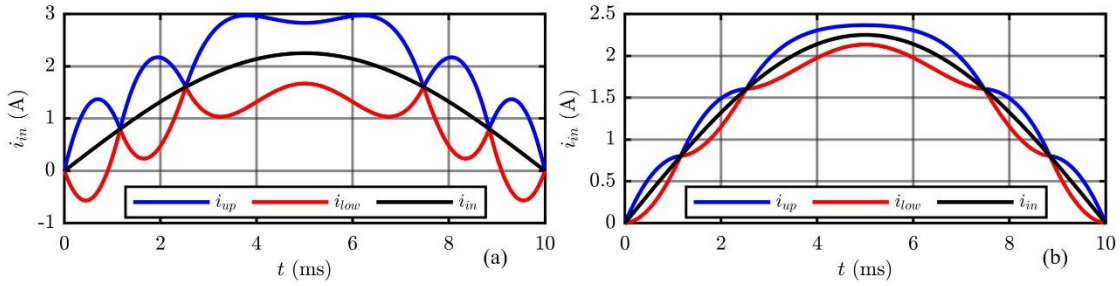

Figure 9. Input moving average current i_{in} waveform was included within the peak ripple envelopes i_{up} (t) and i_{low} (t). (**a**) Current envelopes behavior with L_{eq} = 100 µH, (**b**) current envelopes behavior with L_{eq} = 500 µH.

To ensure CCM operation, it must be imposed:

$$\frac{di_{in}}{dt}(t=0) > \frac{d\left(\Delta i_{pk,Leq}\right)}{dt}(t=0) \tag{22}$$

From Equation (22), calculating the derivatives at t = 0 of the i_{in} and the ripple peak, $i_{\text{pk,eq}}$ flowing in L_{eq}, the boundary condition to work in CCM is obtained:

$$L_{eq} > \eta \cdot \frac{T_{sw} \cdot V_{in,rms}^2}{6 \cdot P_{out}} \tag{23}$$

The mathematical steps to obtain Equation (23) are explained in Appendix A. From the data in Table 1, the critical value of L_{eq} must be greater than 185 µH.

3.1. Output Capacitor Design

Considering a single-phase AC supply, the voltage ripple on the output capacitors of the IBPFC is at two times the grid frequency. It is related also to the pulsed power that moves from input to output of the converter. The dc-link voltage v_{out} is

$$v_{out} = V_{out} \pm \Delta v_{out} \tag{24}$$

where V_{out} is the average of the output voltage, while Δv_{out} is the voltage ripple. Δv_{out} must be selected in order to allow the following constraint:

v_{out} must always be greater than $v_{in,max}$ to maintain the boost voltage conditions and v_{out} must be less than the breakdown of the diodes and power switches of the interleaved legs. Moreover, the required quality of v_{out} must be guaranteed depending on the needs of the cascaded DC/DC converter. The output capacitance C_{dc} is related to the Δv_{out} and depends on the maximum output power and the twice of angular mains frequency ω_{in} [14].

$$C_{dc} \geq \frac{P_{out}}{\Delta v_{out} \cdot V_{out} \cdot 2\omega_{in}} \tag{25}$$

In this paper, Δv_{out} has been selected equal to 2%, while P_{out} maximum is 3 kW and V_{out} = 400 V. Therefore, from (25) the capacitance $C_{dc,min}$ is equal to 1500 µF.

3.2. Power Devices Selection

The devices selected as switches in the three legs of interleaved PFC topology were trench-gate field-stop IGBTs [17]. The field-stop IGBTs combine no-punch through (NPT) and punch-through (PT) features. The last generation field-stop IGBT show remarkable short-circuit ruggedness. Short-circuit performance is useful to improve the reliability of the IBPFC [18,19]. Moreover, a positive temperature

coefficient for high collector current, similar to the MOSFETs, allows an easy parallel connection in high current converter applications [20]. Besides, the IGBTs show a better $V_{CE,sat}/E_{off}$ behavior with low E_{off} and limited tail in the turn-off current. A silicon IGBT solution is a good tradeoff among ruggedness, cost, power losses, and dynamic characteristics for the selected frequency of 60 kHz compared to silicon MOSFETs super-junction solution [21]. The breakdown voltage is related to the maximum output voltage v_{out}. The current $I_{IGBT,rms}$ at maximum output power of 3 kW in every leg was

$$I_{IGBT,rms} = \frac{1}{3} \cdot \eta \cdot \frac{P_{out}}{V_{in,min}} \tag{26}$$

where the $V_{in,min}$ was 10% less than the rated $V_{in,rms}$. The $I_{IGBT,max}$ was

$$I_{IGBT,max} = \sqrt{2} \cdot I_{IGBT,rms} \tag{27}$$

The maximum $I_{IGBT,max}$ current at the rated power of 3 kW was about 7.5 A. The devices selected were 20 A, 600 V trench-gate field-stop IGBTs. The diodes had a breakdown voltage related to the maximum voltage v_{out}. The maximum diode current of each leg was

$$I_{D,max} = \frac{1}{3} \cdot \frac{P_{out}}{V_{out,min}} \tag{28}$$

where $V_{out,min}$ was computed with Equation (24). $I_{D,max}$, at the rated power of 3 kW, was about 3 A. The selected devices were 12 A, 600 V fast switching silicon diodes.

4. Interleaved Boost PFC Experimental Evaluation

The laboratory converter setup for the experimental tests is shown in Figure 10. In Figure 10a, the electrical scheme is shown. In Figure 10b, a photo of the experimental board during a measurement test is shown. The three-cell IBPFC was controlled by a dedicated controller IC. The controller circuit chosen was a commercial integrated circuit (FAN9673), which allowed us to control the PFC boost up to three interleaved channels in CCM mode. FAN9673 acted through a leading-edge control of the average current. The proper design method of the controller circuit was described by the authors of [22]. It was fully compliant with the IEC61000-3-2 specification.

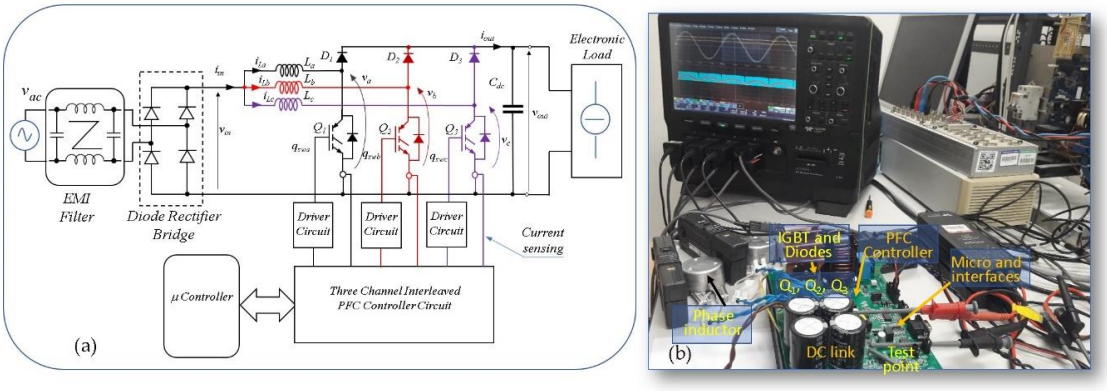

Figure 10. (**a**) Interleaved three cells boost interleaved PFC converter set-up with controller circuit. The PFC circuit is linked to a full-bridge diode rectifier, an electronic load to emulate a current constant load is connected to the converter output. (**b**) Photo of measurement setup.

Furthermore, the controller IC applied a suitable enabling function to the switches. It enabled the number of boost-legs necessary based on the output current demand. At low output current, a single cell was enabled (with the output current less than one-third of the maximum current managed by the

controller). Then, the operation of two or three switching stages was enabled in case a larger load must be supplied. The management of the switch-enabling function optimized the IBPFC efficiency.

The microcontroller unit (MCU) used (Figure 10a) was an STM32F446RE from STMicroelectronics. The microcontroller was programmed in C language to emulate the demands of the LED lighting load. In particular, it provides the PFC controller a feedback on the required DC load. In this way, the FAN9673 controller IC knows how to turn on or off the IBPFC legs as the power level changes. The user interface with the MCU was provided by an SPI and CAN communication, which can be used in a later stage for the control of the whole converter system. As shown in the previous section, the interleaved solution produced a remarkable decrease in both input and output currents ripple. The benefits of the ripple act on the conducted EMI filtering size and cost reduction [23]. The correct PCB layout design is a further important issue to mitigate EMI levels of the converter systems. In the actual realization of the experimental prototype, the DC/DC converter and the LED load are emulated by a constant current controlled electronic load. In the experimental prototype, only the IBPFC was investigated. The electronic load allowed us to establish the IBPFC output current based on the number and power required of the LED lighting system to be implemented.

The main PFC electrical parameters in the actual experimental prototype are reported in Table 2. The choice of L = 900 µH for each leg allowed us to obtain a large margin to CCM operative conditions compared with the minimum power rate of 1000 W of the design constraints (Table 1). From Equation (23), it was possible to compute the minimum power boundary in CCM operative conditions for a selected L_{eq} = 300 µH to obtain $P_{out,min}$ in CCM equal to 1000 W. The experimental switching waveforms at a rated power of P_{in} = 3000 W in working conditions using all three legs of the PFC boost interleaved are reported in Figure 11. In this operative condition, the main electrical quantities can be extracted from Table 3.

Table 2. Main PFC electrical parameters of the experimental prototype.

V_{in} [V]	V_{out} [V]	P_{out} [W]	f_{SW} [KHz]	$L_a = L_b = L_c$ [µH]	C_{dc} [µF]
230 ± 10%	400	3000	60	900	1800

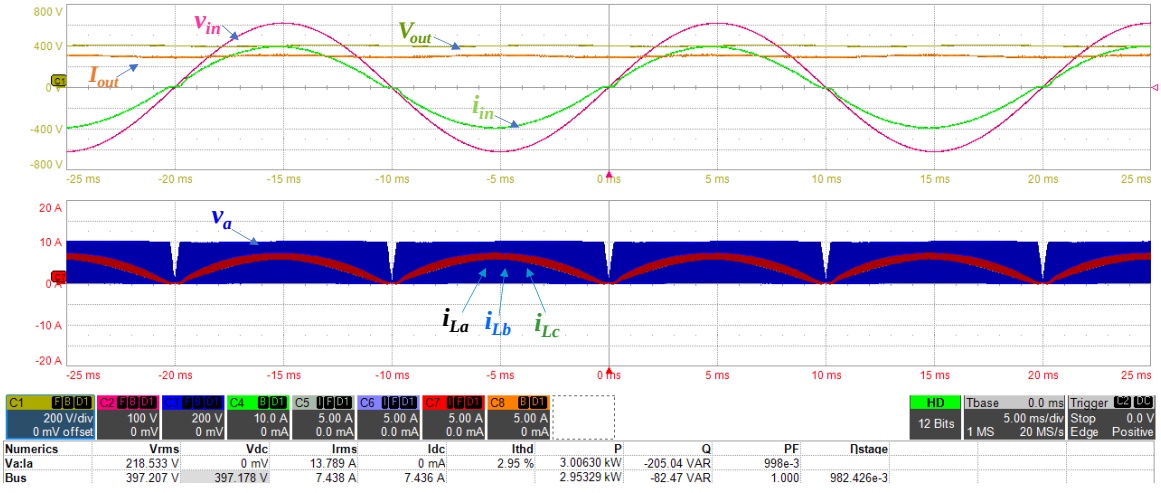

Figure 11. Switching waveforms of three cells interleaved PFC converter. v_{in} = 100 V/div, i_{in} = 10 A/div, V_{out} = 200 V/div, I_{out} = 5 A/div, $i_{La} = i_{Lb} = i_{Lc}$ = 5 A/div, v_a = 200 V/div, P_{in} = 3 kW, t = 5 ms/div.

Table 3. Main IBPFC Electrical quantities at a different input power.

N	P_{in} [kW]	$i_{in,rms}$ [A]	I_{out} [A]	i_{THD}	PF	η	N of Cells
1	1	4.6	2.5	2.76	0.995	0.975	1
2	1.5	6.8	3.6	3.94	0.994	0.982	2
3	2	9.2	4.9	2.80	0.997	0.986	2
4	2.5	11.5	6.2	3.32	0.996	0.988	3
5	3	13.8	7.4	2.95	0.998	0.982	3

The switching waveforms at P_{in} = 1 kW are reported in Figure 12. In this operative condition, the controller works by making only one leg work. From the inspection of Figure 12, the increase of input current ripple clear appeared, which was compared with the same current waveform depicted in Figure 11.

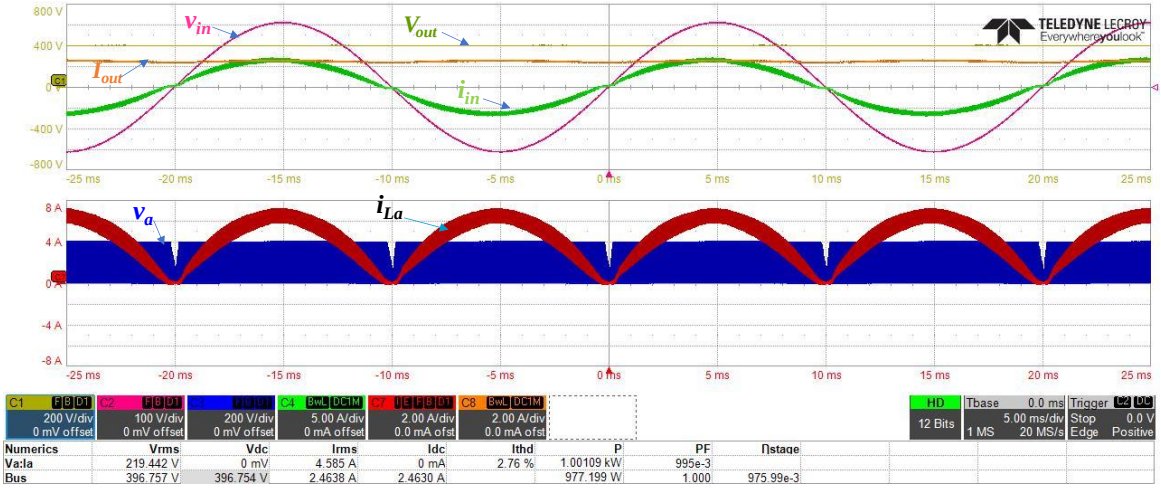

Figure 12. Switching waveforms of boost PFC converter at P_{in} = 1 kW with only one working cell. v_{in} = 100 V/div, i_{in} = 10 A/div, V_{out} = 200 V/div, I_{out} = 5 A/div, i_{La} = i_{Lb} = i_{Lc} = 5 A/div, v_a = 200 V/div, t = 5 ms/div.

Furthermore, the converter, as shown in Figure 12, worked in CCM condition as estimated in the design constraints. The main electrical quantities, such as the current Total Harmonic Distortion (THD), the power factor, and the efficiency of the PFC, are reported in Table 3 at different input powers. The THD is a significant parameter to control in electronics equipment connected to the grid and it should be maintained at a low value to obtain a quality in main network waveforms. Lower values of THD in power electronic converter applications lead an increasing power factor with lower peak currents. Also, the efficiency can be improved [24]. In Figure 13, the current THD (Figure 13a), the power factor (Figure 13b), and the converter efficiency (Figure 13c) are depicted. The graphs depicted in Figure 13 show, at a glance, the quite satisfactory behavior of the main electrical quantities of the PFC converter. In high-performance LED drivers, THD is efficiently mitigated and is less than 10%. The THD percent in the proposed interleaved boost PFC application was less than 6% in the power range of 1–3 kW. Since the number of operating cells is correlated to the load current demand [25]. The currents in the switches of the PFC changed, as reported in the three different working conditions described in Figure 14.

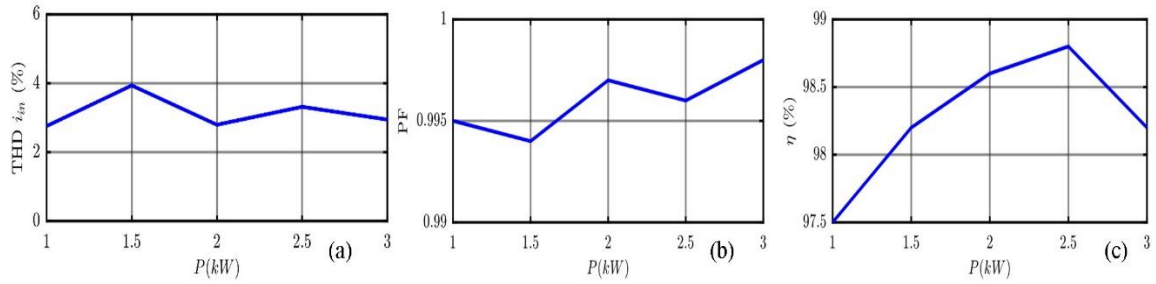

Figure 13. The graphic behaviors of the current THD (**a**), the power factor, (**b**) and the converter efficiency, and (**c**) of the interleaved three cells PFC front-end converter in the range of 1–3 kW.

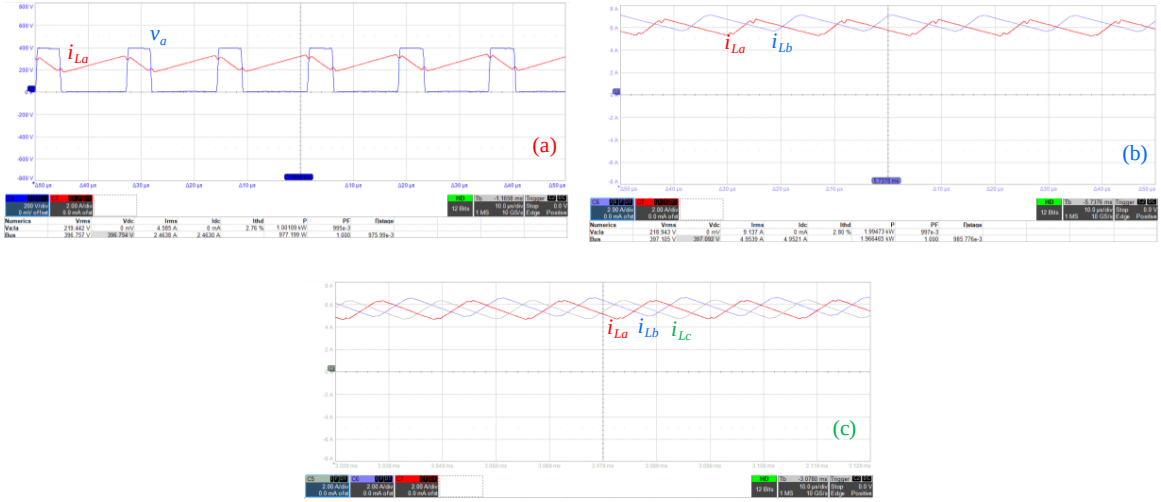

Figure 14. The inductor current waveforms behaviors of the interleaved cells intervention at load current request variation. (**a**) P_{in} = 1 kW, (**b**) P_{in} = 2 kW, (**c**) P_{in} = 3 kW. $i_{La} = i_{Lb} = i_{Lc}$ = 2 A/div, v_a = 200 V/div, t = 10 s/div.

In Figure 14a, a single-leg PFC worked based on the output of the current requested. The i_{La} and v_{a} waveforms are shown at input power, P_{in} = 1 kW. In Figure 14b, P_{in} = 2 kW, in this case, two cells were switched in a suitable phase-shift way. The currents related to leg a (i_{La}) and leg b (i_{Lb}) are reported. Finally, in Figure 14c, three legs operated (P_{in} = 3kW), and the currents i_{La}, i_{Lb}, and i_{Lc} are shown.

5. Discussion

In the high-power LED lighting driver connected to the grid, a PFC converter is a crucial power electronic system in the design of industrial lighting performing equipment. The topological solution of the interleaved boost PFC was used when the power required by the load was higher by paralleling different cells of the converter. Despite the use of the extra legs, there were advantages both in the converter efficiency and size. The frequency of the input and output current ripple is the number of legs multiplied by the switching frequency f_{SW}, thus reducing the required input filter and boost inductors compared to a single leg solution. The design issues of the interleaved boost PFC converter were dealt by deriving the equivalent circuit, where the attention was focused on the transfer function between v_{in} and v_{out} by introducing a duty cycle as the ratio of these two voltages. Looking at the equivalent circuit, a different method was obtained, which allowed us to analyze the dynamics of the electrical quantities related to the equivalent inductance to find an original design criterion of the equivalent inductance which takes into account the envelope of the current ripple. An experimental PFC prototype was implemented, and several tests in the range of 1–3 kW were carried out. The power switches used are the last generation of IGBT devices with fast silicon diodes to realize the

three interleaved boost cells with a switching frequency of 60 kHz. A commercial control circuit was applied to achieve a leading-edge average current method. The control circuit implemented a channel management operation. This enabled a different number of legs based on the load current request, optimizing the converter performance and the devices stress. The measured THD, power factor, and efficiency were quite satisfactory, and the PFC converter was a cost-effective solution thanks to use of IGBT devices instead of SIC or super junction MOSFETs.

The next steps were aimed at the engineering of the prototype and the construction of a complete driving system AC/DC (PFC just presented) and DC/DC (constant current converter in developing stage) for high-power density LED lighting systems with high performance and reduced costs.

6. Conclusions

In this article, a flexible three-leg IBPFC converter suitable for high-power LED driver circuit connected to the grid was presented and discussed. The PFC analysis and design were deeply analyzed, defining the constraints and methods of designing passive components, such as the inductors and output capacitor. Moreover, the power devices selection criteria were considered.

An experimental evaluation of the PFC performances in terms of efficiency, power factor, and THD were carried out in the power range of 1–3 kW. A dedicated control circuit IC was considered in the converter prototype implementation, which enabled the correct number of cells depending on the load consumption. The flexible number of cells achieved an optimized converter performance in terms of efficiency and devices stress. The power switches used in the converter application were field-stop trench-gate IGBT devices and fast silicon diode. The power switches choice permitted quite satisfactory performance at a cost-effective solution.

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Appendix A

The CCM operating condition was obtained by imposing Equation (22);
From Equation (19):

$$i_{in} = I_{max} \sin \omega t = \sqrt{2} \cdot \frac{P_{out}}{\eta \cdot V_{in,rms}} \sin \omega t \tag{A1}$$

$V_{in,rms}$ is the maximum value of RMS value of v_{in}:

$$\frac{di_{in}}{dt}(t) = \sqrt{2} \frac{\omega \cdot P_{out}}{\eta \cdot V_{in,rms}} \cos \omega t \tag{A2}$$

$$\frac{di_{in}}{dt}(t=0) = \sqrt{2} \frac{\omega \cdot P_{out}}{\eta \cdot V_{in,rms}} \tag{A3}$$

$$\Delta i_{pk,Leq} = \frac{\Delta \psi_{pk}(t)}{L_{eq}} = \begin{cases} \frac{1}{2} \cdot \frac{T_{sw} \cdot v_{out}}{L_{eq}} D(t) \cdot \left(\frac{1}{3} - D(t) \right) & 0 \le D \le \frac{1}{3} \\ \frac{1}{2} \cdot \frac{T_{sw} \cdot v_{out}}{L_{eq}} \cdot \left(\frac{2}{3} - D(t) \right) \cdot \left(D(t) - \frac{1}{3} \right) & \frac{1}{3} < D \le \frac{2}{3} \\ \frac{1}{2} \cdot \frac{T_{sw} \cdot v_{out}}{L_{eq}} \cdot \left(D(t) - \frac{2}{3} \right) \cdot (1 - D(t)) & \frac{2}{3} < D \le 1 \end{cases} \tag{A4}$$

with

$$D(t) = \frac{\sqrt{2} \cdot V_{in,rms}}{v_{out}} \sin \omega t = \frac{v_{in}(t)}{v_{out}} \tag{A5}$$

The derivative operation of the function takes place around $t = 0$ for which the time interval was considered:

$$0 \le D \le \frac{1}{3} \tag{A6}$$

$$\frac{d\left(\Delta i_{pk,Leq}\right)}{dt} = \frac{A \cdot B \cdot \omega}{3} \cos \omega t - 2 \cdot A \cdot B^2 \cdot \omega \cos \omega t \cdot \sin \omega t \tag{A7}$$

where

$$A = \frac{1}{2} \frac{T_{sw} \cdot v_{out}}{L_{eq}},\ B = \frac{\sqrt{2} \cdot V_{in,rms}}{v_{out}} \tag{A8}$$

In $t = 0$:

$$\frac{d\left(\Delta i_{pk,Leq}\right)}{dt}(t = 0) = \frac{A \cdot B \cdot \omega}{3} = \frac{\sqrt{2}}{6} \cdot \frac{T_{sw} \cdot V_{in,rms} \cdot \omega}{L_{eq}} \tag{A9}$$

From Equation (22);

$$\frac{\sqrt{2} \cdot \omega \cdot P_{out}}{\eta \cdot V_{in,rms}} > \frac{\sqrt{2}}{6} \cdot \frac{T_{sw} \cdot V_{in,rms}}{L_{eq}} \tag{A10}$$

By processing Equation (A10), Equation (23) was obtained. The minimum output power to work in CCM was obtained from Equation (23):

$$P_{out,min} = \eta \cdot \frac{T_{sw} \cdot V_{in,rms}^2}{6 \cdot L_{eq,crt}} \tag{A11}$$

where

$$L_{eq,crt} = \eta \cdot \frac{T_{sw} \cdot V_{in,rms}^2}{6 \cdot P_{out,min}} \tag{A12}$$

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