A low-power mixed-signal ASIC for readout of SiPM at cryogenic temperature

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A low-power mixed-signal ASIC for readout of SiPM at cryogenic temperature

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ALCOR is a mixed-signal ASIC developed to readout silicon photomultipliers at low temperature. The chip is designed in a 110 *nm* CMOS technology. Both single photon counting and Time-over-Threshold operating modes are supported. In single photon counting mode an event rate of up to 5 *MHz* per channel can be accommodated. The time resolution is 50 *ps* and the target power consumption is less than 5 *mW* per channel. The architecture of a first 32-channel prototype is described. Dedicated test structures to qualify critical building blocks at cryogenic temperature are reported.

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1. Introduction

There is a growing interest in operating Silicon Photo-Multipliers (SiPMs) at cryogenic temperatures [1]. The strongly suppressed dark count rate observed at liquid Xenon and liquid Argon temperatures makes such sensors ideally suited to equip large area detectors like those needed in dark matter and neutrino experiments [2, 3]. Research programs to explore the possibility of building total body PET scanners based on noble liquids readout by SiPM are also ongoing [4, 5]. ALCOR (A Low-power Circuit for Optical sensor Readout) is a first prototype of an ASIC optimised to readout SiPMs at low temperature. The design of chips working at cryogenic conditions entails however several issues. The threshold voltage increases, while the higher carriers mobility may induce an accelerated device ageing. The latter effect can be partially mitigated by avoiding minimum length transistors and/or reducing the power supply voltage [6]. Furthermore, transistor and digital standard cells models below $-40°C$ are usually not provided by the technology vendor. To gain useful insights in view of the design of ALCOR, selected test structures were fabricated in a dedicated Test Chip (TC). The TC includes a copy of the front-end amplifier, a bandgap reference voltage, LVDS transmitters, standard digital gates, clock buffer and a synchronisation circuit. This paper describes the key characteristics of ALCOR and focuses on the measurements obtained on the LVDS transmitter and on the synchronisation circuit.

2. ALCOR ASIC

ALCOR is a mixed-signal 32-channel integrated circuit designed in a 110 *nm* CMOS technology. The ASIC has an area of 4.95 *mm x* 3.78 *mm*. The chip core operates at a 1.2 V, while the LVDS I/Os are powered at 2.5 V. The single channel, shown in Figure 2, occupies an area of 500 μm *x* 500 μm and can be configured to operate either in single photon counting or in Time-over-Threshold (ToT) mode. In the first mode, the arrival time of each photon is recorded. The ToT mode is useful when many photons pile-up in the individual SiPM pixel and they are treated by the electronics as a single continuous signal. The channel embeds a regulated common-gate input stage that acts as the interface between the sensor and the rest of the chain. After the input stage, the signal is fed to two amplifiers with independently programmable gain and shaping time. Each amplifier is connected to a dedicated discriminator with configurable threshold. In ToT mode the two branches work with different gains. This allows to optimise the dark count rejection and the accuracy of the charge measurement. Two leading edge discriminators with configurable threshold generate the trigger CMOS signals that are fed to the channel digital control block. The timing information consists of a coarse part derived from a binary 15-bit counter and a 9-bit fine part generated by low-power time-to-digital converters (TDCs). The bin size and the clock frequency determine the dead time of TDCs, which is 150 *ns* for a clock of 320 MHz and a bin size of 50 *ps*. The digital control logic enables the TDCs according to the operation mode whenever it receives a trigger signal. When ALCOR operates in single-photon detection mode, the four TDC work in stand-alone so as to accommodate a 5 MHZ input data rate. While in ToT operation mode, two TDCs are used for the rising edge of the trigger and the remaining two TDCs are reserved for the trailing edge of the trigger. At the end of the conversion, the data control logic generates a 32-bit payload containing the time-stamp, the channel ID and the specific TDC address. Payloads

are firstly queued and stored in a FIFO register in the channel. They are then transmitted to the periphery of the chip, where the End-of-Column (EoC) collects data from channels and acts as the interface between the channels and outside world. Configuration signals are provided to EoC using an SPI interface, while four LVDS drivers are used to transmit data off-chip. Each output link works in double data rate mode with a maximum transmission speed of 640 $Mbit/s$. The main specification of the ASIC are summarized in Table 1.

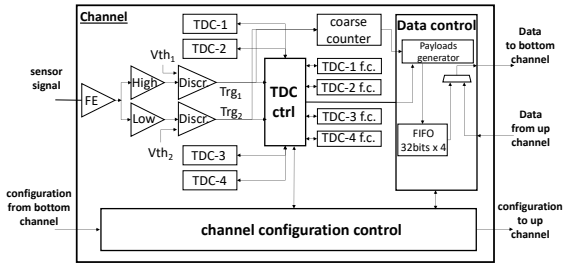

Figure 1: Schematic block of the single channel.

Parameter	Value
Input capacitance	5 nF
Data rate	5 MHz/ch
Input charge	$0.2-4$ pC
Clock frequency	$40-320$ MHz
Time resolution	50 ps
Power consumption	$<$ 5 mW/ch

Table 1: ALCOR design specifications

3. Experimental set-up and Test Chip results

The test setup allows to evaluate the timing performance of digital circuitry at both room and cryogenic temperatures. The TC ASIC is wire bonded to a custom PCB. The test board includes SMA connectors to provide the clock and asynchronous signal, and to read the LVDS output of the synchronised signal. Two commercial LDOs are used to regulate the power supply of 1.2 V for the digital circuits and 2.5 V for the LVDS transmitters. A clock generator and a digital pattern generator provide the external stimuli, while the output signals are captured by an oscilloscope with a sampling frequency of 10 GS/s. The test at cryogenic temperature has been done at 77 K cooling the TC in a bath of liquid nitrogen. Among the implemented test structures, the LVDS driver is particularly interesting because it is a mixed-signal design combining digital gates with analog circuitry, including blocks, such as the common mode feedback loop, which can be prone to stability issue. In addition, it employs transistors on two different power domains. The LVDS is tested providing a non-return-to-zero (NRZ) bit stream of a Pseudorandom Binary Sequence (PRBS) of $2^{31}-1$ pattern length to the digital buffer and the differential output is then monitored and analysed through the oscilloscope. The test has been performed at 320 MHz, which is the maximum clock frequency settable for ALCOR. Figure 2 and Table 2 show a higher amplitude and rise/fall time for 77 K measurements respect to 300 K measurements, while maintaining a similar width and S/N at both temperature. The synchronisation circuit is a critical block of ALCOR because it has been implemented to synchronise hand shaking signals between the single channel and EoC. A synchronisation delay error can lead to the loss of data and therefore may compromise the ASIC functionality. A dedicated test at cryogenic temperature is necessary in order to asses the functionality of this module and have a comparison with SPICE simulations. Figure 3 shows a simplified schematic of the module. The input pad protection and the output LVDS driver are omitted in the drawing. For a better understanding of the bheaviour of the digital circuit, the timing diagram of the synchronisation clock period is reported on the right.

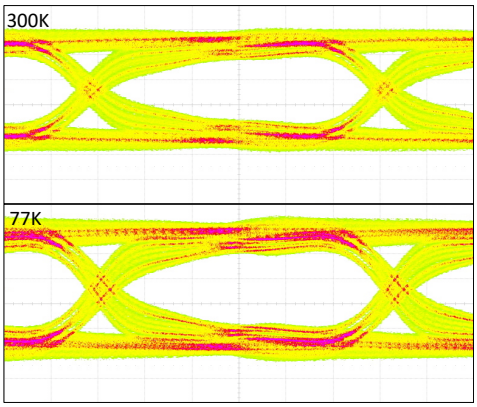

Figure 2: Eye diagram of LVSD transmitter at 320 MHz.

	320 MHz	
	300 K	77 K
Level 1 (mV)	394	465
Level 0 (mV)	-405	-467
Rise Time (ps)	522	752
Fall Time (ps)	597	838
Eye Amp (mV)	799	932
Eye Height (mV)	196	212
Eye Width (ns)	2,63	2,52
Eye S/N	3,97	3,88

Table 2: Eye diagram parameters at different temperatures.

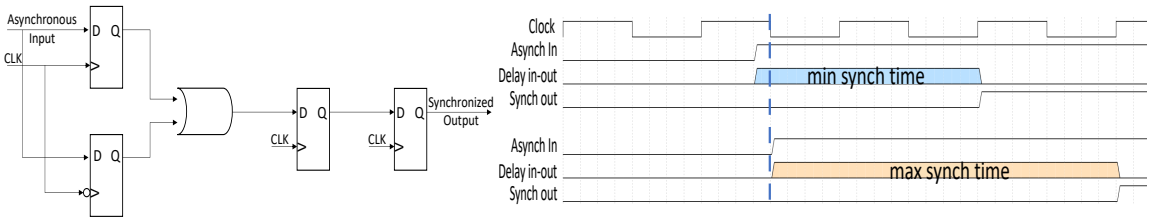

Figure 3: Schematic (left) and time diagram (right) of the synchronisation module embedded in TC.

If the asynchronous input signal occurs immediately before or immediately after the trailing edge of the clock, the synchronisation will take one and half clock period or two and half clock period. The pulse pattern generator provides the asynchronous signal of 250.1 μs period, while the working clock frequency is changed from 40 MHz up to the maximum value settable by the clock generator of 250 MHz. The tests are done measuring with the oscilloscope the delay between the input signal and synchronised signal at two temperatures, 300 K and 77 K. It must be pointed out that full transistor models extracted at 77 K are not available for the used technology, therefore the simulator employs extrapolated parameters. Results of both experimental measurement and simulations are reported in Figure 4. The plot on the left shows the measured (continuous line) and the simulated (dash line) minimum synchronisation delay as a function of the clock frequency. The measurements are affected by a systematic delay of $\sim$ 5.7 ns due to the cables employed in the test set-up. The plot on the right reports the difference between the time delays at the two considered temperatures for both measured and simulated values. The synchronisation circuit simulated with SPICE at cryogenic temperature shows a faster time response of $\sim$ 460 ps compared with room temperature simulation. The ASIC tests revealed a similar trend, with response times measured at cryogenic temperature having an average of $\sim$ 475 ps time difference with respect to room temperature. The analogue simulator approximates reasonably well the experimental behaviour of the circuit, even without parameters defined by the technology vendor for cryogenic temperature. The measurements show that no particular issue with the synchronisation circuit should be expected at 77 K, therefore a similar behaviour can be foreseen also in ALCOR.

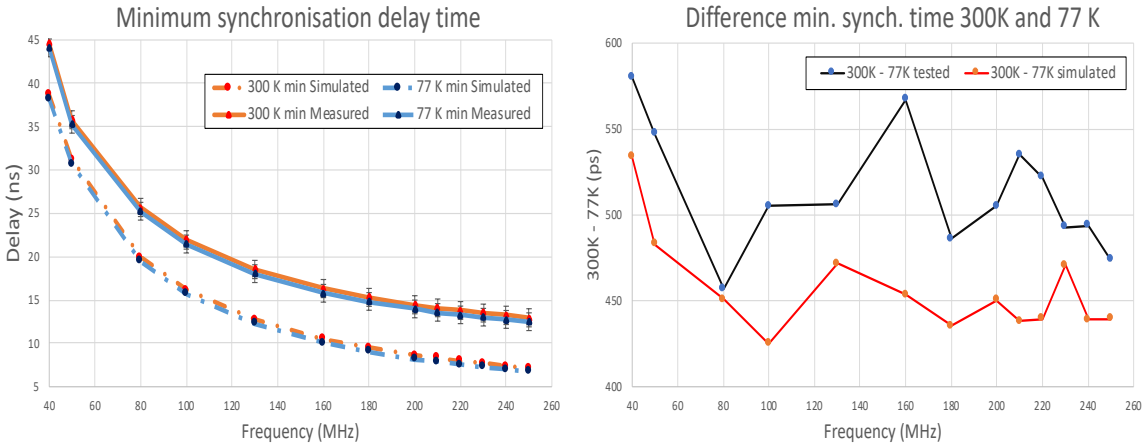

Figure 4: The graph on the left shows the 'minimum delay time' between input signal and synchronised output signal. Graphs show results of simulated and measured values at two different temperatures, 300 *K* and 77 *K*. The blue curves and the orange curves nearly overlap, showing the same trend.

4. Outlook and Conclusions

ALCOR is a 32-channel prototype designed to readout SiPMs sensor at cryogenic temperature. The chip has been sent to fabrication in 2019-Q3. A test chip with several test structures has been implemented in silicon. The experimental results of the LVDS transmitter and the synchronisation circuit are reported in the paper. Both circuits perfom adequately at 77 *K* for the intended application. In particular, the digital circuit works properly at cryogenic temperature and its performance can be well anticipated with SPICE simulations employing extrapolated models.

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