

A 65nm continuous-time sigma-delta modulator with limited OTA DC gain compensation

*Original*

A 65nm continuous-time sigma-delta modulator with limited OTA DC gain compensation / Gonzalez-Diaz, V.R., Pareschi, F.. - In: IEEE ACCESS. - ISSN 2169-3536. - STAMPA. - 8:(2020), pp. 36464-36475. [10.1109/ACCESS.2020.2975601]

*Availability:*

This version is available at: 11583/2804058 since: 2020-03-18T00:01:04Z

*Publisher:*

Institute of Electrical and Electronics Engineers Inc.

*Published*

DOI:10.1109/ACCESS.2020.2975601

*Terms of use:*

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

*Publisher copyright*

IEEE postprint/Author's Accepted Manuscript

©2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collecting works, for resale or lists, or reuse of any copyrighted component of this work in other works.

(Article begins on next page)

Received February 11, 2020, accepted February 14, 2020, date of publication February 21, 2020, date of current version March 2, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2975601

# A 65nm Continuous-Time Sigma-Delta Modulator With Limited OTA DC Gain Compensation

VICTOR R. GONZALEZ-DIAZ<sup>1</sup>, (Member, IEEE),  
AND FABIO PARESCI<sup>2,3</sup>, (Senior Member, IEEE)

<sup>1</sup>Faculty of Electronics, Benemerita Universidad Autonoma de Puebla, Puebla 72000, Mexico

<sup>2</sup>Department of Electronics and Telecommunications, Politecnico di Torino, 10129 Torino, Italy

<sup>3</sup>Advanced Research Center on Electronic Systems (ARCES), University of Bologna, 40125 Bologna, Italy

Corresponding author: Victor R. Gonzalez-Diaz (vicrodolfo.gonzalez@correo.buap.mx)

This work was supported by the Consejo Nacional de Ciencia y Tecnología (CONACyT) Mexico through Infrastructure Project under Grant INFRA2013205873.

**ABSTRACT** This paper explores the effects of compensating the performance degradation in high-speed Continuous-Time Sigma-Delta modulators when the loop integrators are implemented through limited gain Operational Transconductance Amplifiers. Yet, the low DC-gain strongly affects both integrator magnitude and phase responses, with a reduction in the overall effective number of bits. This work models the degradation as due to a signal-dependent memory-less perturbation and theoretically studies its compensation by feeding an opposite signal back to the integrator input. The implementation and experimental results on a 65nm CMOS 2nd order prototype evaluate the performance increase with this technique, where no other compensation, nor any digital calibration, is included. Tested in different conditions, the compensated prototype improves more than 1.5 bit the ENOB with respect to the uncompensated counterpart. For a sampling frequency of 500 MHz the power consumption is 1.7mW, resulting in a 477.2fJ/conv-lev Walden and a 148.8dB Schreier Figures of Merit.

**INDEX TERMS** Limited low-frequency gain OTA, OTA-based integrators, sigma-delta modulators.

## I. INTRODUCTION

Analog-to-Digital converters (ADCs) represent a critical stage in many high-performance portable applications. The accomplishment of a good trade-off between conversion performance and energy-consumption is a critical specification that is typically not easy to achieve. The recent research items up to 2019 [1] show the continuing interest on the Continuous-Time (CT)  $\Sigma\Delta$  based data converters. For a wide bandwidth, these present a good balance between the system resources and are still an option for high-performance data converters design. Another influential feature is the low quantization levels that make these modulators attractive for signal processing. As an example, other recent publications show important benefits for ultra wide-band communications with single-bit CT  $\Sigma\Delta$  encoded streams [2]. The main reason is that a single-bit architecture allows using, in the feedback loop, a simple comparator and a digital buffer as Digital-to-Analog converter (DAC) and ADC, respectively, thus reducing the delay in the loop. In this scenario, regardless

of the improvement in the state-of-the-art, of the increase in order, and of special techniques that may be incorporated to obtain the desired noise shaping, the design of high-performance, large bandwidth (BW) integrators is the critical issue. In particular, when considering Operational Transconductance Amplifier (OTA) based CT integrators, both the BW and the low-frequency open-loop gain (the DC gain) of the OTA must accomplish the in-band noise requirements for a specific resolution [3].

When the OTA design requires a very large BW (i.e., up to a few GHz), the implementation of a multi-stage OTA is problematic. Stability issues require a passive compensation network that, however, limits the BW and increases the resources to fulfill the CT modulator's requirements. A workaround often addressed by designers is given by implementing OTAs composed of a single-stage [4]. This solution easily allows a very large BW. However, achieving a single-stage OTA with DC gain higher than 40 dB is not an easy task [5]. Therefore, a low OTA DC gain is a non-ideality that must be considered at design time. The effect in CT modulators is not only a modification of the integrator's magnitude as a function of the frequency but also a degradation of the phase response.

The associate editor coordinating the review of this manuscript and approving it for publication was Jenny Mahoney.

An integrator whose response deviates from the ideal one is known as *leakage integrator* [6].

Many solutions have been proposed so far in the effort of improving the CT integrators in  $\Sigma\Delta$  modulators. For the sake of illustration, the topology proposed in [3] is based on a *Single Amplifier Biquad* (SAB) integrator with an additional RC passive network in the feedback path. The peculiarity of the design allows relaxation in the requirements of the GBW product for the OTA. However, even if a low GBW can be tolerated, a more detailed analysis shows that the noise shaping in this solution is still sensitive to a low OTA DC gain. Another aspect to be considered is that leakage integrators not only degrade the Signal to Quantization Noise Ratio (SQNR) because of the magnitude influence on the noise transfer function but also change the integrator's frequency response, giving rise to the Excess Loop Delay (ELD). New topologies have been proposed compensating the ELD and the aforementioned inconveniences with more stages in the OTA [7]. Another recent option is the single-amplifier resonator in CT  $\Sigma\Delta$  modulators [8], [9]. The properties in this CT circuit improve the overall modulator's resolution at the expense of more passive elements. The mentioned work highlights the limitations of the OTA DC gain, which must be higher than 40 dB to achieve the desired benefits.

Notwithstanding the mentioned improvements, it is also possible to increase the resolution employing a digital calibration-correction scheme. The drawback is the increase of both the complexity of the DAC in the feedback loop and system power requirement. Anyway, even considering the digital-assisted architectures, the CT integrator is still the bottleneck at increasing the performance of a  $\Sigma\Delta$  modulator.

Previous works show that it is possible to compensate for the OTA limited DC gain by introducing negative feedback in the integrator [10]–[13]. This solution is sometimes indicated as *negative-R assisted integrator*. More recent works [11], [13] suggest advantages in implementing this feedback by using a transconductance amplifier. The main contribution of this work concerns implementation considerations for the transconductance based compensation of the limited DC OTA gain.

Concerning [11], [13], and other similar papers, the novelty of our work can be summarized as follows. *i*) We present a detailed theoretical background, to highlight the limits and the advantages of the proposed technique, but also of refuting some erroneous conclusions appearing in the recent literature. *ii*) The entire design of the  $\Sigma\Delta$  prototype is specifically studied to operate in the condition where the proposed compensation is of paramount importance. The designed OTA is a single-stage high bandwidth, but with a quite low gain. The transconductance compensation stage is designed to work paired with the designed OTA and includes a common-mode compensation that is not present in other works. The single-bit architecture is selected to allow a high sampling frequency; furthermore, as a minor contribution, a simple and high-speed comparator is proposed to implement the one-bit DAC with a limited loop delay. Finally,

no digital compensation is used, so that any observed advantage is due to the compensation technique. *iii*) We propose an evaluation of the effectiveness of the approach through a straightforward comparison between measurements from a non-compensated prototype and measurement from a compensated prototype that does not feature any other compensation technique, nor any digital compensation. To the best of our knowledge, this is the only paper in the literature capable to present such a complete discussion on this technique. As an example, [13] proposes a low-bandwidth low-power  $\Sigma\Delta$  based on high-gain two-stages folded cascode OTAs, where there is actually no need for the low DC gain compensation and lacks in the comparison between performance obtained without compensation.

The manuscript is organized as follows. Section II introduces some analytical aspects of the CT integrators' behavior under the assumption of a limited OTA DC gain. Section III explains the proposed compensation strategy on a CMOS 65 nm process, with emphasis on the critical circuit design constraints. Section IV shows the measurement setup and results of the designed prototype. Results are compared with that achieved by the most recent CT modulators, highlighting the Figures of Merit (FoMs). Finally, Section V draws the conclusion.

## II. LOW DC GAIN COMPENSATION IN CT INTEGRATORS

Due to reliability purposes, high-speed CT voltage integrators for  $\Sigma\Delta$  modulators are designed upon a traditional OTA scheme. In this paper, we focus on the topology based on a single-stage OTA, whose schematic is shown in Fig. 1. For an ideal OTA, we have an infinite transconductance  $g_m \rightarrow \infty$ , an infinite output resistance  $r_o \rightarrow \infty$  and a negligible output capacitance  $C_p \rightarrow 0$ . Under these assumptions, the circuit of the figure implements an ideal inverting voltage integrator: indicating with  $e_i$  the input signal, with  $e_2$  the OTA input signal, and with  $e_3$  the output of the integrator, and considering zero initial conditions, the integrator evolution is  $RCd e_3(t)/dt = -e_i(t)$ , or in the Laplace domain:

$$\frac{e_3(s)}{e_i(s)} = -\frac{1}{sRC} \quad (1)$$

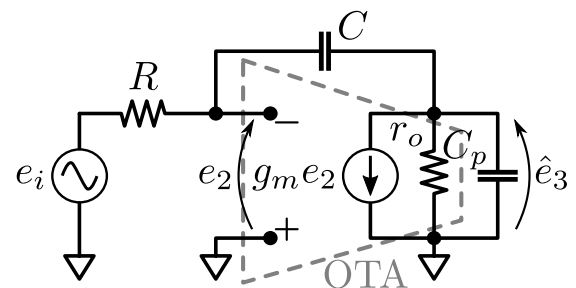


FIGURE 1. Schematic of the OTA-based inverting integrator.

Yet, the deviation of real OTA implementations from this ideal and simple model is the principal source of resolution degradation in CT  $\Sigma\Delta$  data conversion. To keep this

into account, we introduce in the OTA model: *i*) a limited transconductance  $g_m$ ; *ii*) a limited output resistance  $r_o$ ; *iii*) a limited bandwidth, modeled in Fig. 1 with the non-zero intrinsic capacitance  $C_p$ . Note that  $C_p$  and  $r_o$  could be used to include additional non-idealities due to a capacitive or a resistive OTA load, respectively.

**A. RESPONSE OF A NON-IDEAL SINGLE-STAGE OTA BASED INTEGRATOR**

Let us consider the OTA-based integrator for CT  $\Sigma\Delta$  modulators of Fig. 1 with a non-ideal OTA, and let us indicate with  $\hat{e}_3$  the output of the circuit. Even with a non-ideal model, it is still reasonable to assume that:

$$\begin{cases} g_m R \gg 1 \\ g_m r_o \gg 1 \\ C_p < C \end{cases} \quad (2)$$

The frequency response of the non-ideal integrator deviates from the ideal one (1), and by means of (2) can be approximated as:

$$\frac{\hat{e}_3(s)}{e_i(s)} = -g_m r_o \frac{1 - \frac{C}{g_m} s}{1 + g_m r_o RC s + r_o R C C_p s^2} \quad (3)$$

With respect to (1), the magnitude response in (3) is not going to infinity for  $s \rightarrow 0$ , but is upper bounded by  $g_m r_o$ . At a first glance, this is the principal source of performance degradation; indeed, it is possible to show that the low OTA DC gain severely impacts also the phase response.

The transfer function (3) features a (positive) real zero with associated frequency  $\omega_z = g_m/C$  and two (negative) real poles with associated frequencies:

$$\omega_{p1,p2} = \frac{-g_m r_o RC \pm \sqrt{(g_m r_o RC)^2 - 4 r_o R C C_p}}{2 r_o R C C_p}$$

that, given (2), can be approximated in:

$$\begin{aligned} \omega_{p1} &\approx \frac{1}{g_m r_o RC} \\ \omega_{p2} &\approx \frac{g_m}{C_p} \end{aligned}$$

with  $\omega_{p1}$  the dominant low-frequency pole, and  $\omega_{p2}$  the high-frequency one.

It is reasonable to assume that  $\omega_z$  is larger than the system BW. Since  $\omega_{p2} > \omega_z$ , both  $\omega_z$  and  $\omega_{p2}$  have little impact on the in-bandwidth signal. Conversely, the low-frequency pole  $\omega_{p1}$  deviates from zero. This results in a non-negligible magnitude and phase distortion with respect to the desired ideal response for the in-bandwidth signal, that can be evaluated as in the following.

For frequencies lower enough than  $\omega_z$ , the dominant pole approximation is suitable for (3), that can be written as:

$$\frac{\hat{e}_3(s)}{e_i(s)} = -g_m r_o \frac{1}{1 + C g_m R r_o s} \quad (4)$$

By relating (1) with (4), we can evaluate the magnitude deviation as:

$$\left| \frac{e_3(j\omega)}{\hat{e}_3(j\omega)} \right| = \frac{\sqrt{1 + (g_m r_o RC \omega)^2}}{g_m r_o RC \omega}$$

and a phase deviation:

$$\angle e_3(j\omega) - \angle \hat{e}_3(j\omega) = \arctan \frac{1}{g_m r_o RC \omega}$$

which are non-negligible for values of  $\omega$  lower enough than  $1/(RC)$ . As an example, for very low values of  $\omega$ , the phase error grows up to  $\pi/2$ . The circuit turns from an inverting integrator to a low-pass inverting amplifier, canceling the integration effect.

In other words, the effect of a limited DC gain in single-stage OTA based integrators is not only a magnitude error but also a phase one. Of course, the two effects are strongly related; however, we would like to put stress on the second one. By considering the phase error, it is possible to immediately see that the problem is not just a DC-gain smaller than the expected one, but that the underlying principle is radically changed, turning from an integration operation to amplification. This point of view makes clearer how an uncompensated limited DC gain can strongly affect the integration operation.

**B. COMPENSATING THE LIMITED DC GAIN**

It is possible to formulate Eqn. (4) into the time domain as:

$$RC \frac{d \hat{e}_3(t)}{dt} = -\frac{\hat{e}_3(t)}{g_m r_o} - e_i(t) \quad (5)$$

i.e., there is an additional time-dependent term  $-\hat{e}_3(t)/(g_m r_o)$  with respect to the expected ideal integrator response.

Eqn. (5) suggests that a possible way to cope with the limited DC gain is to consider the term  $-\hat{e}_3(t)/(g_m r_o)$  as a signal-dependent memoryless perturbation, that can be canceled by injecting into the circuit an equal term with opposite sign. For low values of  $\omega$ , i.e., in the part of the transfer function that needs to be adjusted, we can neglect the parasitic capacitive elements in nodes  $e_2, e_3$  of Fig. 1 and consider  $\hat{e}_3(t)/(g_m r_o) = e_2(t)$ . So, we can either consider the perturbation term proportional to  $\hat{e}_3$  or  $e_2$ . This observation is important since it allows us to conclude that the node  $e_2$  has all the necessary information to cancel the perturbation.

The circuit we propose to compensate the limited DC gain is the integrator of Fig. 2, where a current signal  $g_c e_2$  is injected into the  $e_2$  node. Using (2), and indicating with  $\bar{e}_3$  the compensated circuit output, the transfer function can be approximated as:

$$\frac{\bar{e}_3(s)}{e_i(s)} = -g_m r_o \frac{\left(1 - \frac{C}{g_m} s\right)}{1 - g_c R + g_m r_o RC s \left(1 - \left(1 + \frac{C_p}{C}\right) \frac{g_c}{g_m}\right) + r_o R C C_p s^2} \quad (6)$$

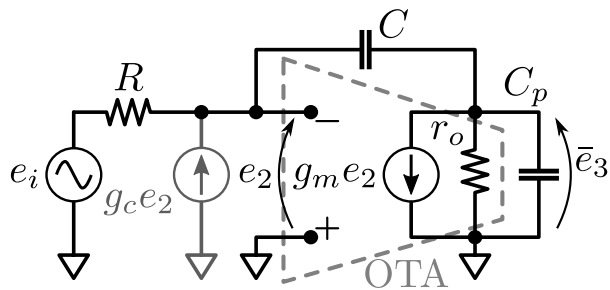


FIGURE 2. Schematic of the proposed compensated OTA-based inverting integrator.

with a high-frequency positive real zero with  $\omega_z = g_m/C$  and two negative real poles with:

$$\omega_{p1} \approx \frac{1 - g_c R}{g_m r_o R C} \left( 1 - \left( 1 + \frac{C_p}{C} \right) \frac{g_c}{g_m} \right)^{-1}$$

$$\omega_{p2} \approx \frac{g_m}{C_p} \left( 1 - \left( 1 + \frac{C_p}{C} \right) \frac{g_c}{g_m} \right)$$

where the perturbation term  $(1 - (1 + C_p/C) g_c/g_m)$  can be reasonably considered not far from the unity value.

By setting  $g_c = 1/R$  the pole  $\omega_{p1}$  goes to zero, and the above perturbation term goes to 1, so that the response of the compensated integrator matches that of the ideal integrator. The error with respect to the ideal response can be obtained by recomputing the transfer function (6) by considering all terms previously neglected. This leads to:

$$\frac{\bar{e}_3(s)}{e_i(s)} = -g_m r_o \cdot \frac{\left( 1 - \frac{C}{g_m s} \right)}{s R C \left( 1 + g_m r_o + r_o C_p s \right)}$$

where the zero and the non-null pole are still larger than system BW, so that the transfer function, for the frequencies of interest, can be approximated with:

$$\frac{\bar{e}_3(s)}{e_i(s)} = -\frac{1}{s R C} \left( 1 + \frac{1}{g_m r_o} \right)^{-1}$$

This results in zero phase error and in a constant, negligible magnitude deviation, given by:

$$\left| \frac{e_3(j\omega)}{\bar{e}_3(j\omega)} \right| = 1 + \frac{1}{g_m r_o}$$

The developed model allows also to evaluate the effect of limited bandwidth for the additional transconductance stage. Let us assume a low-pass transfer function  $g_c(s)$ , with a single-pole in  $s_0$

$$g_c(s) = g_{c0} \frac{1}{1 + \frac{s}{s_0}}$$

and let us use this expression to replace all  $g_c$  terms in (6), easily computing the new integrator transfer function. Its expression is quite cumbersome, and it is not reported here. It features two zeros, the first (negative) at  $s_0$  and the second (positive) at  $g_m/C$ , and three (negatives) poles. Under the

assumption that  $1/(g_m r_o R C) \ll s_0 \ll g_m/C_p$ , the computed poles are:

$$\omega_{p1} \approx \frac{1 - g_c R}{g_m r_o R C} \left( 1 - \left( 1 + \frac{C_p}{C} \right) \frac{g_c}{g_m} \right)^{-1}$$

$$\omega_{p2} \approx s_0 \left( 1 - \left( 1 + \frac{C_p}{C} \right) \frac{g_c}{g_m} \right)$$

$$\omega_{p3} \approx \frac{g_m}{C_p}$$

where, neglecting as above the perturbation term  $(1 - (1 + C_p/C) g_c/g_m)$ , we have a pole-zero cancellation between  $\omega_{p2}$  and the additional zero. So, the response is same as for an ideal  $g_c$  transconductance.

Note that  $1/(g_m r_o R C)$  is the pole of the uncompensated integrator and has typically a low-frequency value. The design of the  $g_c$  stage is, therefore, not critical in terms of bandwidth. In conclusion, the cost in terms of resources of this compensation approach is very low and given by an additional, small, low-bandwidth, low-power transconductance stage.

### C. INFLUENCE OF LEAKAGE INTEGRATORS ON THE $\Sigma\Delta$ MODULATOR NTF

An approach to theoretically calculate the effective resolution of a CT  $\Sigma\Delta$  modulator based on a one-bit quantizer from the Noise Transfer Function (NTF) and Signal Transfer Function (STF) can be found in [14]. The *Effective Resolution* is calculated by relating the normalized power of the input signal to the integrated noise figure within the signal bandwidth. Indicating with  $H_N(s)$  the NTF, and considering the second order modulator architecture in Fig. 3, we get:

$$H_N(s) = \frac{1}{1 - B(s)}$$

where  $B(s)$  is the continuous time filtering of the quantization error in the feedback path, i.e., from  $Y(s)$  to  $Q(s)$  in the figure:

$$B(s) = \frac{Q(s)}{Y(s)} = H_2(s) (-\beta_1 H_1(s) - \beta_2)$$

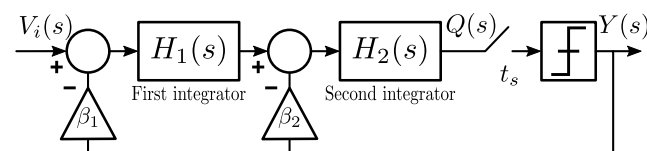


FIGURE 3. Architecture of a generic 2nd order modulator.

Accordingly, the deviated integrator transfer functions set a lower bound on the NTF, and the overall resolution of the converter is impaired. The case studies plotted in Fig. 4 have been obtained replacing  $H_1(s)$  and  $H_2(s)$  with expression (1) for the ideal case, (4) for a limited and uncompensated DC gain, and (6) for a limited but compensated DC gain.

The ideal NTF achieves a second order filter profile. The theoretical Signal to Noise Ratio (SNR), that yields the converter effective resolution, is 75 dB. The limited DC gain

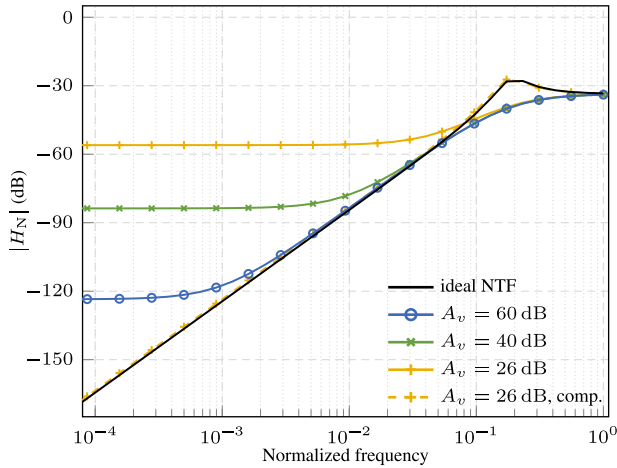


FIGURE 4. Theoretical noise figure of a 2nd order modulator.

increases the in-band noise. For a value of  $g_m r_o$  as low as 26 dB (i.e., a 20 V/V gain), the SNR drops to 42 dB. This result corroborates the large DC gain requirements. Typically,  $A_v \gg \text{OSR}$  is required to shape the noise figure to an acceptable profile [15]. Indeed, in the compensated integrator regulated by (6), the NTF remains very close to the ideal performance.

Note that (6) considers the bandwidth limitation. The compensation stage ideally cancels the constant term of the characteristic polynomial but does not appear on the high order terms. It is possible to conclude that, as long as the non-dominant pole is not within the signal-band, the NTF is barely affected. The work presented in [13] mentions that the negative-resistance compensation relaxes the unity-gain frequency limit for the OTA. However, the detailed analysis and experimental tests help to highlight the limitations of the circuit.

D. PERFORMANCE OF NOISE AND LINEARITY

The transconductance-based DC compensation inherently reduces the overall noise figure of a CT integrator. The schematic in Fig. 5 shows the integrator with possible input noise sources:  $v_n$  model the OTA noise referred to input, while  $i_n$  other sources of noise, including that introduced by the

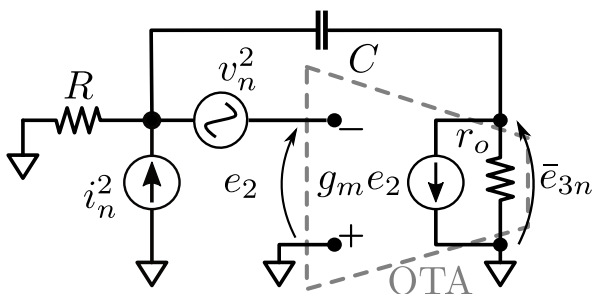


FIGURE 5. Schematic of the OTA-based inverting integrator including main sources of noise.

transconductance compensator. The output referred noise is:

$$e_{3n}(s) = -\frac{g_m r_o \left(1 - \frac{C}{g_m s}\right) ((Rg_c - 1)v_n(s) + R i_n(s))}{s(RC + C r_o - RCg_c r_o + RCg_m r_o) - Rg_c + 1}$$

With  $g_c = 1/R$ , the expression reduces to:

$$e_{3n}(s) = -R \frac{g_m r_o \left(1 - \frac{C}{g_m s}\right)}{sRC(1 + g_m r_o)} i_n(s) \tag{7}$$

Therefore, in the ideal scenario, the input referred noise  $v_n$  of the OTA is canceled by the compensation scheme. In addition, the noise figure in (7) locates the pole to zero frequency, and shapes the compensation stage noise  $i_n$  to a high-pass function. In a more realistic scenario, perfect compensation cannot be reached. Indeed, under the assumption that  $Rg_c \approx 1$ , and that  $v_n$  and  $R i_n$  are comparable in terms of power, the main contribution to the output noise is given by  $i_n$  due to the presence of the scaling factor  $Rg_c - 1$  term in the transfer function of the  $v_n$ . So, we focus on the  $i_n$  contribution.

Fig. 6 shows, assuming  $v_n$  negligible, the value of  $H_n(s) = e_{3n}(s)/i_n(s)$  for realistic values of the integrator parameters and for different compensation outcome. In other words, the figure gives an idea of how the input noise is transferred to the output according to the achieved compensation. A perfect compensation correctly locates a pole to the zero frequency and drastically reduce the low-frequency noise. Yet, for  $g_c = 1/(0.9R)$  the low-frequency output noise is still reduced by 12 dB with respect to the uncompensated case.

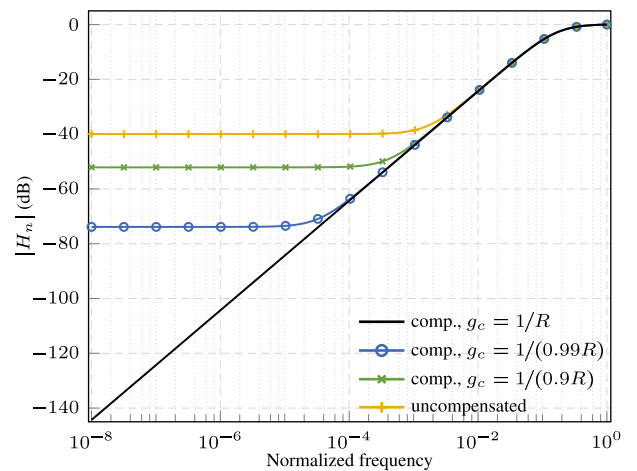


FIGURE 6. Noise transfer function for the non-perfect compensated integrator.

This model is valid as long as the OTA remains in the linear range of operation. The compensation circuit monitors the analog ground nodes, having small signal amplitude. Therefore, the compensation circuit design must behave linearly for this small signal amplitudes.

For the sake of clearness is important to notice that it is possible to use the compensation scheme also for multi-stage amplifiers because the compensating stage does not influence high order terms. However, the limits in bandwidth and power

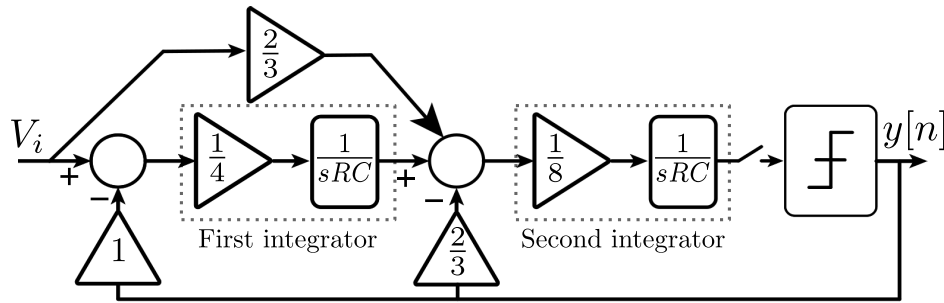


FIGURE 7. Block diagram for the implemented 2nd order CT  $\Sigma\Delta$  modulator.

consumption make the compensation ineffective. This application is particularly suited for high-speed modulators.

### III. CIRCUIT IMPLEMENTATION

#### A. TOPOLOGY SELECTION AND LIMITATIONS

The scope of our work is to analyze the benefit of the transconductance based compensation scheme on the Sigma-Data modulator. For a better analysis, the topology and design must reduce other non-ideal circumstances.

The target design is a medium to high-speed converter based on integrators with a very large BW so that a design based on single-stage OTA is preferable. The achievement of a high-gain is not an easy task, but the consequence of a low gain is the impairment of the integrator transfer function. The need for a high-speed converter requires considering an architecture having a good trade-off between tolerance to ELD, linearity and Noise Shaping.

According to the existent theoretical considerations in [6], the second-order single-loop CT modulator raises the in-band noise floor to  $-80$  dB, with an ELD less than twenty percent of the sampling period. Therefore, this topology can tolerate large ELD values. In higher-order topologies the tolerance is reduced to only a few percentage units, with the need for ELD compensation, rising other complications.

Therefore, for the experiment design in this work, the second-order scheme ensures stability, ELD tolerance, and a 2-levels quantization ensures linearity and simplicity of a Non-Return to Zero (NRZ) DAC to reduce circuit resources.

The DACs are simple inverters from the digital output to the CT integrators, without the need for including additional voltage references. The only drawback is the power supply noise, that can be reduced with proper decoupling and routing techniques. Moreover, Section II-D discusses the advantages of the compensation scheme in noise. Furthermore, a feed-forward typology requires an additional summing point that limits bandwidth and resolution [6]. This is the motivation for selecting a distributed feedback topology, including the consolidated high-speed CT  $\Sigma\Delta$  design techniques.

In conclusion, this scenario is actually the ideal case study to highlight the effects of the limited DC gain in the OTA implementing the CT integrators.

Given the aforementioned considerations, the proposed compensation scheme has been applied to the two integrators used in a high-speed second-order single-bit  $\Sigma\Delta$  modulator whose block diagram is depicted in Fig. 7. A feedforward path is used to reduce the output swing in the second integrator. The coefficients are selected to improve the effective resolution under the assumption that the  $\Sigma\Delta$  sampling frequency is  $F_s = 1/(RC)$  and that the input signal can span the whole range  $[0, V_{dd}]$ , that is also the conversion range of the 1-bit DAC. The circuit has been designed in the UMC 65 nm mixed-signal process. Table 1 summarizes the main  $\Sigma\Delta$  modulator parameters.

TABLE 1. Parameters for the designed  $\Delta\Sigma$  modulator.

Sampling frequency, $F_s = 500$ MHz	$V_{dd} = 1.2$ V
Oversampling Ratio = 48	$R = 1$ k $\Omega$
BW = 5.2 MHz	$C = 2$ pF

The implementation of the modulator at circuit-level follows a fully-differential approach and is shown in Fig. 8. Integrators are based on a simple RC scheme using single stage OTAs and have been compensated using two transconductance stages according to the approach illustrated in Fig. 2. With respect to the theoretical approach of Sec. II, two minor changes are considered: *i*) being fully differential, the compensating stages are driven by a doubled voltage with respect to the single-ended approach. As a result, their transconductance value is set to  $g_c/2$ ; *ii*) both integrators present multiple inputs. In this case, the  $g_c$  must be calculated according to the equivalent resistance at the integrator's input.

#### B. SINGLE STAGE OTA

The CT integrators of the designed prototype are based on a single stage fully differential OTA. Fig. 9 shows the schematic at transistor level, the dimensions and the specs of the OTA. The OTA uses a discrete time common mode feedback circuit [16] to set the output common mode output to the  $V_{cm} = V_{dd}/2$  value. The common mode control is on the  $V_{CMFB}$  node in the scheme. The DC gain is only 21 dB; however, the gain-bandwidth (GBW) product is very large

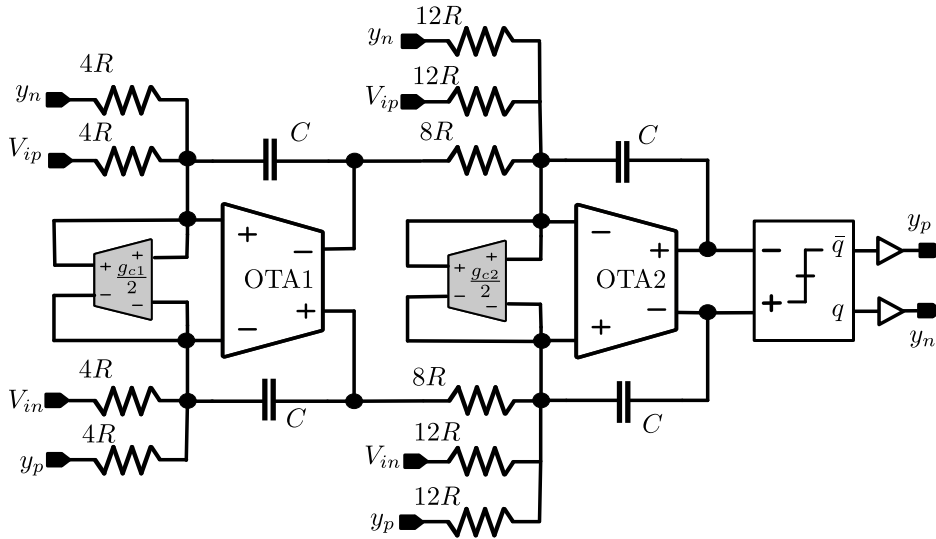


FIGURE 8. Topology of the implemented 2nd order CT  $\Sigma\Delta$  modulator with feedforward and limited DC gain compensation.

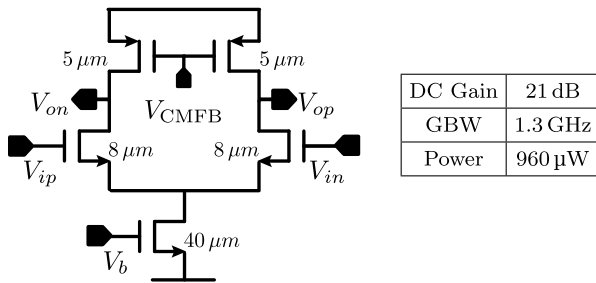


FIGURE 9. Schematic of the single stage OTA circuit, along with specs.  $L = 120$  nm for all transistors.

and equal to 1.3 GHz, allowing for sampling frequencies up to  $F_s = 500$  MHz.

### C. COMPENSATING TRANSCONDUCTANCE STAGE

The schematic of the compensating transconductance stages is based on the fully differential pair shown in Fig. 10. The circuit includes a CT CMFB block that sets the common

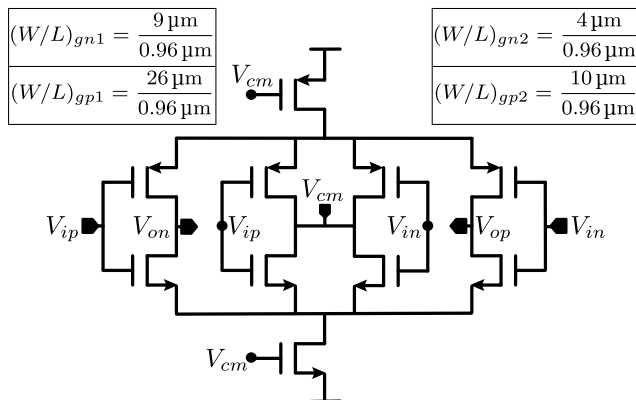


FIGURE 10. Schematic of the compensating transconductance stage and the device dimension.

mode voltage to  $V_{cm}$ . All the NMOS transistors and all the PMOS transistors have the same size, indicated with  $(W/L)_{gn}$  and  $(W/L)_{gp}$ , respectively, that is set according to the desired values of  $g_{c1}$  and  $g_{c2}$ . Note that, due to the non-tight requirements in terms of bandwidth (as addressed in Sect. II), we preferred to design this stage using long-channel transistors (i.e.,  $16 L_{min} = 0.96 \mu\text{m}$ ) to limit the mismatch between transistors and so the variations of the compensating transconductance.

According to the modulator's schematic in Fig. 8, the two integrators are driven by an equivalent resistance equal to  $2R$  and  $24R/7$ , respectively. Given the value of  $R$  in Tab. 1, the desired gain for the transconductance stages is  $g_{c1} = 500 \mu\text{S}$  and  $g_{c2} \approx 290 \mu\text{S}$ , i.e.,  $g_{c1}/2 = 250 \mu\text{S}$  and  $g_{c2}/2 \approx 145 \mu\text{S}$ .

### D. COMPARATOR

Since this work aims to propose a measurement of real advantages of the compensation of the low DC-gain in the OTA integrator, it is necessary to keep all other sources of error at a negligible level. In particular, it is of paramount importance that the degradation of converter performance due to the comparator delay is limited (and negligible) compared with the performance degradation due to the low DC gain. Therefore, in the pursuit of reducing the loop delay, the speed of the comparator is critical.

As a minor contribution of this paper, the designed circuit embeds a novel high-speed comparator based on the regenerative latched comparator in [17]. We introduce two modifications: *i*) the position of transistors in the fully complementary regenerative network is rearranged in order to reduce the number of series transistor, with beneficial effects in low voltage and high-speed applications; and *ii*) the Set-Reset latch is very simple with a cross-coupled inverters pair and the evaluating devices are two NMOS transistors. The schematics of

the fully differential comparator and of the SR latch (FDSR) are shown in Fig. 11.

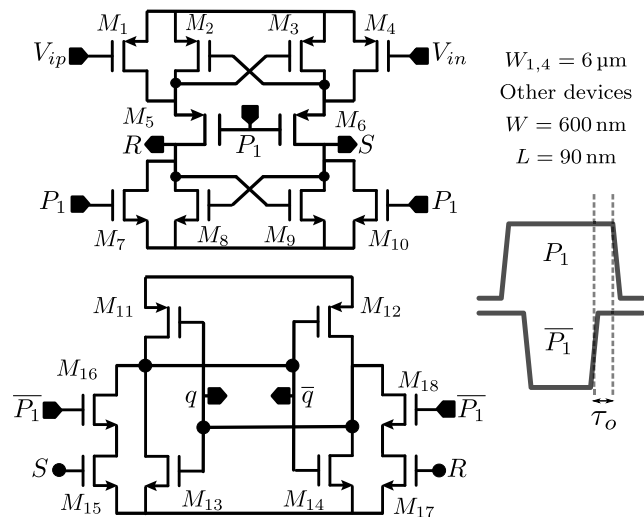


FIGURE 11. Schematic of the fully differential comparator and of the SR latch (FDSR).

In the input stage,  $M_{1,4}$  pre-amplify the differential input signal. Transistors  $M_{2,3}$  and  $M_{8,9}$  form a metastable regenerative network with positive feedback that speeds up the comparison and holds the result.  $M_{5,6}$  and  $M_7 - M_{10}$  reset the circuit according to the synchronization signal  $P_1$ . Timing scheme for  $P_1$  and its non-overlapping complementary  $\bar{P}_1$  is highlighted in the figure. When  $P_1 = V_{DD}$ ,  $M_7 - M_{10}$  turn on and the  $S, R$  nodes reset to  $V_{SS}$ , and  $M_{5,6}$  turn off. In this configuration, the differential input is in wait mode, while the latch stage holds the previous state. As soon as  $P_1 = V_{SS}$ ,  $M_7 - M_{10}$  turn off, and after a safe time,  $M_{5,6}$  turn on thus enabling the metastable circuit.

The latch is formed by transistors  $M_{11} - M_{18}$ . In the hold state ( $\bar{P}_1 = V_{DD}$ ), the preamplifier computes with outputs disconnected from the latch.  $M_{11} - M_{14}$  operate as a standard holding circuit. In the set state ( $P_1 = V_{DD}$ ), the preamplifier outputs are stable and passed to the latch storing the result. When the latch is disabled, even if the preamplifier enters into a not-valid state, the latch holds the previous comparison and a new cycle starts.

E. ROBUSTNESS OF THE COMPENSATION

The circuit for the compensation scheme uses the common mode bias point to set the transconductance. The compensation scheme in [13] is similar, since the cross-coupled inverters can also set the transconductance, but the bias point is not statically set. As a consequence, the scheme may not be effective when considering Process-Voltage-Temperature (PVT) changes.

Indeed, the scheme presented here is robust to PVT variations. In this section, we limit ourselves to provide simulation results when considering process variations. Fig. 12 shows the transfer function of the first integrator of the loop of Fig. 8 (considering both magnitude and phase response) in

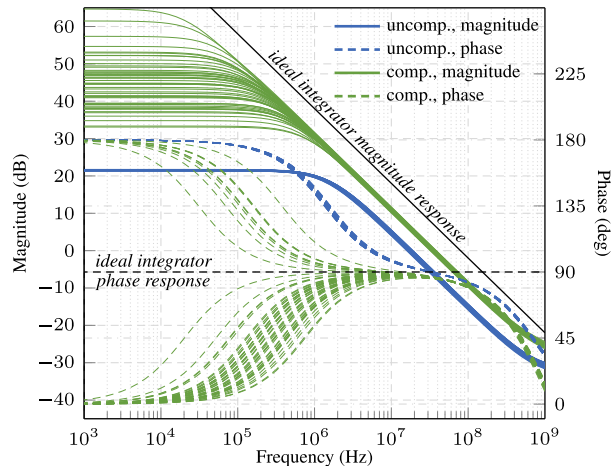


FIGURE 12. Montecarlo simulation considering process variations in the compensated and uncompensated integrator.

50 runs of a Montecarlo simulation using the device models provided by the foundry that include process variations. Both the compensated and uncompensated integrators have been considered. In all runs the compensation scheme is capable to improve the overall integrator’s performance both in magnitude and phase. Even if the uncompensated circuit features smaller variations, the fully differential topology of the compensated scheme ensure stability for all cases, and the compensated phase response is close to the 90 deg value of the ideal inverting integrator for a quite large range of frequency.

Note that the introduction of variability in the circuit parameters results in a non-perfect compensation between  $g_c$  and  $R$ . More precisely, we may obtain an integrator that is undercompensated (i.e.,  $g_c R < 1$ ) or overcompensated (i.e.,  $g_c R > 1$ ). In the first case, we obtain for low frequencies, an inverting transfer function, with phase equal to 180 deg, while in the second case a non-inverting transfer function, with phase equal to 0 deg. This is the expected behavior: according to (6), if  $g_c R \neq 1$ , the integrator is turned again into a low-pass amplifier as in the non-compensated case. This amplifier is inverting or non-inverting if  $1 - g_c R$  is positive or negative, respectively. This is visible in the figure where the worst-case reduces the cut-off frequency by at least one order of magnitude, comparing to the uncompensated case.

IV. EXPERIMENTAL RESULTS

A. EXPERIMENTAL TEST SETUP

The microphotograph of the integrated circuit prototype is depicted in Fig. 13. The circuit has been designed and manufactured in UMC 65 nm CMOS design process using the multi-project wafer service offered by Europractice®. The design tool used for the design was Cadence® Virtuoso. The prototype physically embeds multiple instances of the designed  $\Sigma\Delta$  modulator, in which the value of  $C$  was scaled to allow to work at three sampling frequencies  $F_s = \{125 \text{ MHz}, 250 \text{ MHz}, 500 \text{ MHz}\}$ . For comparison purposes, the prototype embeds both the Sigma-Delta modulator with and without the compensation stages.

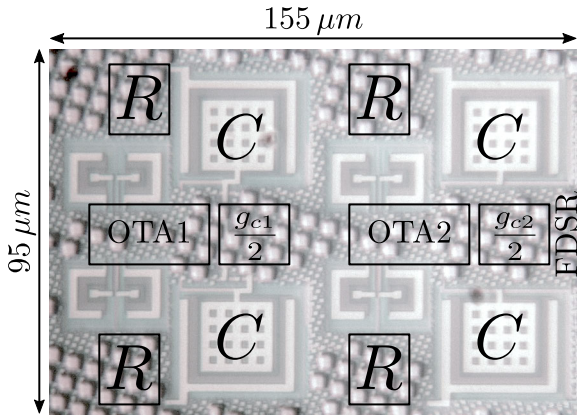


FIGURE 13. Integrated circuit microphotograph and stage locations.

The experimental setup is shown in Fig. 14. The prototype is powered by a 3.3 V button cell battery, used to generate the  $V_{dd} = 1.2$  V power supply voltage, the  $V_{cm} = V_{dd}/2$  and all OTA current references (“Bias mini-board” in the figure). This solution is adopted to reduce noise coupling and to allow at the same time to change the OTA biasing. The input signal is transformed to fully differential with a JT-1975 balun, with a 80 MHz bandwidth and a 3 dB insertion loss in this frequency range. The Keysight 81160A arbitrary signal generator provides the clock signal, while the input signal is from a Siglent SDG1025 waveform generator. A Keysight 16851A logic signal analyzer is used to acquire the oversampled bit-stream. When possible, the logic signal analyzer and the device under test share the same clock signal to capture data in the synchronous configuration. Due to hardware limitations, this was possible up to 300 MHz; beyond this limit, the logic analyzer allows only the asynchronous setup.

**B. MEASUREMENT RESULTS**

The designed prototype has been characterized by measuring the Signal to Quantization Noise Ratio (SQNR) according to the frequency spectrum computed through the Discrete

Fourier Transform of the acquired signal using, for a better distinguishing of the harmonic content,  $N = 81920$  points. A total of 8 spectra have been considered and averaged to avoid (either best- and worst-case) corner cases.

Fig. 15 shows the CT modulator dynamic range for the compensated and uncompensated cases. The difference between the two curves approximately ranges between 6 dB and 10 dB for any input power level, resulting in a gain that can be evaluated between 1 bit and 1.5 bit. Moreover, the dynamic range for the compensated prototype shows an extended behavior close to the full scale (0 dB) amplitude ranges, with a higher gain concerning the uncompensated case.

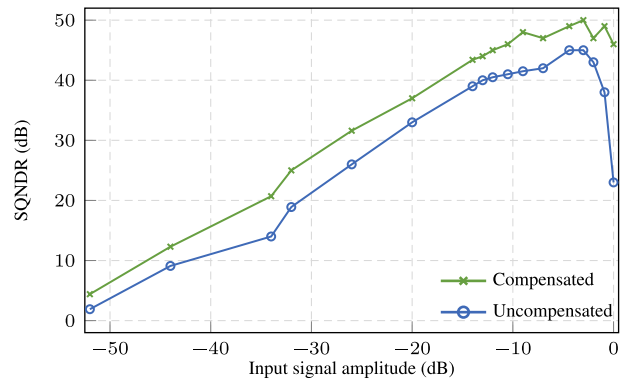


FIGURE 15. Dynamic range for the in-band tests, with  $F_s = 250$  MHz.

Fig. 16 shows the spectrum of the uncompensated and compensated cases for the  $F_s = 125$  MHz sampling frequency. The input signal is within the signal bandwidth  $F_{in} = 193.8$  kHz and  $-3$  dB from the Full Scale (FS) reference. The ratio between  $F_{in}$  and the system BW is set to 0.148, thus ensuring that any possible harmonic content rises in the signal bandwidth. The comparison between the two curves clearly shows an increased harmonic content and quantization noise floor level for the uncompensated circuit. The effective number of bits is improved by almost 2 bit.

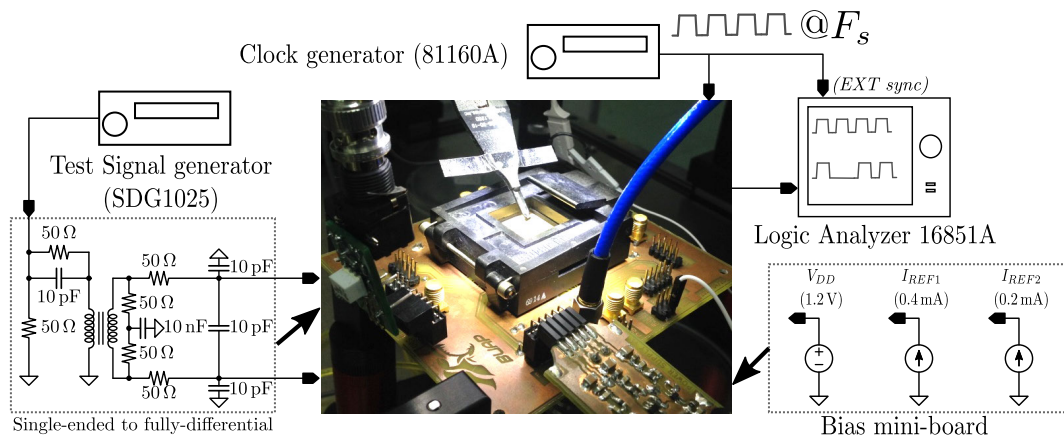


FIGURE 14. Physical test setup.

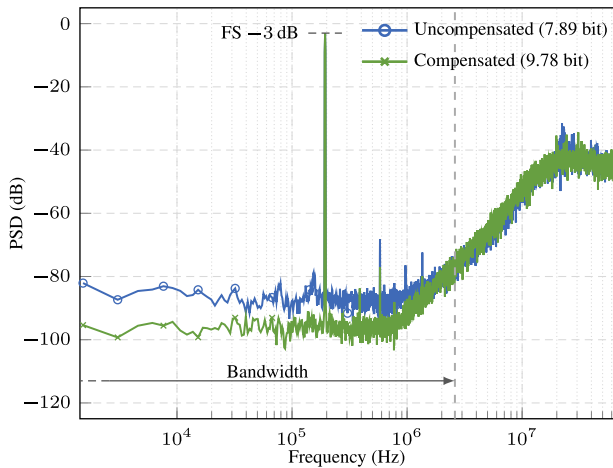


FIGURE 16. Power spectral density for a  $-3$  dB FS 193.8 KHz sinusoidal tone input signal, with  $F_s = 125$  MHz.

Note that the resolution achieved by the compensated circuit is very similar to that achieved by high-level simulation of an ideal system and given by 10.53 bit. This is an important result, considering that the gain of the single-stage OTA used in the integrator blocks is only 21 dB.

A similar trend can be observed in Fig. 17, which shows the result for an input signal with  $F_{in} = 103.8$  kHz and  $-3$  dB from the Full Scale (FS), using a  $F_s = 500$  MHz sampling frequency. Note that, to the curves of Fig. 16, both harmonic distortion and noise floor are slightly increased. We believe that this is due to the hardware limitation of our measurement setup, which does not allow the synchronization between the signal analyzer and the prototype clock, resulting in an additional uncertainty source. Anyway, the improvement of the compensated case is more than 1.5 bit also in this case.

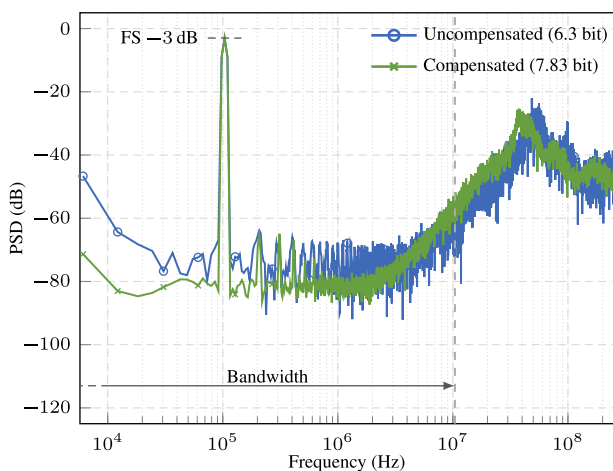


FIGURE 17. Power spectral density for a  $-3$  dB FS 103.8 KHz sinusoidal tone input signal, with  $F_s = 500$  MHz.

Figure 18 shows the distribution of the 1.71 mW measured from the prototype. The most power hungry blocks are the OTAs, which are designed for a 1.3 GHz BW. In particular,

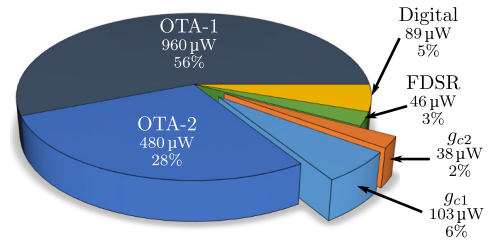


FIGURE 18. Distribution of the 1.71 mW measured from the prototype working at  $F_s = 500$  MHz.

the first in the loop is responsible for more than half of the power due to the lower gain. As highlighted in the figure, the two compensating transconductance stages allocate only about 8% of the overall power consumption. As an additional important contribution of this work, the comparator consumes a very low amount of energy corresponding to the 3% of the overall power consumption.

C. LINEARITY TEST

Fig. 19 shows the PSD measured with a two-tone input signal. Programming the Siglent SDG1025 signal generator with the EasyWave application makes possible the scenario where two tones with the same amplitude are closely spaced in frequency (they are located at  $f_1 = 83$  kHz and  $f_2 = 103.8$  MHz, with  $f_2 = 1.25 f_0$ ). The aim is moving intermodulation tones to the lower part of the spectrum. The prototype with the compensation scheme achieves very good linearity, as there are no intermodulation effects around the frequency  $f_2 - f_1$  in this test.

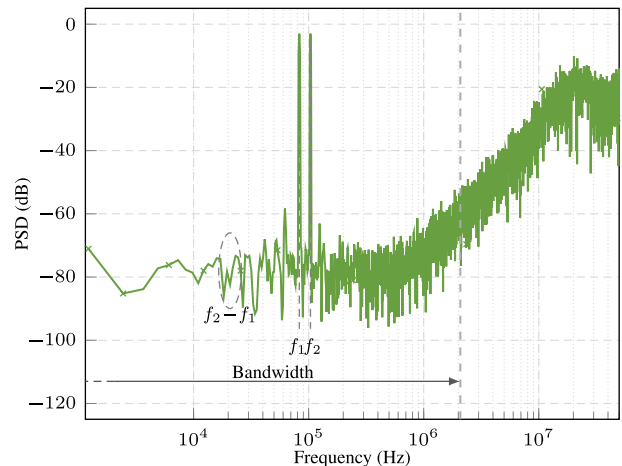


FIGURE 19. Power spectral density for a two-tone input signal (83 KHz and 103.8 KHz) with  $F_s = 100$  MHz.

D. DIFFERENCES WITH RECENT COMPENSATION SCHEMES

The work in [10] introduces the possibility to compensate the OTA limited DC gain with negative feedback implemented employing a low-gain inverting amplifier and a resistance. However, the basic idea is not practical because the proposed schematic includes an amplifier whose output is a

**TABLE 2.** Comparison between the designed circuit and some recent CT  $\Sigma\Delta$  modulators.

	This work	[12] (2014)	[7] (2015)	[18] (2016)	[3] (2018)	[9] (2018)	[19] (2018)	[20] (2018)	[21] (2018)	[22] (2018)	[13] (2019)
CMOS process (nm)	65	65	55	90	65	130	65	40	65	28	65
Modulator's order	2	3	3	3	3	3	2	3	3	4	3
Quantizer levels	2	8	16	16	16	2	256	4	3	16	2
Calibration scheme levels	No	FIR-DAC	DWA	DEM	Trim	No	Neural	SAR-ELDC	ELD	ELD-ISI	No
Area (mm <sup>2</sup> )	0.015	0.039	0.089	0.17	0.033	0.232	0.024	0.029	0.14	0.024	0.27
VDD (V)	1.2	1.1	1.2/1.8	1.2	1.2/1.8	0.54	0.8	-	1.2	1.16/1.5	1.2
$F_s$ (MHz)	500	650	140	480	640	10	0.032	500	6.144	2000	8
OSR	48	32	32	24	32	50	32	20	128	20	200
BW (MHz)	5.2	10	2.2	10	10	0.1	0.001	25	0.024	50	0.02
Power (mW)	1.71	1.82	4.5	14.4	5.35	0.055	0.0008	1.16	0.068	64.3	0.055
Peak SNR (dB)	52.5	69.3	90.8	63.7	79.6	69.84	66.2	70.4	94.1	79.8	88.5
FoMWa (fJ/conv-lev)	477.2	41.4	37.8	575	36.5	415.96	480.9	17.1	34.2	80.5	63.2
FoMSch (DR) (dB)	144.8	166.8	178.9	-	177	157	154.1	70.7	179.5	168.7	178.7

voltage signal. The design is more difficult compared to a transconductance amplifier, in particular for large bandwidth. The compensation scheme requires both a precise amplifying factor and a matched resistance value, thus increasing the error sources.

The work in [11] introduced the possibility to use a transconductor stage in the compensation scheme, thus achieving clear benefits. However, the results are presented only at a simulation-level, and most importantly, the compensation scheme is applied on a  $\Sigma\Delta$  with a multi-bit quantizer. A problem of the compensation scheme for multi-bit quantizers is that the compensation transconductance value depends on the different values of the DAC resistances. Also, process variations have a negative impact, as it is evident from the simulated results. To make the compensation scheme more reliable it is necessary to add a transconductance stage for every feedback resistor of the DAC. Moreover, if the number of ADC levels is beyond 8, a calibration scheme is required limiting the overall ELD and the physical implementation is not straightforward for high-speed modulators. Therefore, the increased complexity and calibration of a multi-bit ADC reduces the effectiveness of the idea.

The recent works in [13] and [12] present a similar compensation strategy for the OTA's low DC gain. The work in [13] uses the compensation in a two-stage folded-cascoded OTA embedded in a low-power and low-frequency application. For the required bandwidth is possible to select an ad-hoc OPAMPs architecture. Besides, the over-sampling ratio makes the limited OTA DC gain to be a non-dominant source of error. The circuit in this work provides a comparison between the experimental results of a prototype with and without the compensation strategy. The work in [12] uses a multi-bit and inverted based integrator CT filter. The topology includes several circuit techniques to improve the overall SNR performance and is not possible to distinguish the impact of negative-resistance compensation.

### E. COMPARISON WITH RECENT CT TOPOLOGIES

Table 2 shows the important parameters to calculate the most accepted FoMs [1], [23] of the recent CT  $\Sigma\Delta$  modulators. For the sake of distinction, the table includes the relation of the architecture with the quantizer levels and the utilization of calibration schemes. The comparison with the similar works is presented in chronological order. The topologies in [3], [7], [12] present good FoM numbers at the expense of a third-order topology and more quantization levels. These solutions use a calibration scheme and the enhanced performance is the combination of the special techniques. The solutions in [13], [20]–[22] give also important numbers, with the integration of several SQNR enhancement techniques.

To highlight the contribution of this work we emphasize the work in [13] which takes a similar DC-gain compensation scheme. A big difference is that the compensating circuit of the reference is impaired with the common-mode voltage of the main OTA, and the modulator aims low-frequency rates, with a multi-stage based amplifier.

In contrast, the  $\Sigma\Delta$  modulator designed in this work aims to medium to high speed bandwidth, where the compensation scheme is more relevant. It achieves a Walden FoM of 477.2 fJ/conv-lev and a Schreier FoM of 144.8 dB. The result confirms the effectiveness of the simple DC-Gain compensation scheme in the application where is necessary.

### V. CONCLUSION

A theoretical analysis shows that the OTA's low DC-gain degrades to CT voltage integrators. The low DC-gain impairs both the integrator's magnitude and phase responses. Furthermore, it nullifies the integrator operation for the low-frequency components of the input signal. Therefore, OTA's low DC-gain is the bottleneck in the important CT  $\Sigma\Delta$  implementations. In this work, through an integrated circuit prototype of a CT  $\Sigma\Delta$  modulators designed in a CMOS 65 nm process, we show that is possible to compensate the negative impact of a low DC gain in single

stages OTA. A feedback transconductance stage cancels the frequency-dependent perturbation. With the proposed solution it is possible to achieve a good power to conversion-level balance without cumbersome compensation circuits or additional calibration techniques.

## REFERENCES

- [1] B. Murmann, *ADC Performance Survey 1997–2018*. [Online]. Available: <http://web.stanford.edu/~murmman/adcsurvey.html>
- [2] X. Tang, Q. Hu, and W. Tang, "Delta-Sigma encoder for low-power wireless bio-sensors using ultrawideband impulse radio," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 7, pp. 747–751, Jul. 2017.
- [3] W. Wang, Y. Zhu, C.-H. Chan, and R. P. Martins, "A 5.35-mW 10-MHz single-opamp third-order CT  $\Delta\Sigma$  modulator with CTC amplifier and adaptive latch DAC driver in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2783–2794, Oct. 2018.
- [4] S. Pavan, R. Schreier, and G. C. Temes, *Circuit Design for Continuous-Time Delta-Sigma Modulators*. Hoboken, NJ, USA: Wiley, 2017, ch. 10, pp. 301–361.
- [5] R. Pova, N. Lourenco, R. Martins, A. Canelas, N. Horta, and J. Goes, "Single-stage OTA biased by voltage-combiners with enhanced performance using current starving," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 11, pp. 1599–1603, Nov. 2018.
- [6] M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion Fundamentals, Performance Limits and Robust Implementations* (Series in Advanced Microelectronics). Amsterdam, The Netherlands: Springer, 2006.
- [7] C.-Y. Ho, C. Liu, C.-L. Lo, H.-C. Tsai, T.-C. Wang, and Y.-H. Lin, "A 4.5 mW CT self-coupled  $\Delta\Sigma$  modulator with 2.2 MHz BW and 90.4 dB SNDR using residual ELD compensation," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2870–2879, Dec. 2015.
- [8] K. Matsukawa, Y. Mitani, M. Takayama, K. Obata, S. Dosho, and A. Matsuzawa, "A fifth-order continuous-time delta-sigma modulator with single-opamp resonator," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 697–706, Apr. 2010.
- [9] P. C. C. de Aguirre and A. A. Susin, "A 0.6-V, 74.2-dB DR continuous-time sigma-delta modulator with inverter-based amplifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 10, pp. 1310–1314, Oct. 2018.
- [10] V. R. Gonzalez-Diaz, F. Maloberti, and A. Peña-Perez, "Opamp gain compensation technique for continuous-time  $\Delta\Sigma$  modulators," *Electron. Lett.*, vol. 50, no. 5, pp. 355–356, Feb. 2014.
- [11] V. R. Gonzalez-Diaz, A. Pena-Perez, and F. Maloberti, "Continuous time  $\Delta\Sigma$  modulator with efficient gain compensated integrators," *Microelectron. J.*, vol. 56, pp. 38–45, Oct. 2016.
- [12] S. Zeller, C. Muenker, R. Weigel, and U. Ussmueller, "A 0.039 mm<sup>2</sup> inverter-based 1.82 mW 68.6 dB-SNDR 10 MHz-BW CT- $\Sigma\Delta$  -ADC in 65 nm CMOS using Power- and area-efficient design techniques," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1548–1560, Jul. 2014.
- [13] M. Jang, C. Lee, and Y. Chae, "Analysis and design of low-power continuous-time delta-sigma modulator using Negative-R assisted integrator," *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 277–287, Jan. 2019.
- [14] R. Schreier, "An empirical study of high-order single-bit delta-sigma modulators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 40, no. 8, pp. 461–466, Aug. 1993.
- [15] F. Maloberti, *Data Converters* (Electronics and Electrical Engineering). Amsterdam, The Netherlands: Springer, 2007.
- [16] F. Maloberti, *Analog Design for CMOS VLSI Systems*. Boston, MA, USA: Springer, 2001.
- [17] F. Gerfers, M. Ortmanns, and Y. Manoli, "A 1.5-v 12-bit power-efficient continuous-time third-order  $\Sigma\Delta$  modulator," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1343–1352, Aug. 2003.
- [18] R. Ritter, J. G. Kauffman, J. Becker, and M. Ortmanns, "A 10 MHz bandwidth, 70 dB SNDR continuous time delta-sigma modulator with digitally improved reconfigurable blocker rejection," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 660–670, Mar. 2016.
- [19] C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "A 92 dB dynamic range sub- $\mu V_{rms}$ -noise 0.8 $\mu W$ /ch neural-recording ADC array with predictive digital autoranging," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 470–472.
- [20] J. Liu, S. Li, W. Guo, G. Wen, and N. Sun, "A 0.029 MM2 17-FJ/Conv-Step CT  $\Delta\Sigma$  ADC with 2<sup>nd</sup>-order noise-shaping SAR quantizer," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2018, pp. 201–202.
- [21] C. Lee, M. H. Jang, and Y. Chae, "A 1.2V 68 $\mu W$  98.2 DB-DR audio continuous-time delta-sigma modulator," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2018, pp. 199–200.
- [22] T. He, M. Ashburn, S. Ho, Y. Zhang, and G. Temes, "A 50 MHz-BW continuous-time  $\Delta\Sigma$  ADC with dynamic error correction achieving 79.8dB SNDR and 95.2 dB SFDR," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 230–232.
- [23] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Sel. Areas Commun.*, vol. 17, no. 4, pp. 539–550, Apr. 1999.



**VICTOR R. GONZALEZ-DIAZ** (Member, IEEE) was born in Puebla, Mexico. He received the M.Sc. and Ph.D. degrees from the National Institute for Astrophysics, Optics, and Electronics (INAOE), Puebla, in 2005 and 2009, respectively. He collaborated as a Postdoctoral Fellow with the Microsystems Laboratory, The University of Pavia, Italy, from 2009 to 2010. Since 2011, he has been a full-time Professor and the Head of the Circuits and Systems Characterization Laboratory, Faculty of Electronics-BUAP, Puebla. His main research interests are frequency synthesizers, data converters, and sigma-delta modulation for analog and digital applications.



**FABIO PARESCHI** (Senior Member, IEEE) received the Dr. Eng. degree (Hons.) in electronic engineering from the University of Ferrara, Italy, in 2001, and the Ph.D. degree in information technology from the University of Bologna, Italy, in 2007, under the European Doctorate Project (EDITH).

He is currently an Assistant Professor with the Department of Electronic and Telecommunication, Politecnico di Torino. He is also a Faculty Member with ARCES, University of Bologna. His research activities focus on analog and mixed-mode electronic circuit design, statistical signal processing, compressed sensing, random number generation and testing, and electromagnetic compatibility.

Dr. Pareschi received the Best Paper Award at ECCTD 2005, and the Best Student Paper Award at EMC Zurich 2005 and the IEEE EMCCompo 2019. He was a recipient of the 2019 IEEE BioCAS Transactions Best Paper Award. He served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II, from 2010 to 2013. He is also an Associate Editor of the IEEE OPEN JOURNAL OF CIRCUITS AND SYSTEMS.

...