K-band combined GaAs monolithic Doherty power amplifier

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***Abstract*—This paper presents the design, simulations, and measurements of a 35 dBm K-band Doherty power amplifier, fabricated on 0.15 μm GaAs monolithic technology of Qorvo. The power amplifier is based on combining on-chip two Doherty modules with a matching power combiner. To demonstrate the power scaling and gain a better insight into the design, the single Doherty module has been fabricated and characterized as well. The Doherty output matching is designed for maximizing the bandwidth and minimizing the components count, with the output capacitance of the active devices determining the impedance inverter impedance. The combined Doherty shows an output power of 35 dBm at 24 GHz, that is almost exactly 3 dB larger than the single Doherty module power module, and with a 6 dB OBO efficiency of 27%, and a gain of 11.5 dB. It compares well with the state of the art, representing the highest power GaAs Doherty at similar frequencies.**

***Index Terms*—Gallium arsenide, K-band, microwave radios, power amplifiers.**

I. Introduction

The power amplifier (PA) is a crucial component of microwave transmitters for its impact on performance and cost, especially at high frequency. Among the several solutions proposed in literature to optimize the trade-off linearity/efficiency in PAs, the Doherty PA (DPA) [1], [2] is the reference choice at communication frequencies, and is gaining growing attention for higher frequency, medium power applications, as 5G, point-to-point radios, and satellite communications, where microwave monolithic integrated circuits (MMICs) are the common choice for the PA realization [3], [4], [5], [6], [7], [8], [9]. Despite few examples of GaN based DPA for K-band being proposed [5], GaAs technology is still perceived as a more reliable and less expensive choice. However, in GaAs, it is not straightforward to achieve Watt-level output power without compromising significantly bandwidth and efficiency, and DPA design it is even more complicated due to the need of controlling the load modulation [10], [11].

This paper presents a possible design approach to increase output power in a DPA design with low impact on bandwidth and complexity. The paper focuses on the output section of the DPA, while the driver stages and the related matching networks are only slightly modified from previous designs and hence of less interest.

II. Design approach

In high frequency PA design the size of the active device cell of the final stage is always a fundamental choice. The foundry is often able to indicate the maximum cell size that can be employed in a given frequency band, thanks to their preliminary load-pull characterization, non-linear device simulations, and design experience with their process. Then, if a power larger than the one of the single device is required, the PA has to be based on a combined structure. In the case of the DPA, the combination of more stages can be carried out at "device" level (internally to the main and auxiliary branches (Fig. 1 left), or by combining more DPAs (Fig. 1 right). In a general sense it is difficult to claim which solution

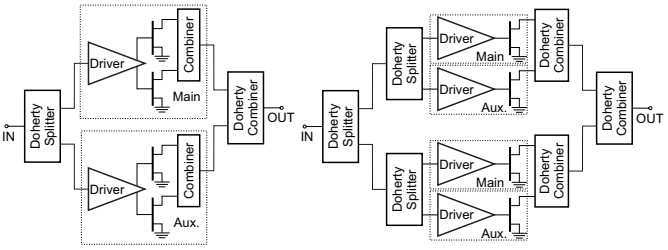


Fig. 1. Possible power combining approaches in DPA. Single DPA with combined devices (left). Combining two DPA modules (right).

is preferable. Considering that in K-band drivers are embedded in the main and auxiliary paths[6], [7], [8], [9], the solution in left of Fig. 1 seems much simpler from a routing point of view. However, the scheme of Fig. 1 right that potentially might have wider bandwidth, thanks to a better control of the load modulation, has been chosen for the here proposed DPA. At the same time, in order to mitigate the complexity of the routing, other aspects of the design have been considered, starting from the careful planning of the chip layout, see Fig. 2. The output matching of each DPA has to be connected to the drain bias pads on the side of the MMIC and needs to route the DC current to the internal interstage devices (red lines in Fig. 2). The main driver and final device are both biased in the same class AB point, so they can share the gate voltage rail (blue lines). Conversely, biasing the auxiliary driver and final device at different points can help improve output power, efficiency and linearity, so these gates are kept separated (green/purple lines). For this reason, in the layout, the main stages are placed internally and the auxiliary externally, since it will be easier to route a single gate to the middle of the chip.

To cover the whole 20.8-24 GHz band the design choice adopted for the present work has been to design the DPA combiner with minimum components count, using the equivalent output capacitance of the device C_{O}. The ideal impedance

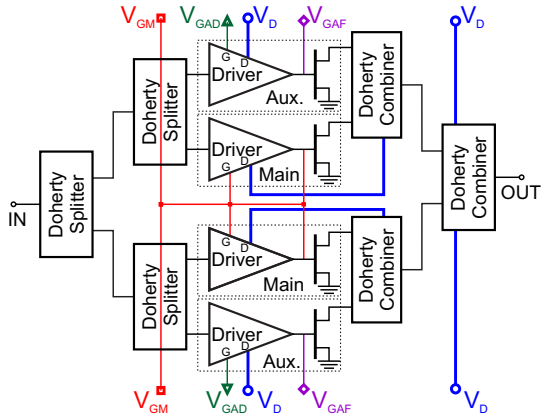


Fig. 2. Layout planning for the combined DPA.

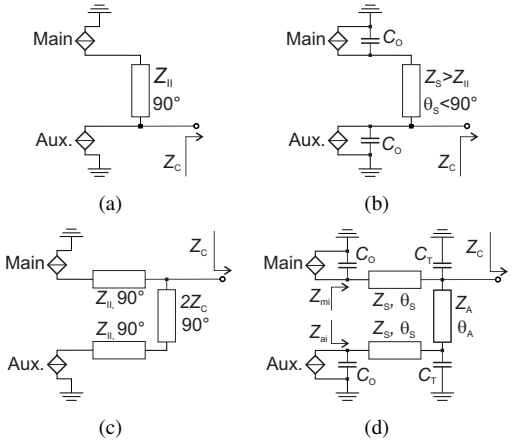


Fig. 3. Simplified schematics of DPA design solutions. (a) Conventional architecture. (b) Semi-lumped inverter absorbing device capacitance; (c) With non-inverting network on the auxiliary; (d) Like in (c), but with semi-lumped networks.

inverter of Fig. 3(a) has to be modified accounting for main and auxiliary equivalent output capacitance C_{O}, as shown in Fig. 3(b), where the transmission line characteristic impedance Z_{S} and length θ_{S} are designed to embed the effects of these capacitances. In particular, we choose to realize an equivalent impedance inverter with impedance

$$Z_{\mathrm{II}} = \sqrt{2R_{\mathrm{opt}}Z_C} \tag{1}$$

so that C_{O} are completely absorbed. This strategy, suited for the required broadband operation, however actually works only if $R_{\mathrm{opt}} = 2Z_{\mathrm{C}}$, and the line ($\theta_{\mathrm{S}}$) is long enough to physically connect the drain of the main and auxiliary devices. If one of these conditions is not verified, the equivalent scheme of Fig. 3(c) can be used instead, where the auxiliary branch is connected to the common node by two transmission line sections: the first identical to the main one, cascaded with a second one, restoring the auxiliary non inverting impedance transformation. The scheme of Fig. 3(d) represents the here adopted practical implementation of the ideal scheme of Fig. 3(c), accounting for the device output capacitances and implementing both sections as semi-lumped networks.

III. Design and Simulations

The maximum device size available from the employed 0.15 μm GaAs process of Qorvo at this frequency has a periphery of 1 mm, and provides a power of around 0.6 W when biased at 6 V, with an intrinsic optimum load $R_{\mathrm{opt}} = 20\,\Omega$. The equivalent output capacitance C_{O} can be estimated around 0.4 pF, that at the center design frequency of 22.4 GHz determines $Z_{\mathrm{II}} = 17.8\,\Omega$ and $Z_{\mathrm{C}} = 7.9\,\Omega$. Despite the favourable impedance values, with R_{opt} not too distant from $2Z_{\mathrm{C}}$, the solution of Fig. 3(b) had to be discarded because θ_{S} results too short to connect the two drain pins, and the scheme of Fig. 3(d) has been preferred. The resulting components values

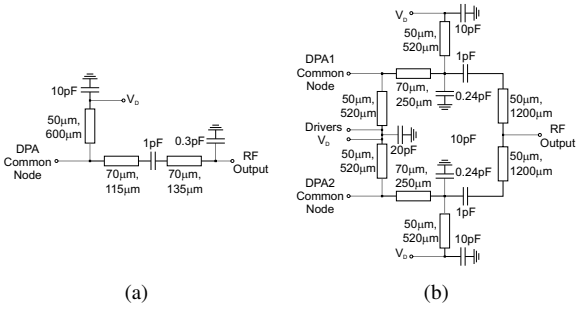


Fig. 4. Scheme diagram of the output matching in the (a) Single DPA, (b) Combined DPA. Transmission line dimensions are indicated as (width, length), already reflecting the optimization after EM simulations.

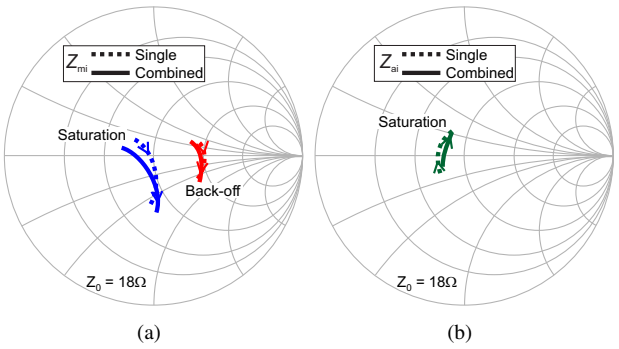


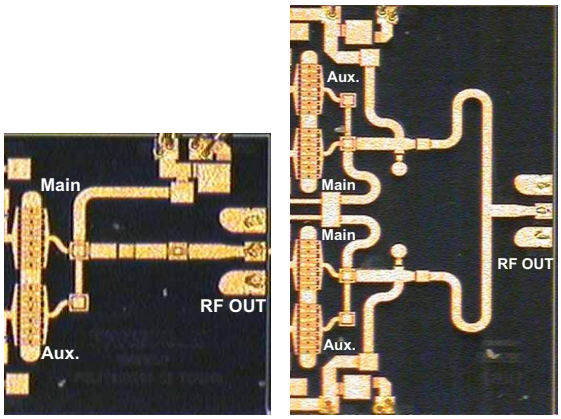
Fig. 5. Simulated intrinsic generator loads for single and combined DPA, in the 20.8–24 GHz band. Main device (a), auxiliary device (b).

of the Doherty combiner after some optimization to adjust the frequency behaviour on a design band from 20.8 GHz to 24 GHz, are: $Z_{\mathrm{S}} = 70\,\Omega$, $\theta_{\mathrm{S}} = 12°$ at 22.4 GHz, $C_T = 1$ pF. Two DPAs are designed; a single DPA, in order to test the behaviour of the DPA cell, and a combined DPA as for Fig. 1 (right). The common node impedance Z_{C} needs to be matched to 50 Ω in the single DPA case; this is achieved through the semi-lumped stub-line-stub structure shown in Fig. 4(a). In the combined DPA the matching is provided by the output combiner, whose scheme is shown in Fig. 4(b). The simulated fundamental load at the intrinsic generator plane

of the main and auxiliary devices ($Z_{\rm mi}, Z_{\rm ai}$ in Fig. 3(d)) is shown in Fig. 5(a) and Fig. 5(b), respectively, for the single and combined DPA. The load trajectories are in good agreement, suggesting that similar efficiency behaviour can be expected from single and combined DPA.

IV. Characterization

The manufactured single and combined DPA MMICs have a size of 2.9x1.4 mm^2 and 3.7x2.4 mm^2, respectively. Fig. 6 shows the microscope pictures of the output sections of the two MMICs. Since the driver stages are very similar to a previously published work by the same authors, the full pictures will be provided in the final paper only to avoid authorship disclosure.



(a) (b)

Fig. 6. Microscope picture of: (a) Single, (b) Combined DPA output section.

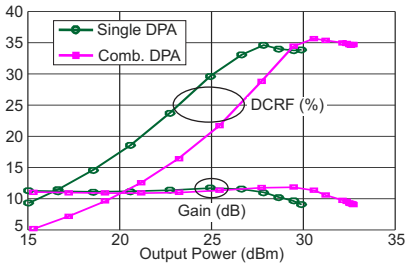


Fig. 7. Measured CW gain and efficiency (DCRF) vs. output power at 24 GHz. Comparison between single DPA (blue circles) and combined DPA (red squares) at same bias point.

Fig. 7 shows the measured gain and efficiency of the single and combined DPAs at 24 GHz. In both cases, the bias is $V_{\rm D}$=6 V, main current at 100 mA/mm for driver and final, and auxiliary with $V_{\rm GAD}$= -1.3 V, $V_{\rm GAF}$= -0.95 V. At 2 dB compression, the combined DPA shows an output power of 1.9 W, almost exactly 3 dB larger than the single DPA, and with an efficiency of 35%. For both DPAs, the 6 dB back-off efficiency is of 25%, with a small signal gain of 11.5 dB. Table I compares the combined DPA results with other GaAs DPAs at similar frequencies. A full characterization over the 20.8-24 GHz band was prevented by parametric oscillations appearing in the low

TABLE I
Comparison with previously published GaAs MMIC DPAs.

Ref.	Freq. (GHz)	$P_{\rm MAX}$ (W)	$\eta_{\rm MAX}$ (%)	$\eta_{\rm OBO}$ (%)	Gain (dB)	Size (mm^2)
[6]	26.4	0.3	38	27	10.3	25.0
[7]	24	1.1	38	20	12.8	4.29
[8]	26.6	0.5	42	32	10.5	25.0
[9]	29.5	0.5	38	32	10.5	4.59
This	**24**	**1.9**	**35**	**25**	**11.5**	**8.88**

portion of the band (20.8–23.2 GHz). Since this instability is present for both the single and combined stages, we excluded that is a consequence of odd-mode oscillations due to the lack of isolation resistor at the output combiner. On the other hand, by using an innovative simulation approach, the possible source of instability has been identified and a re-design of the critical elements performed. The new version of the DPA has been fabricated and it is now under measurement to verify experimentally if the problem has been solved.

V. Conclusion

The paper presented a design approach to achieve a 2 W Doherty power amplifier in K-band in GaAs technology. Two Doherty cells, designed for maximum bandwidth and minimum component counts, are combined with an on-chip matching combiner, leading to a power increase of ∼3 dB with negligible impact on efficiency and gain. The approach is made possible by a careful planning of routing and layout.

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