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Impact of Dead Times on Radiated Emissions of Integrated and Discrete DC-DC Converter

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***Abstract*—An integrated synchronous buck converter, designed in a 0.18-μm high-voltage CMOS technology, is analyzed to investigate the impact of the dead times between the control signals on the radiated emissions. The designed converter enables to set the dead times of the control signals for both integrated or off-chip transistor switches. The test boards are designed to analyze the impact of dead times on radiated emissions for integrated and discrete synchronous buck converter. The radiated emissions of both integrated and discrete converter are measured in a semi-anechoic chamber.**

***Index Terms*—dead times, radiated field, switching power converter, synchronous buck converter.**

I. Introduction

Higher power efficiency makes synchronous switching DC-DC converters more attractive for power supplies compared to non-synchronous converters [1]. However, due to their switching operation, switching DC-DC converters are a major source of conducted and radiated emissions, which is the main downside of these power supply circuits [2].

While the on-time of the high-side (HS) switch defines the voltage conversion ratio for the given switching period, the efficiency of the synchronous switching DC-DC converter is largely dependent on the duration of the dead times of the control signals [3]. It is also shown that even a sub-nanosecond shift of the dead times can have an impact on a far-field radiation of a switching DC-DC converter [4].

A number of papers analyzed the impact of various parameters of a DC-DC on its radiation characteristics, such as inductance of the package [5], input decoupling network [6] reverse recovery effect [7] or design of the output stage of the converter [8].

In this paper, an impact of dead times on radiated emissions is investigated for synchronous switching converters with integrated and off-chip driver stage and FET switches. The integrated synchronous buck converter is designed in a 0.18-μm high-voltage CMOS technology to achieve precise adjustment of dead times for both on- and off-chip high-side (HS) and low-side (LS) transistor switches [9].

Section II introduces the designed converter and measurement setup. In Section III, the radiated emissions measured using a semi-anechoic chamber are presented and discussed. Section IV concludes the paper.

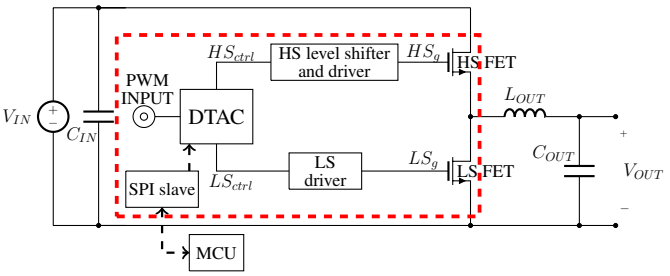

Fig. 1. Simplified schematic of a synchronous buck converter with the part designed on chip marked by the red dashed rectangle.

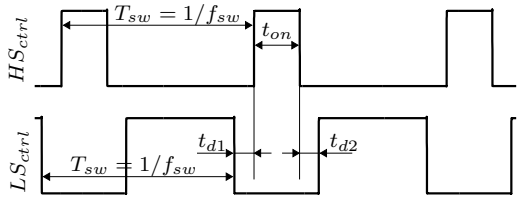

Fig. 2. Control signals for the HS and LS switch of the synchronous DC-DC converter with indicated switching period T_{sw}, on-time of the HS FET t_{on} and dead-times t_{d1} and t_{d2}.

II. Device Under Test and Measurement Setup

A. Designed integrated synchronous buck converter

The simplified schematic of the designed converter is marked in red-dashed rectangle in Fig. 1. The designed circuit consists of the dead-time adjustment circuit (DTAC) that generates the control signals for the FET switches [9], SPI communication 'slave' circuit, driver stages and transistor switches. Additionally, the outputs of the DTAC are routed to the output pins of the integrated circuit, which allows to use the external drivers and FET switches. The characteristic timings of the control signals, HS_{ctrl} and LS_{ctrl}, are set by an external microcontroller unit (MCU) and written into the 'slave' circuit by the SPI communication.

An example of the generated control signals HS_{ctrl} and LS_{ctrl} with characteristic timings is shown in Fig. 2. The switching frequency f_{sw} as well as the on-time of the HS FET t_{on} are defined by the PWM signal that is externally applied to the circuit. The control signals are used by the driver stage to

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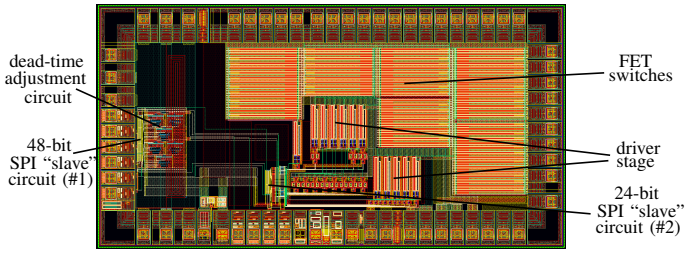

Fig. 3. Top view of the layout of the designed synchronous buck converter.

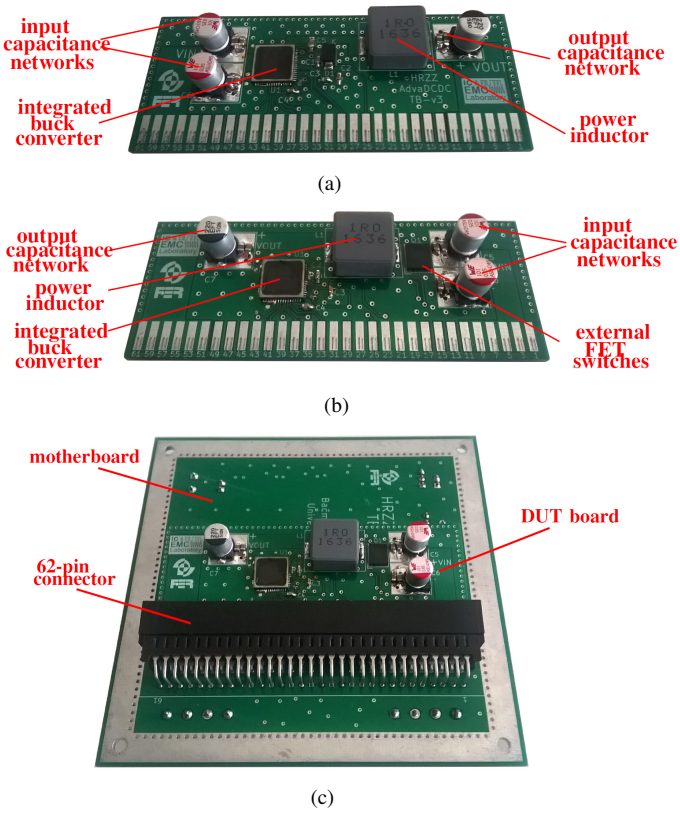

Fig. 4. Device under test (DUT) boards: (a) integrated converter (b), discrete converter and (c) motherboard.

produce the driving signals HS_g and LS_g. The driving signals are also routed to the output pins of the chip, which allows to use the designed integrated buck converter by itself or to use it with external drivers and FET switches. The driving stage can be turned on or off using the second on-chip SPI "slave" circuit depending on the usage of on-chip or external drivers and switches.

The top view of the layout of the designed integrated buck converter is shown in Fig. 3. It has an area of approximately 3100 × 1600 µm. The largest part of the chip belongs to the FET switches which are designed as three nMOS transistors in parallel in order to sustain larger currents during the on-time.

B. Test boards

Two converters are designed: an integrated (Fig. 4(a)) and discrete (Fig. 4(b)). The integrated converter has the driver stage and FET switches placed on the chip. Two 1-µF and one 10-µF multi-layer ceramic capacitors (MLCC) as well as two 100-µF electrolytic capacitors are used for the input decoupling network of the designed converter as proposed in [8]. A 1-µH inductor, one 1-µF, one 10-µF and one 100-µF capacitor are used for the output filter. An external bootstrap diode and capacitor are added to achieve the proper operation of the integrated converter.

In contrast to the integrated converter, a discrete one (Fig. 4(b)) uses an external driver and FET switches, while the designed integrated converter is used to provide the control signals for the driver. The device MCP14700 from Microchip drives the FET switches. The device FDMS3615S from Fairchild is used for the HS and LS switch. It is a dual n-channel MOSFET in a single package in which the source of the HS FET is internally connected to the drain of the LS FET.

Both converters are designed on the PCBs that enable their insertion into the 62-pin connector to the motherboard (Fig. 4(c)) that has a size of 100 mm × 100 mm that can be used for far-field estimation using a TEM cell. The 5-V battery voltage, load resistor and PWM signal are applied to the motherboard.

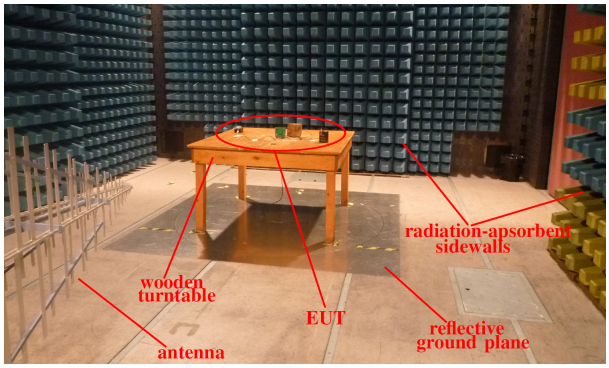

Fig. 5. Measurement setup in a semi-anechoic chamber.

III. Measurements

A. Test cases and measurement setup

Both integrated and discrete converter are tested under the same operating conditions: input voltage of 5 V, switching frequency of 1 MHz, duty cycle of 50%, load resistance of 5 Ω (output current of 0.5 A). The 5-V input voltage is applied to the board using the rechargeable battery instead of the voltage source which could affect measurement results. The PWM signal is applied from the arbitrary waveform generator that is placed outside the chamber.

The photo of the measurement setup in the semi-anechoic chamber is shown in Fig. 5. The equipment under test (EUT) is placed on the wooden turntable in the center of the chamber. Radiated field is measured by broadband antenna R&S HL562 and recorded by the EMI receiver R&S ESR 7. The measurements are done from 30 MHz to 1 GHz in 20000 points on the linear scale, using the quasi-peak detector and RBW filter of 120 kHz, for both vertical and horizontal position of

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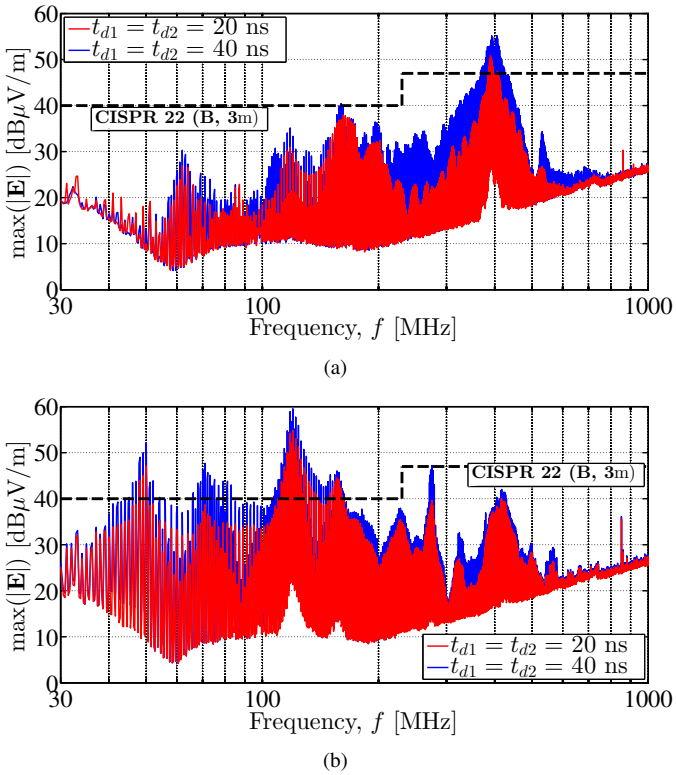

Fig. 6. Measured radiated field of (a) integrated and (b) discrete converter. The black dashed line represents the radiated emission limits according to the CISPR 22 standard for class B (3-m measurement distance) [2].

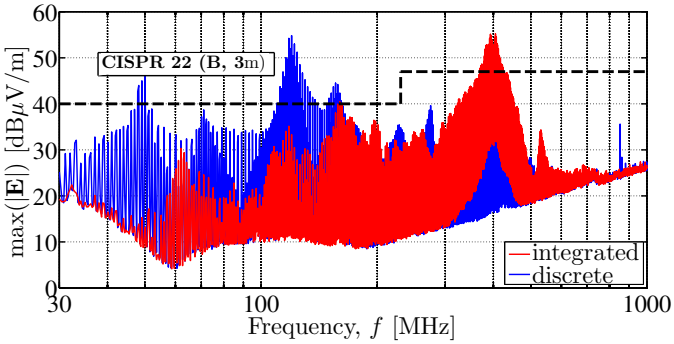

Fig. 7. Comparison of radiated field of discrete and integrated converter for dead times $t_{d1} = t_{d2} = 20$ ns.

the antenna at heights from 100 cm to 400 cm and turntable positions of 0°, 90°, 180° and 270°. The presented results are the largest radiated emissions that are measured at each frequency point for every turntable position, antenna height and polarization.

B. Radiated emissions

The radiated emissions of both integrated and discrete converter are measured for two values of dead times, 20 ns and 40 ns. Both dead times, at trailing and leading edge of the control signal, are equal. The dead times are generated by adjustment of the timings of the control signal for the LS FET to keep the same voltage conversion ratio.

The measured radiated emissions for the integrated converter are shown in Fig. 6(a). The largest radiated field is measured at frequency of approximately 400 MHz at which the resonance of the radiating loop is formed [8]. If the dead times are increased from 20 ns to 40 ns, the radiated field at the resonance is larger by 4.5 dB. Larger dead times between the control signals cause a drop of power efficiency and larger current from the battery is needed to achieve the same output power level. Larger input current flowing through the radiating loop causes larger radiated emissions.

The measured radiated emissions for the converter with external driver and FET switches are shown in Fig. 6(b). The largest field, i.e. the resonance, is observed at 120 MHz. The same increase of radiated emissions of 4.5 dB is observed at the resonant frequency when the dead times are twice larger.

The comparison of radiated emissions between integrated and discrete converter for dead times of 20 ns is shown in Fig. 7. The shift of resonant frequency to lower values is observed if the off-chip driver and FET switches are used due to the larger area, i.e. the parasitics of the radiating loop. The radiated field measured at the resonant frequency is around 55 dBμV/m for both integrated and discrete converter.

IV. Conclusion

A designed integrated synchronous buck converter with adjustable control signals is analyzed to investigate the impact of the dead times on the radiated emissions for converter with integrated and discrete switches. The larger dead times causes an increase of measured emission of 4.5 dB for both converters. The shift of the resonant frequency to lower values for the discrete converter is due to the larger radiating loop compared to the integrated converter.

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