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A 300mV-Supply Standard-Cell-Based OTA with Digital PWM Offset Calibration

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***Abstract*—This paper introduces a fully digital pulse-width-modulation (PWM) based calibration technique intended to dynamically compensate the input offset voltage due to process and mismatch in Ultra Low Voltage (ULV) Digital-Based Operational Transconductance Amplifiers (DB-OTA). Post-layout simulations on a DB-OTA circuit in 180nm featuring the proposed calibration technique demonstrate that process and mismatch related offset voltage can be effectively compensated by varying the duty cycle of a square wave signal with minimum performance overhead. The proposed OTA consumes just 7.34nW while driving a capacitive load of 80pF with a Total Harmonic Distortion lower than 2.26% at 100mV input signal swing. The total silicon area is 1,700 μm^2.**

***Index Terms*—Digital-Based OTA Circuit, Digital Offset Calibration, Process variability,Ultra-Low Voltage (ULV), Internet of Things (IoT).**

I. Introduction

Mostly digital, standard cell-based implementations of analog and mixed-signal functions have been intensively investigated over the last years to achieve Ultra-low Voltage (ULV), Ultra-Low-Power (ULP) operation as required in present day Internet of Things (IoT) applications at very low cost and design effort [1], [2]. In this scenario, fully digital implementations of many circuit building blocks have been proposed [3–10], including digital-based Operational Transconductance Amplifiers (DB-OTAs) [10], [11].

While digital OTAs can be extremely power and area efficient, their operation can be impaired by process variations and mismatch, which easily result in unacceptable offset voltage and reduced yield. Aiming to mitigate the effects of process spreads and mismatch, standard cells in critical parts can be designed with a strength which is much larger than minimum leveraging Pelgrom's law [12], analog layout guidelines should carefully followed and/or weighted element calibration networks are included to fine-tune the parameters of critical devices [10], as routinely done in analog circuits calibration [13]. In all the cases, however, robustness against process variations comes at the cost of significantly increased area and design complexity, which offset the advantages of DB-OTAs.

In this context, a novel, digital in concept approach to compensate process- and mismatch- variations in a DB-OTA with minimum area and performance overhead is proposed in this paper. The novel approach, which consists in the activation of a calibration device with a controlled duty cycle,

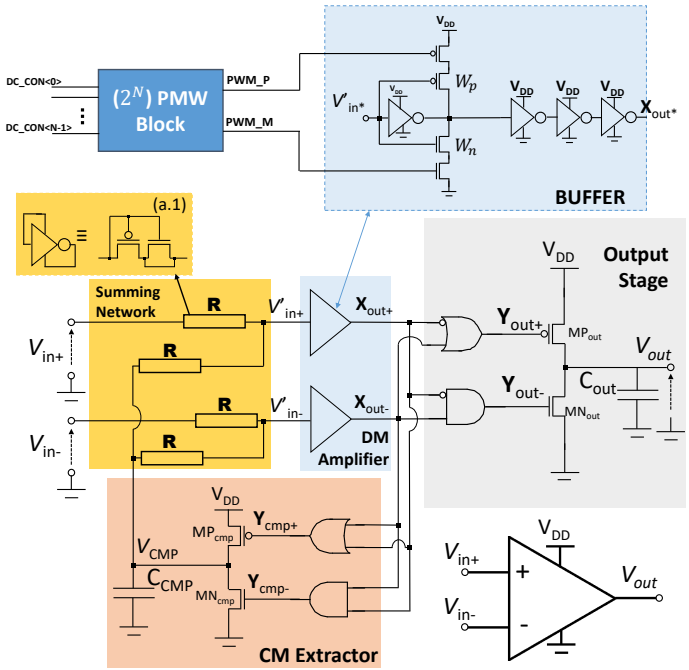


Fig. 1. DB-OTA schematic. N is the number of stages in the calibration inverter chain.

is demonstrated in a 300mV-power-supply standard-cell based OTA in 180nm CMOS on the basis of post-layout simulations.

The paper is organized as follows: in Section II, the DB-OTA operation is revised and the effects of process variations are highlighted. Then, the novel PWM calibration network is introduced in Section III and the effectiveness of the proposed calibration strategy is demonstrated in Section IV based on post layout simulations. In the same Section, the impact of the new calibration on the DB-OTA performance and power consumption is discussed and compared with other calibration approaches. Finally, in Section V, some concluding remarks are drawn.

II. ULV DB-OTA Circuit Description and Design

In this section, the operation principle of the DB-OTA first presented in [11] and then adopted in [10] to design an ULV OTA in 180nm is reviewed. Then, the network introduced in [10] to compensate process variations, which requires some custom analog design and layout effort, is focused and it is

replaced by a fully-synthesizable PWM modulator to make the digital OTA design fully compatible with a digital flow and to further reduce the overall design effort.

A. Digital-Based Differential Circuit Description

The schematic of a DB-OTA is shown in Fig. 1. The circuit is made up of a *Differential-Mode (DM) amplifier*, of a *Common-Mode (CM) extractor* loop, of a *summing network* and of an *output stage*, as in [11]. The main goal of this topology is to implement the same functionality of the classical CMOS differential stage with digital gates, i.e., to amplify the differential input signal $v_{\rm d} = (V_{\rm in+} - V_{\rm in-})$ while being insensitive to common mode input signal variations $v_{\rm cm} = \frac{(V_{\rm in+}+V_{\rm in-})}{2}$. To reach these goals, the *DM Amplifier*, which is formed by two digital buffers, is used to sense the level of the input voltages w.r.t. the buffers voltage tripping points ($V_{\rm T}$) resulting in four possible logical outputs: $(X_{\rm out+}, X_{\rm out-}) = (0,0),(1,1),(1,0),(0,1)$.

Whenever $(X_{\rm out+}, X_{\rm out-}) = (0,1),(1,0)$ the *output stage* is activated and $V_{\rm out}$ is increased/decreased depending on $v_{\rm d}$. Otherwise, when $(X_{\rm out+}, X_{\rm out-}) = (0,0),(1,1)$, the *CM Extractor* is turned on to correct the input CM signal.

Once it is sensed that the CM input signal must be corrected, the transistor $\rm MN_{cmp}$ ($\rm MP_{cmp}$) is turned on and $C_{\rm CMP}$ is properly discharged (charged) and the generated $V_{\rm CM}$ signal is then subtracted from the input through the *summing network* ($V'_{\rm in+(-)} = 0.5(V_{\rm CMP} + V_{\rm in+(-)})$). On the other hand, when the CM input component is within the CM input range, the transistors $\rm MP_{out}$ and $\rm MN_{out}$ are operated depending on the sign of $v_{\rm d}$ so that to charge or discharge $C_{\rm OUT}$ according to the input differential signal. A detailed analysis of the circuit under dynamic conditions can be found in [11].

B. Process Variations and Calibration

The operation of the ULV DB-OTA can be severely impaired by process variations and mismatch in the trip points $V_{\rm T}$ of the first inverters of the *DM amplifier*, which result in an input offset voltage [11]

$$V_{OFF} = \Delta V_T + \frac{I_{OUT}}{C_{OUT}} \Delta t_D \qquad (1)$$

where $\Delta V_{\rm T} = V_{\rm T1} - V_{\rm T2}$ is the difference between positive and negative path trip points and Δt_D is the difference in the propagation delays of the two branches of the DM amplifier. I_{OUT} is the output stage current capability. For minimum-size devices, in particular, the offset predicted by (1) can be easily large enough to saturate the DB-OTA, thus fully impairing the DB-OTA operation.

Since the trip points $V_{\rm T}$ depend on the aspect ratios of the pull-up and pull-down devices as

$$V_{\rm T} = \frac{\frac{\kappa T}{q} \log\left(\frac{I_{\rm D0P}\left(\frac{W}{L}\right)_{\rm P}}{I_{\rm D0N}\left(\frac{W}{L}\right)_{\rm N}} \right) + \frac{V_{\rm DD}}{n_{\rm P}}}{\frac{1}{n_{\rm P}} + \frac{1}{n_{\rm N}}} \qquad (2)$$

where the parameters have their usual definitions [14], the effects of process variations can be in principle compensated by in post-fabrication calibration by tuning the aspect ratio of either the pull-up or the pull-down device.

With this aim, a calibration network consisting of pMOS (nMOS) devices with binary weighted width $2^k W_0$, to be connected in parallel to first stages of the DM amplifier depending on a calibration code, has been introduced in [10]. That calibration network, however, is not compatible with a pure digital flow and requires some extra analog design and layout effort. In view of these limitations, a different, all-digital

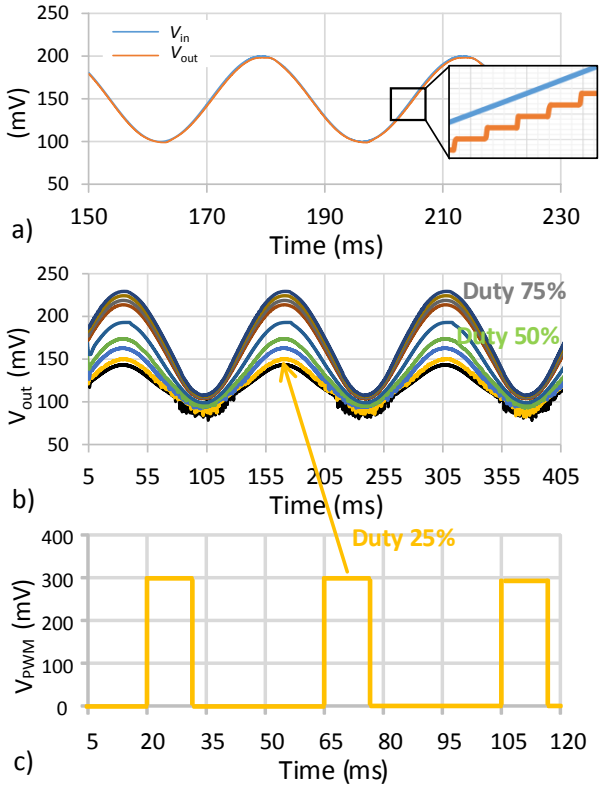


Fig. 2. a) V_{in} and V_{out} for $C_{out} = 80\,pF$, $V_{amp} = 50\,mV$ and $f_{in} = 30\,Hz$. b) V_{in}, V_{out} before calibration (black) and V_{out} after calibration (red) for $C_{out} = 80\,pF$, $V_{amp} = 50\,mV$ and $f_{in} = 120\,Hz$. c) PWM calibration signal.

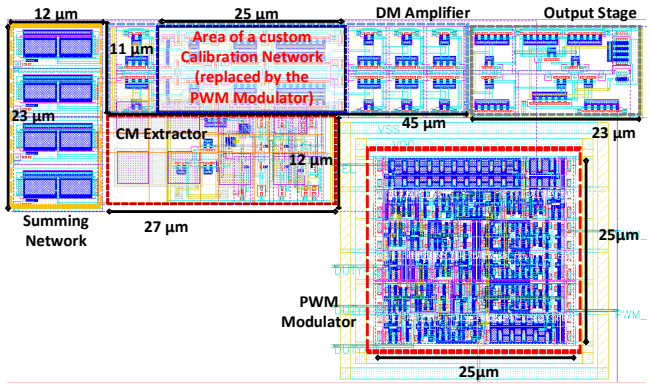


Fig. 3. DB-OTA layout. Total area of 1,700 μm^2.

calibration approach is explored in this paper.

C. PWM Calibration Network

The proposed PWM calibration network consists of a calibration inverter driven by the input signals and connected in parallel to the first stage of each branch in the DM amplifier, as depicted in Fig.1. The pull-up (pull-down) network of the calibration inverter can be tied to the supply (to ground) through a pMOS (nMOS) power gating switch, as depicted in the figure. When the pMOS (nMOS) gating switch is on, the pMOS (nMOS) of the calibration inverter, with width W_n (W_p) is enabled and connected in parallel to the nMOS (pMOS) device in the first stage of the DM amplifier, thus effectively increasing its width and significantly reducing (increasing) its trip point according to (2).

In the proposed calibration network, one of the power gating switches is driven by a square wave, N-bit digital pulse-width modulated (PWM) voltage with a duty cycle $D = n/2^N$ that can be configured by the calibration code n as in Fig.2. As far as the PWM frequency is larger than 10X the DB-OTA GBW, it is observed that periodically enabling the nMOS (pMOS) network of the calibration inverter has the same net effect on the trip points of the DM amplifier gates as increasing the width of the DM amplifier devices by DW_n (DW_p), as shown in Fig.2, where the DB-OTA output waveforms obtained with the same input signal under different PWM duty cycles of the enable signal for the pMOS and nMOS branches.

The proposed PWM calibration approach has been adopted in a DB-OTA designed as in [10] to compensate process variation and mismatch and its effectiveness will be discussed in the following on the basis of post-layout simulations.

III. Post-Layout Simulations

In order to validate the proposed PWM calibration approach, a DB-OTA has been designed and laid out in 180nm CMOS. A 3-bit digital PWM modulator has been synthesized in a digital flow to generate the gating signals for the proposed PWM calibration. The overall layout, including the calibration network, occupies just 1,700 μm^2 as shown in Fig. 3.

The proposed DB-OTA has been designed as in [10] to operate at $V_{DD} = 300$mV power supply driving up to 80pF capacitive load and its nominal performance, verified by post-layout simulations, are briefly summarized in what follows. Then, the possibility to replace the custom calibration network introduced in [10] by the PWM calibration described above is verified by post-layout MonteCarlo simulations.

A. Performance under Nominal Conditions

The input and output waveforms of the proposed DB-OTA under nominal process parameters, at $V_{DD} = 300$mV, with sine wave input at 30Hz frequency, 50mV peak amplitude and $C_{out} = 80$pF capacitive load are reported in Fig.2(a) and reveal the operation of the circuit as an opamp and less than 2% THD and 2nW power consumption. A zoom in the waveform shows the step-wise changes in v_{out} resulting from digital operation. Fig.4 depicts THD versus the sinewave input

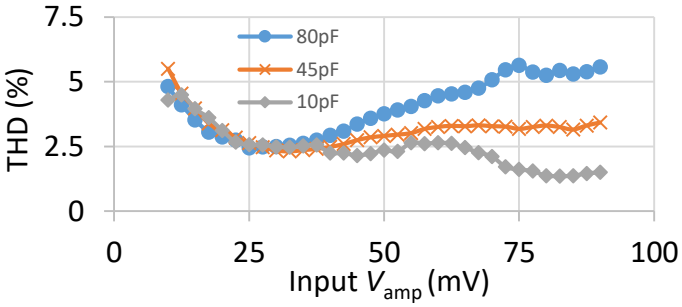


Fig. 4. THD (%) versus V_{amp} (nominal process parameters, no mismatch)

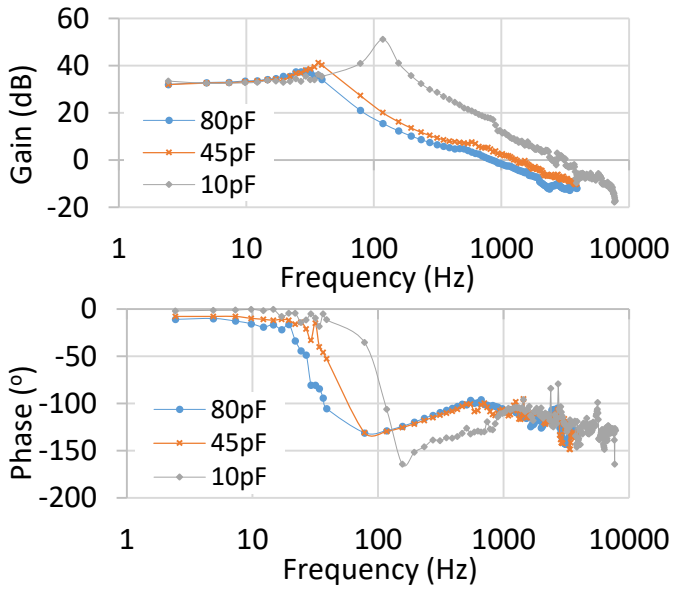


Fig. 5. ULV DB-OTA frequency response (nominal process parameters, no mismatch).

signal amplitude V_{amp} for three different values of the output capacitance $C_{out} = 80, 45, 10$pF keeping $f_{in} = 120$Hz.

The frequency response of the DB-OTA, estimated as the ratio of the Fast Fourier Transform (FFT) component at the fundamental frequency f_0 of the output and of the differential input voltage, $A_d(f) = \frac{V_{out}(f)}{V_d(f)}$ is reported in Fig.5 for different capacitive loads. Based on the figure, the DB-OTA shows 35dB DC gain and 0.85, 1.3 and 2.48kHz Gain Bandwidth Product (GBW) with phase margin 76°, 68.5° and 57° under $C_{out} = 80, 45$ and 10pF load, respectively.

B. Process Variations and PWM Calibration Validation

The DB-OTA without calibration has been tested under process variations for $V_{amp} = 50$mV, $C_{out} = 80$pF and $f_{in} = 120$Hz by Montecarlo (MC) simulations on 100 samples. The histogram of the output THD is reported in Fig.2(c) and reveals a noticeable number of samples exceeding 10% THD due to the spread in the trip voltages of the *DM amplifier* ΔV_T, which in the worst cases (89% THD) results in the output voltage saturation, as shown in Fig.2(b).

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART ULTRA-LOW-VOLTAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Performance	[15]+	[16]+	[17]+	[18]+	[19]*	[20]* MC-OTA	[20]* FFC-OTA	This work*				Unit
								Typical Condition	Worst case mismatch and process			
									No Calib.	Custom Calib.	PWM Calib.	
Technology	65	130	180	350	65	130	130	180	180	180	180	nm
Supply Voltage	0.35	0.25	0.5	0.6	0.3	0.3	0.3	0.3	0.3	0.3	0.3	V
DC Gain	43	60	52	69	60	46.2	49.8	35	N/A	27	26	dB
GBW	3600	1.88	1,200	11.4	70	2,450	9,100	0.85	N/A	0.59	0.47	kHz
Slew Rate	5600	0.7	2,890	14.6	25	2,400	3,800	0.5	N/A	0.38	0.39	$\frac{V}{ms}$
THD	0.6	0.2	1	0.08	-	-	-	3	89	2.6	2.26	%
Phase Margin	56	52.5	-	65	53	52	76	76	N/A	70	67	^{o}
C_{out}	3	15	20	15	5	2	2	80	80	80	80	pF
Power	17,000	18	110,000	550	51	1,800	1,800	2	N/A	1.64	7.34	nW
Area	5,000	83,000	26,000	60,000	3,000	-	-	1,426	1,426	1,426	1,700	μm^2
FOM_S	19	29	0.11	0.18	2.05	81	303	1020	N/A	857	153	V^{-1}
FOM_L	34.6	14.6	26.27	23.9	73.4	80	140	600	N/A	553	127	-

+experimental; *simulation;
$FOM_S = 100\frac{GBW C_{OUT}}{I_{DD}}$; $FOM_L = 100\frac{SR_{avg} C_{OUT}}{I_{DD}}$ where $SR_{avg} = \frac{SR_+ + SR_-}{2}$ is the slew rates (averaged between negative and positive) and I_{DD} is the RMS current consumption.

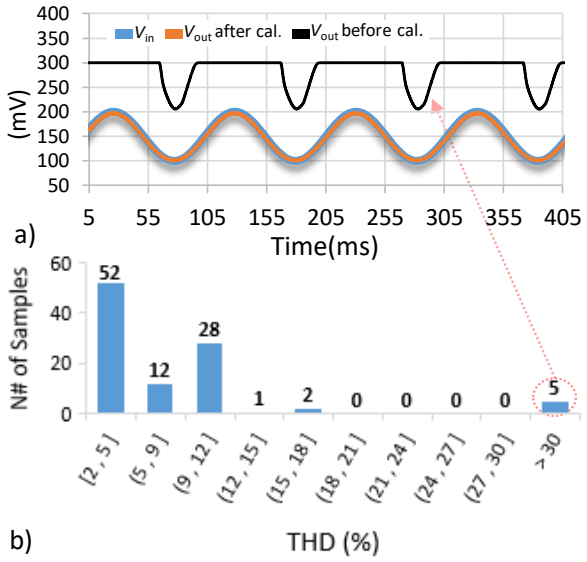


Fig. 6. a) output voltage of the worst sample with and without PWM calibration b) THD histogram of 100 montecarlo samples

In order to validate the proposed PWM calibration approach, the worst samples resulting form the above MC analysis have been considered. Even in these worst cases, a decent performance has been recovered by properly programming the digital PWM modulator with a 3-bit code so that to generate a PWM signal with 24μs period and with a convenient duty cycle, and to apply it either to the pMOS or to the nMOS enable switches in Fig.1. In Fig.6, in particular, the DB-OTA output voltage waveform for the worst sample, before and after PWM calibration, is reported.

The performance of the worst MC sample after PWM calibration has been compared with the performance of the same sample when calibrated by the traditional custom approach described in Section.IIb. The results reported in Tab.I reveal that the samples calibrated by the traditional and by the PWM approaches show comparable GBW, slew rate and gain and that the THD is even lower for the PWM calibration. The overhead in terms of power of the PWM calibration strategy is 5.34nW, i.e. the power consumption of the PWM modulator. The comparison with state of the art ultra-low voltage (ULV) OTAs reveal competitive performance also for the worst case samples after calibration.

IV. CONCLUSION

A fully digital dynamic calibration to compensate process and mismatch related offset in ULV DB-OTA has been presented. An opamp circuit featuring the proposed calibration technique in 180nm CMOS has been designed and verified by post-layout simulations, which demonstrates that process and mismatch variations can be effectively compensated in a fully digital way by varying the duty cycle of a square wave signal with minimum performance overhead. The proposed OTA consumes just 7.34nW while driving a capacitive load of 80pF with Total Harmonic Distortion lower than 2.26% at 100mV input signal swing. The total silicon area is 1,700 μm^2. The results demonstrate the feasibility of a fully synthesizable, technology portable and minimum design effort approach in DB-OTA calibration.

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