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# Resistive switching in ALD metal-oxides with engineered interfaces

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# Summary

Resistive Random Access Memories (ReRAMs), belonging to the wide family of memristive devices, have recently gained great attention for their logic-in-memory capability and the ability to mimic the biological synapses behavior, becoming a good candidate for the realization of new technologies able to overcome the bottleneck of Von Neumann architectures. In this study, metal-insulator-metal (MIM) devices are considered, where the active layer consists in a binary metal-oxide thin film deposited via atomic layer deposition (ALD). The first part of the dissertation is devoted to the inspection of the correspondences between the internal dynamics responsible of the switching and the engineering of active layer and electrodes. The influence of several factors is inspected, such as the device geometry, the active layer composition and the electrode materials. The choice for the active layer in this material-based study falls on oxides that are not conventionally used in microelectronic components. In particular, an extensive study on ZnO is reported, including DC and AC characterizations. Moreover the ALD doping process is defined and the impact of the insertion of partial $Al_2O_3$ single-layers in ZnO and $TiO_2$ thin films is inspected, dealing with the differences in the material properties (such as structure, morphology, stoichiometry...) and in the memristive response. In the second part of the dissertation, $HfO_2$-based devices are introduced. These devices, with their low temporal and spatial variability, allow systematic electrical tests. The main purpose in this part is the study of multi-bit information storage and resistance multi-state control. The multi-state retention, the behavior reliability over consecutive programming operations and the impact of different programming stimuli are the main explored elements. Finally, the multi-resistance control is achieved by pulse rise time modulation, thanking advantage from the multi-oxidation states of the W top electrode and the proper engineering of oxide/electrode interfaces.

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# Chapter 1

# Introduction

## 1.1 Motivation

Neuro-inspired technologies, which can mimic the behavior of biological neural networks and act as our brain, are one of the hot topics of the moment. In recent years, the amount of data to be processed is increasing exponentially, demanding new technologies and architectures for data processing and storage. Suffice it to remember that embedded systems and Internet of Things are surrounding our every-day life, ranging from the smart sensors to the autonomous driving tools, from wearable devices to systems that can interact with machine through natural language. If on one hand the accuracy in recognition and classification for large-scale visual/auditory data-base imposes deep learning algorithms, which require depth and big neural networks, on the other hand severe fabrication constraints in term of power consumption and design area are mandatory. In order to allow the reader to get a rough estimation of the complexity of the networks, we can report as example the Google's stacked auto encoder algorithm. The ability to detect specific images from $10^7$ random patterns taken from YouTube videos was achieved by a cluster of 16000 processor cores for a power consumption of $\sim$100 kW and a training of three days.
The conventional Von Neumann architectures, with their dislocation of memory and processing units, have been forced to a bottleneck, facing the so called Von-Neumann memory wall. In fact, in these circuits the separation of microprocessor and storage system determines a high latency in terms of data transfer between the

two units and strict limits in the circuit scalability and in the reduction of the power consumption. The problem becomes not negligible especially when the data-set is extremely large, which is the case for the training databases for complex neural networks. One promising solution to Von Neumann memory wall is the introduction of neuro-inspired systems based on state-full logic, since these systems allow a co-localization of computing and memory resources. Artificial synapses, coherently with the biological ones, are dynamic connections that can strength or weaken the data transmission between linked network nodes and remember the weight over time (plasticity). From this point of view, synapses act contemporary as processing unit, modulating the information transmitted across, and as memory, thanks to their plasticity properties. In this scenario, resistive-switching random access memories (ReRAMs), belonging to the huge category of memristor devices, have recently gain great interest in the the scientific community. In ReRAMs, the memory principle is related to the retention of an internal resistance state, whose value depends on the history of applied current and voltage. Although a general model of the internal dynamics of the devices and the complete control of performances are still open issues, high scalability, low power consumption, fast operation time, long retention and logic-in-memory capability are key properties of ReRAMs. Moreover, the memristor ability in emulate the synapses behavior marks these devices as interesting candidates to be employed as artificial synapses in the realization of neuro-inspired circuits.

## 1.2 Memristor Overview

### 1.2.1 Memristor and Resistive Switching

The first definition of *Memristor* dates back to 1971, when Leon Chua claimed the discovery of the fourth fundamental circuit element [1]. He observed that the other three passive elements were defined by coupling two of the four fundamental electronic variables, i.e. current, voltage, magnetic flux and charge ($I$, $V$, $\phi$ and $q$), as presented in the scheme of Figure 1.1. The relation between $\phi$ and $q$ was still missing. Therefore, by analogy to resistor, capacitor and inductor, the memristor was defined as the passive electronic component whose constitutive equation is a

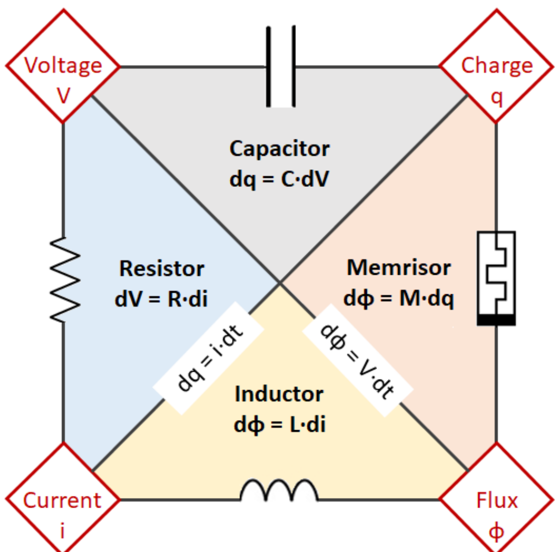


Figure 1.1: Schematic representation of electrical fundamental variables and relations

direct relation between charge and flux, expressed by:

$$\begin{aligned} \phi &= f(q) \\ d\phi &= M(q)dq \end{aligned} \tag{1.1}$$

Where $M(q)$ is the so called *Memristance* and determines the intrinsic non-linearity of the circuit element, since is itself a function of q. The variable $\phi$ has to be considered not as the magnetic flux, but as the integral of voltage in time. For this reason, $\phi$ is defined as *voltage momentum* [2].
Considering the time derivative of Equations 1.1, the definition can be quantified in term of $I$ and $V$:

$$\begin{cases} V(t) = \dfrac{df(q)}{dq} I(t) = M(q)I(t) \\ \dfrac{dq}{dt} = I(t) \end{cases} \tag{1.2}$$

Through these expressions, it is easy to visualize a memristor as an element that can store an internal state ($M$ value) depending on the charge passing through the device in the time interval by the effect of the applied voltage. Moreover, considering the equations 1.2, one can extract the memristor fingerprint, which consists in the peculiar I-V hysteresis loop pinched in the origin of axis.

The original definition was extended in 1976 to a broader class of devices [3] through the insertion of a state variable $x(t)$. The new set of equations is the mathematical definition of the memristor:

$$\begin{cases} \phi = f(q, x(t)) \\ \dfrac{dx(t)}{dt} = g(x, I) \\ \dfrac{dq(t)}{dt} = I \end{cases} \tag{1.3}$$

which become in terms of voltage and current:

$$\begin{cases} V(t) = M(q, x(t))I(t) \\ \dfrac{dx(t)}{dt} = g(x, I) \end{cases} \tag{1.4}$$

Where the function $g(x, t)$ controls the evolution over time of the state variable and its explicit form depends on the device physical dynamics. In this way, the contribution of variables such as applied field, internal temperature and defect concentration are taken into account.

The link between memristor theory and resistive switching on experimental devices was established in 2008 by HP lab members Strukov and Williams [4], gaining soon a huge interest in the scientific community. They proposed a Pt/$TiO_2$/Pt thin film device which was able to switch between two different resistance states by voltage control, presenting the peculiar I-V characteristic pinched in the origin, as theorized by Chua. The connection between mathematical expression and electronic devices, led to the definition of a memristor device as an electrical resistance switch that can retain a state of internal resistance based on the history of applied voltage and current. Since the 2008 claim, the attention of scientific community to the memristor devices has been growing. In particular, the simple two terminal metal-insulator-metal (MIM) structures, in which a metal oxide layer is inserted between two electrodes, have shown good performances and have been extensively studied. Many valuable results are reported in the reviews [5–9]. Plenty of binary oxides, and especially transition and lantanide series metal oxides, exhibited resistive switching properties, combined with different electrode materials (Figure ), including the conductive nitrides (e..g. TaN and TiN). Among the oxides, $HfO_x$,

$TaO_x$, $ZrO_x$ and $AlO_x$ have drown most attention, since they are extensively employed in the fabrication of micro-electronic components.

Figure 1.2: Periodic table of the elements, presenting the oxides and metals employed in the memristor device realization. Taken from [10].

### 1.2.2 Working principle

The commercialization of any device application imposes a high repeatability in switching performances and a deep understanding of the internal dynamics and mechanisms responsible for the resistance variation. Many chemical interactions and physical phenomena have been considered to be involved in the resistance switching, mainly controlled by electric field and Joule heating, through the applied voltage. Among them, concerning the metal-oxide MIM structures (Figure 1.3a), the resistance change is related to the filamentary switching. The working principle behind filamentary switching is based on the formation/rupture of a conductive filament (CF) in the insulating layer, whose shape and evolution dynamics depend on: used materials, involved chemical reactions and physical phenomena. Several simulations and models were reported in order to describe the CF evolution under applied stimuli [11–17]. Moreover, the past decade improvements in characterization of nano-scale materials enabled the in-situ observation and study of the CF. In particular, a first confirmation of the filamentary switching mechanism was achieved by conductive-AFM [18, 19], which allowed the CF detection in different

metal oxides. Using high-resolution transmission electron microscopy (HR-TEM), the CF evolution during SET and RESET operations was observed in real time, making possible an estimation of the CF diameter dimension (<20nm) [20–23]. Depending on the CF nature and the mechanism that are involved in its formation, resistive switching mechanisms can be classified in different categories [24]. The most relevant in this work are the ones related to chemical reactions and ion migration, which are valence change (VCM) and electrochemical metallization (ECM) mechanisms and will be extensively explained in Sections 1.2.2 and 1.2.2. However, other switching phenomena have been reported, implying physical changes, such as magnetic-tunnel, ferroelectric and phase-change switches [25–27].

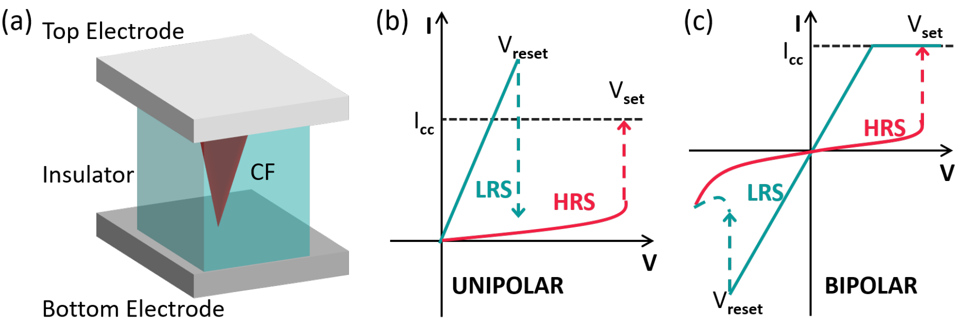


Figure 1.3: (a) Schematic representation of a basic MIM, which is a simple two terminal structure in which an insulator is sandwiched between two electrodes; the resistance switching is determined by CF formation-rupture. I-V characteristic scheme for unipolar (b) and bipolar (c) resistive switching; HRS, LRS, $I_{cc}$, $V_{set}$ and $V_{reset}$ are reported.

In both VCM and ECM, the first filament formation usually requires an electroforming procedure, in which the first filament formation takes place by carrier migration under applied voltage. When the forming voltage $V_{forming}$ is reached the current passing through the device increases and the resistance is subjected to an abrupt change. After this step, the CF rupture-rebuilt defines the switching between a low resistance state (LRS) and a high resistance state (HRS). The process in which the HRS→LRS transition occurs is called *SET* process, while the opposite transition LRS→HRS is called *RESET*. For both the forming and SET operations, is important to limit the maximum flowing current by setting a current compliance limit ($I_{cc}$), in order to avoid the breakdown of the device. Two different switching modes are achievable depending on the input stimuli, the insulating layer material

and the involved mechanism: *unipolar* (Figure 1.3b) when SET and RESET procedures are performed in the same electrical polarity, and *bipolar* (Figure 1.3c), when the two procedures are forced in opposite polarities. Certain devices have shown coexistence of both the switching modes [28, 29]. In order to control and modulate CF formation-rupture and to stabilize the process over time, extensive studies have been carried out, following different approaches. Material engineering (including active layer composition, electrode choices ad substrate material selection) and control of the electrical input stimuli are two of the major techniques for CF modulation. The material engineering approaches include the doping of the active layer [30] and the oxide/electrode interface modification, achieved by the insertion of additive layers. These can be categorized as oxygen barrier layers (for example $Al_2O_3$) [31–33], and oxygen scavenging layer (Ti, Ta and Hf) [34, 35], depending on the properties of the chosen material.

| **Conduction Mechanism** | **Current Density Expression** | **Electric Field and Temperature Dependency** [b] |
|---|---|---|
| Schottky Emission | $J_{SE} = \frac{4\pi q m^*(kT)^2}{h^3}\exp\left[\frac{-q(\phi_B-\sqrt{qE/4\pi\varepsilon})}{kT}\right]$ | $J_{SE}\propto T^2\exp\left(A\frac{\sqrt{E}}{T}-B\right)$ |
| Fowler-Nordheim (F-N) Tunneling | $J_{FN}=\frac{q^2}{8\pi h\phi_B}E^2\exp\left(\frac{-8\pi\sqrt{2qm^*}}{3hE}\phi_B^{3/2}\right)$ | $J_{FN}\propto E^2\exp\left(\frac{-A}{E}\right)$ |
| Direct Tunneling | $J_{DT}\approx\exp\left\{\frac{-8\pi\sqrt{2q}}{3h}(m^*\phi_B)^{1/2}\kappa\cdot t_{ox,eq}\right\}$ | $J_{DT}\propto\exp(-A\cdot\kappa t_{ox,eq})$ |
| Poole-Frenkel (P-F) Emission | $J_{PF}=q\mu N_C E\exp\left[\frac{-q(\phi_T-\sqrt{qE/\pi\varepsilon})}{kT}\right]$ | $J_{PF}\propto E\cdot\exp\left(A\frac{\sqrt{E}}{T}-B\right)$ |
| Space-charge-limited Conduction (SCLC) [a] | $J_{SCLC}=\frac{9}{8}\varepsilon_i\mu\theta\frac{V^2}{d^3}$ | $J_{SCLC}\propto E^2$ |
| Ionic Conduction | $J_{ionic}\propto\frac{E}{T}\exp\left\{\frac{-\Delta G^{\neq}}{kT}\right\}$ | $J_{ionic}\propto\frac{E}{T}\exp\left(\frac{-A}{T}\right)$ |
| Ohmic Conduction | $J_{ohmic}=\sigma E=q\mu N_C E\exp\left[\frac{-(E_C-E_F)}{kT}\right]$ | $J_{ohmic}\propto E\cdot\exp\left(\frac{-A}{T}\right)$ |
| Nearest Neighbor Hopping (NNH) | $J_{NNH}=\sigma_0\exp\left(\frac{-T_0}{T}\right)\cdot E$ | $J_{VRH}\propto E\cdot\exp\left(\frac{-A}{T}\right)$ |
| Variable-range Hopping (VRH) | $J_{VRH}=\sigma_0\exp\left(\frac{-T_0}{T}\right)^{\frac{1}{4}}\cdot E$ | $J_{VRH}\propto E\cdot\exp\left(\frac{-A}{T}\right)^{\frac{1}{4}}$ |
| Trap-assisted Tunneling (TAT) | $J_{TAT}=A\exp\left(\frac{-8\pi\sqrt{2qm^*}}{3hE}\phi_T^{3/2}\right)$ | $J_{TAT}\propto\exp\left(\frac{-A}{E}\right)$ |

[a] High field only, low field follows Ohm's Law; [b] A & B are constants.

Figure 1.4: Typical conduction mechanisms observed in ReRAM and their dependency from electric field and temperature. Extracted from [36].

Regarding the current conduction mechanism inside the device during SET and RESET operations, it is crucial to identify the correct physical transport model in order to exploit the device properties. To this purpose, the I-V curves in ln-ln scale are interpolated by a linear fit [36]. The table reported in Figure 1.4 summarizes the conduction mechanisms that were reported in literature for the ReRAMs. Several works agree on the linear/ohmic transport mechanism for the LRS, but the HRS conduction characteristic is still under debate: Schottky, Poole–Frenkel, Trap Assisted Tunnelling (TAT) and space charge limited current (SCLC) are the most accepted [36].

### Valence Change Memories

In VCM memories the main contribution for CF formation is related to the oxygen anion migration inside the insulating layer, which consists commonly in a metal-oxide. The bipolar devices presents an ohmic counter electrode with high oxygen affinity and an inert electrode, but also symmetric devices have been registered [36, 37]. The VCM switching process is represented in Figure 1.5a. When a voltage drop is applied, a soft dielectric breakdown occurs and $O^{2-}$ ions drift under the effect of high electric field, reaching the anode electrode. At the interface with the anode, $O^{2-}$ can be discharged as neutral oxygen if the electrode is a noble metal or be reduced by interaction with an active material. In the second case, an oxide thin layer is formed at the interface and the active electrode acts as an oxygen reservoir layer. The resulting CF is a sub-stoichiometric oxide path made of oxygen vacancies (Vö) as a consequence of the ion migration, resulting in a valence change of the metal-oxide layer. During the RESET, oxygen ions are created by redox reactions at the electrode/oxide interface and migrate back, recombining with Vö. The device switches back to HRS. Therefore, the SET process can be considered as a dynamic reconstruction of the partially ruptured CF along the gap opened during RESET, while the main part of CF remains stable over cycling [38]. Moreover, after the first filament formation, the creation of new CF by SET is less likely to form during the SET process because the electric field, current, and temperature are considerably higher in the region close to the partial CF [39].

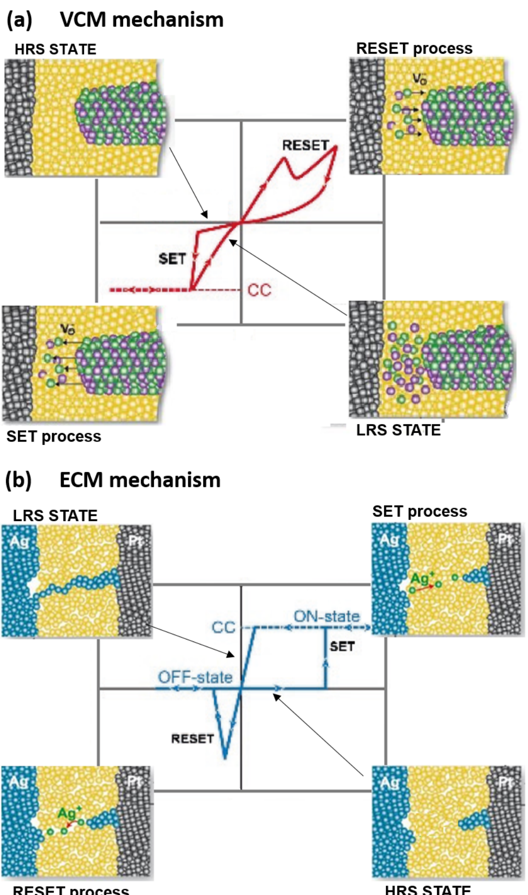


Figure 1.5: Illustration of the switching process for a VCM (a) and an ECM (b) cells; an inspection of the filament evolution in 4 different stages is reported, corresponding to SET and RESET operations, and HRS and LRS states (adapted from [37]).

### Electro-Chemical Memories

In ECM devices, the filament is formed by migration of metallic cations in a solid electrolyte. Therefore is fundamental request of ECM an asymmetric structure, where one of the electrodes consists of an electro-chemically active metal (i.e. Cu, Ag and Ni) and the other is an inert electrode [37, 40, 41]. ECM mechanism is graphically described in Figure 1.5b. During the forming, a positive voltage is applied to the active electrode causing metal atom anodic dissolution and positive ion migration in the insulating layer by effect of the high electric field. When the cations reach the inert electrode, they are reduced and crystallize at the electrode

surface as neutral atoms. A conductive metallic bridge starts to grow from the counter electrode through the active one. When the CF is completely formed, the SET occurs. To reset the device a negative voltage is applied on the active electrode in order to partially dissolve the metallic filament. In ECM, the filament growth and structure are strongly influenced by ion species, ion mobility and redox rate [41]. Valov et al. [42] explained how the transport properties and the chemistry of the involved materials determine the nanobattery effect in ECM cells, influencing the device switching dynamics.

### 1.2.3 Emerging Applications

The main application for memristor devices is the realization of new generation memories, where the memory capability depends on the storage of an internal resistance state. This kind of devices is a part of the big category of *ReRAMs*. The ReRAMs are a promising candidate to overcame the limits of the conventional charge-based memories, fulfilling the requests of high scalability (cell size $\leq$10 nm), sub-nanosecond operational speed and low power consumption ($\leq$0.1 pJ) [43]. Multi-bit capability is another interesting property of memristors. By accurate control of the input voltage stimuli, it has been proved that multilevel retainable resistance states can be achieved. The co-localization of computation and storage in the same devices by multilevel resistance controllability can solve the problem of separation of central programming unit and memory in the actual technologies, allowing the exceeding of the Von Neumann technologies bottleneck. Moreover, ReRAM technologies are CMOS compatible, allowing the integration of crossbar arrays, where each cross point represents a memristor device. Recently for example, Pi et al. [44] reported the fabrication of a crossbar array denser than the 64-layer triple level cell NAND flash (4.5 terabits per inch square). The most reliable devices present an integrated transistor (1T1R technology) in order to internally limit the current compliance, avoiding current overshoot during the voltage SET transient that can cause a fast degradation of the devices [45–47].

Considering the analogue control of resistance by train pulses, memristors can emulate the behavior of synapses in hardware neural networks and neuro-inspired circuits. In our brain, the interaction between neurons are mediated by the axon terminal which is connected via synapses to the dendrites of the following neuron.

Therefore, synapses are dynamical connections between neurons, which can modulate the quantity of information passing in the form of electrical spikes through the activation/inhibition of calcium channels located on the cell membrane. The ability of synapses to strengthen or weaken under voltage stimuli over time is defined as plasticity. The level of information that can pass trough a synapses are quantified by the synaptic weight over time. Two different kind of plasticity are possible and are fundamental for our learning and memory: the short-term plasticity which acts in the range ms↔min and long-term plasticity in the range of hours. Based on long-term potentiation and depression (LTP and LTD) of the synapses, one of the main rules that control the memory/learning process is the so called *spike-time-dependent plasticity* (STDP). According to STDP, the synaptic weight is modified by temporally correlated pre- and post-synaptic spikes; it means that the weight increases when the pre-synaptic spike precedes the post-synaptic spike, while it decreases if the temporal order is reversed. Memristor resistance modulation works as the weight control on biologic synapses and the time in which the state is retained when the power supply is turned off defines the kind of plasticity.

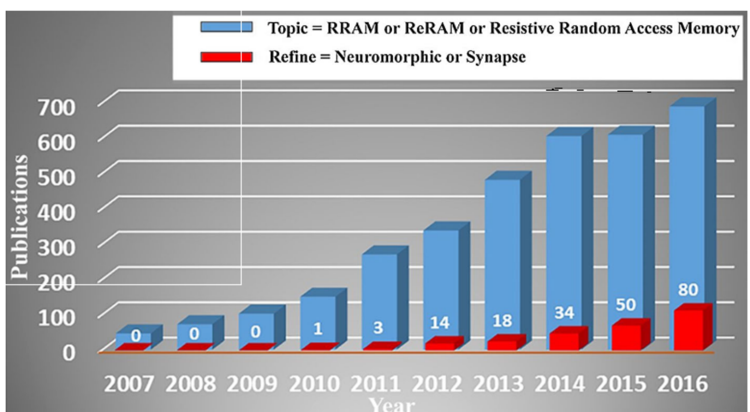


Figure 1.6: Statistic on the publications from 2007 to 2016. The blue bars present the number of publication containing the words "ReRAM" or "Resistive Random Access Memory", while for the red bar the research was refine adding the word "neuromorphic"; graph extracted from [48].

The use of memristors for synaptic applications was proposed for the first time in 2010 by Jo et al. [49], who presented a STDP curve. Since then, a growing interest in memristor-based neural networks, has been reported, as it is visible in the

statistic reported in Figure 1.6 Although the device performance randomicity, the device-to-device variability and the memristor non linear conductance variation are still open issues to be improved, the memristor-based neural networks are nowadays employed for a large number of applications, such as pattern recognition and big amount of data classification [50–52].

### 1.2.4 Performance metrics

The major performance parameters to evaluate a memristive device are: switching parameters (HRS, LRS, $V_{set}$, $V_{reset}$), power consumption (depending on writing current and speed), retention time, endurance, scalability and multilevel storage. Among these parameters, the most interesting in the purpose of our dissertation are described in details.

**Endurance** The endurance is defined as the number of switching cycles that can be performed maintaining a significant resistance ratio, before device break-down [37]. The endurance depends on a variety of factors, such as switching layer and electrode materials [53, 54] , fabrication process [55], device structure, and input stimuli [56]. The performances over cycles can degrade and finally stuck in a failure state, which usually correspond to LRS. The main reason of final breakdown have to be sought in a reorganization and accumulation of oxygen vacancies (or metal ions) that constitute the CF. The carrier distribution non-uniformity can be accentuated by the electric field non-uniformity due to the electrode roughness, as addressed by Lee et al. in [57].

**Retention** The time for which a resistive state is maintained without performing writing operations is defined as retention [37]. Retention higher than 10 years are required in order to build nonvolatile reliable memories. One common extrapolation method for retention is to monitor the resistance evolution at a high temperature and extrapolate the resistance value by a linear fit to the ten-year point [5]. It is important to mention that the retention time depends on the writing speed through the voltage-time dilemma [17, 58].

**Performance uniformity** One of the main problem in ReRAM large-scale production is related to the parameter fluctuations in terms of switching voltages and HRS and LRS states. The parameter variations includes the temporal,

i.e. cycle to cycle (C2C), and spatial, i.e. device to device (D2D), variability. The fluctuations may be determined by the stochastic nature of the oxygen vacancies (metal ions) distribution and by the randomicity of SET/RESET processes [59]. Different techniques have been proposed to reduce the fluctuations, for example Banerjee et al. [33] proposed the CF confinement through surface engineering, while Parck et al. [60] the control of CF size.

**Multi-Resistance Control** Multi-bit operations and synapses-like behaviour are one of the most interesting characteristics of ReRAMs. In different oxides the modulation of the resistance value has been studied, to realize multi-level operations. In particular, is proved that the LRS value can be changed by the $I_{cc}$ control, while the HRS value is controllable by the reset stop voltage [61–64]. To potentiate and depress the devices obtaining gradual resistance variation, different input stimuli have been used, including pulse train with incremental amplitude [65, 66] or identical amplitude [67–70].

In the last five years, metal-oxide ReRAMs revealed high performance parameters, such as large endurance ($10^{10}$ cycles [55]), long retention ($10^5$ s at 200°C [71]), low power consumption (peak voltage of ±1 V and current of 1-20 $\mu$A [72]). The value are referred to $HfO_x$ based memristors, which is one among the most studied materials for ReRAM realization. However, some issues still need to be addressed, such as small HRS/LRS ratio, large C2C and D2D variability, device reliability, controllable multi-level storage, etc. [6].

## 1.3 Atomic Layer Deposition

Resistive switching have been proved for many oxides and most of them are transition metal oxides, such as SiOx, TaOx, HfOx, TiOx, AlOx [5, 6, 9]. In fact, in transition metal oxides the transitional nature of metal ions facilitates the oxidation process and the consequent valence state modification for CF formation. Among the fabrication techniques for metal oxide growth employed in memristor fabrication - including sputtering, chemical vapour deposition (CVD) and pulse laser deposition (PLD) - the atomic layer deposition (ALD) has gained great attention because of its peculiar properties. Morover, different methods have been developed in order to enhance the device performances and to tune memristor electrical response,

including material selection and electrode/oxide interface engineering [32, 33, 73, 74], creation of oxide alloy structures and oxide doping [75–79].

### 1.3.1 Technique Overview

The demand of semiconductor industry for device miniaturization led to development of deposition techniques for thin films down to the nanometer scale and nanostructures. ALD is one of the most interesting technique for its unic properties. The main advantages of ALD are: growth control at sub-nanometer level (up to the single atomic layer), uniformity on large substrates, conformal coating even on high aspect ration structures and low deposition temperature [80–82]. ALD is a self-limiting deposition technique, which takes advantage from the surface chemical reaction on the heated substrate, in particular chemisorption of the precursor molecules. The precursor excess is purged out of the deposition chamber through inert gas flow.

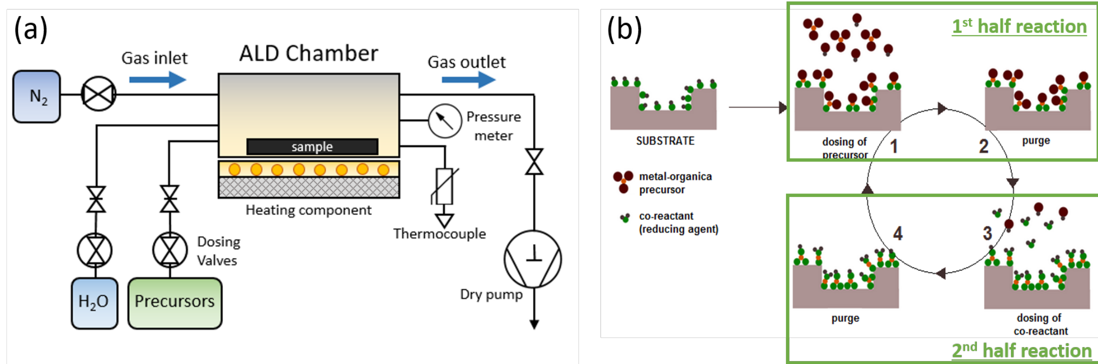


Figure 1.7: (a) ALD reactor illustration; (b) Schematic representation of a typical ALD deposition cycle.

A typical ALD reactor (Figure 1.7a) contains a hot source chamber, which has small dimensions in order to facilitate the operation of pumping and purging. Inside the chamber the precursors are injected in vapour phase carried by the gas flow. A system of valves control the precursor dose and the gas fluxes, which are fundamental parameter for homogeneous deposition. In fact, when the precursor quantity and exposure are sufficient, a saturated growth is obtained and the *growth per cycle* (GPC) reaches its nominal value. Every ALD cycle deposits a sub monolayer of oxide and the quantity of material deposited per cycle is a peculiar property of

the deposited material and precursors. The cycle repetition defines the thickness of the thin film, accordingly to GPC. Concerning the deposition of metal binary oxides, in one cycle two half reactions and four consecutive steps can be identified, as schematically illustrated in Figure 1.7b. During the first half reaction, a metal-organic precursor is introduced in the chamber, which is able to react with the substrate surface through the hydroxyl groups on the surface. The exceeding precursor, which does not react with the substrate, is purged away. Then an oxidizing precursor acting as co-reactant, i.e. $H_2O$ or $O_3$, is inserted to complete the reaction and a single oxide layer is deposited. Finally, a purging step removes the reaction rests and the surplus of precursor. The two half cycles can be described by chemical equations that define the chemical reactions on the surface [37]. Considering a binary material AB from metal precursor $AX_2$ and co-reactant $BY_2$, the equations are:

$$\begin{aligned} &(1) \quad s - Y_{(ads)} + AX_{2\,(vap)} \rightarrow s - AX_{(ads)} + XY_{(gas)} \\ &(2) \quad s - AX_{(ads)} + BY_{2\,(vap)} \rightarrow s - ABY_{(ads)} + XY_{(gas)} \end{aligned} \tag{1.5}$$

where $X$ and $Y$ are the ligands that will be purged and $s$- is the substrate surface. The repetition of process (1) and (2) leads to the creation of an ABABAB... thin film. Is important to remember that 1.5 are valid just for binary compounds, while for more complex ALD processes the number of ligands and surface groups can increase. For a specific process, self-limiting growth, constant GPC and uniformity are achievable only in a specific temperature window, where the correct chemical and physical conditions are established. Out of this temperature values, several processes can disrupt the growth, such as condensation of vapor precursor and low surface reactivity for low temperature, or etching effects, desorption and precursor decomposition for high temperature. As a final remark, one should notice that here just the simplest ALD process has been presented. Additional steps can be added to ALD process, in order to increase the temperature window, control the film cristallinity and change the oxide composition [83]. For example, *super-cycles* are employed to deposit alloy structures, multi-layers and doped oxides.

### 1.3.2 ALD Doping Procedure

Exploiting the extreme control on growth achievable trough ALD, a single monolayer from a different compound can be periodically inserted in a growing oxide, causing physical and chemical modification respect to the pure film. The created localised defects induce a change in the electrical properties of the material, acting as a dopant [75, 76, 84–86]. Therefore, the insertion of periodic monolayer inside an oxide film can be consider as an *ALD doping procedure*.

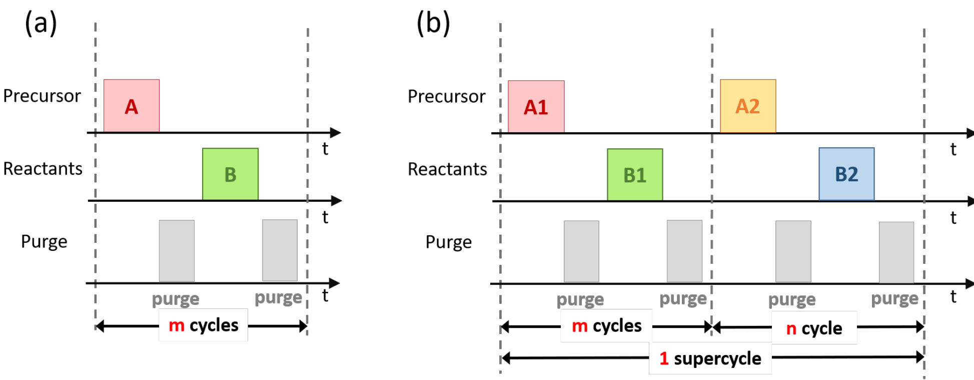


Figure 1.8: (a) ALD deposition scheme, consisting in the repetition of a 2-step cycle; A is the metal precursor and B the co-reactant. (b) Deposition scheme for multi-layer deposition, in which two different metal precursor (A1 and A2) are employed. When n=1 the procedure is defined as ALD doping.

Figure 1.8a,b present a comparison between a standard binary oxide deposition process and the doping procedure. A super-cycle is introduced, where 1 single cycle of the dopant is inserted after a defined number of main oxide cycles. Controlling the periodicity of the insertion different doping levels are obtained.

## 1.4 Dissertation outlook

In this work we investigated the properties of memristors based on $TiO_2$, $Al_2O_3$, ZnO, $HfO_2$ deposited via ALD and their combinations, to enhance the device responses. The effect of the active layer engineering and of the electrode/active layer interface modulation are studied.

**Chapter 2 - Experimental and Methods**

The chapter provides an overview of the experimental research methodology followed in this work. The two adopted fabrication processes are presented, focusing on the process-flow steps, the employed materials and the different deposition techniques. Then the adopted material characterization and electrical testing techniques are listed and explained in details.

**Chapter 3 - $TiO_x$:$Al_2O_y$ devices**

The chapter introduces the concept of ALD doping through the analysis of the $TiO_2/Al_2O_3$ multi-layers and the $TiO_x$:$Al_2O_y$ structures, fabricated by low temperature ALD. The multi-layer structures are studied, in order to define the parameters for a new deposition process, which could optimize the film growth rate and uniformity. Physical and chemical properties of the $Al_2O_3/TiO_2$ multi-layers are inspected through different material characterizations. Finally, Pt/$TiO_x$:$Al_2O_y$/Pt devices are realized and tested in DC voltage sweep, to explore the doping effect on the switching properties of $TiO_2$, with a particular focus on the switching voltage trends, the resistance state variation and the involved conduction mechanism.

**Chapter 4 and 5 - ZnO and $ZnO_x$:$Al_2O_y$ devices**

The composition of these two chapters provide a full insight in the structural, physical and electrical properties of pure and Al-doped (AZO) ZnO thin films deposited via ALD. Chapter 4 and 5 begin with the definition of the ALD growth parameters for pure ZnO and AZO thin films, respectively. Than the material characterizations provide a comprehensive overview on the main properties of ZnO and AZO films, with a particular attention on the dissimilarity produced by doping. In chapter 4 the properties of ZnO-based memristors are inspected, considering the effect of the device engineering and the programming conditions, to find an optimum in switching performances. The result is employed in chapter 5, where the electrical response of Pt/AZO/Cu devices are compared with the one of the pure ZnO samples. The visible improvement in device performances achieved by doping is presented and explained in terms of switching dynamics and conduction mechanism modification through oxide layer engineering.

**Chapter 6 and 7 - $HfO_2$ devices**

The last two chapters include the work accomplished in a one-year period at the École Polytechnique Fédérale de Lausanne (EPFL) in the Microelectronic Systems

Laboratory (LSM) under the supervision of professor Yusuf Leblebici. The electrical performances of $HfO_2$-based devices are inspected, considering different input stimuli, which include DC voltage sweep, AC endurance, train of ramping pulses and train of identical pulses. Two different top electrodes are employed in the dissertation. The TiN electrode (Chapter 6) presets the most robust performances, as it is proved by the statistical analysis on C2C and D2D variability over a large number of devices, while the W main advantage is related to its complex interaction with oxygen. In W-based devices (Chapter 7), the modulation of oxygen exchange at $HfO_2$/W interface, achieved by the insertion of a Ti scavenger and an $Al_2O_3$ barrier layer, allows the control of the filament shape and dynamics. Resistance multi-level modulation has the main focus in these two chapters, in order to realize suitable devices for multi-bit operation architectures and neuro-inspired circuits.

# Chapter 2

# Experimental and Methods

In this chapter, the experimental methodologies for device fabrication processes and characterization are presented. The first section reports the procedures followed for memristor fabrication, including the process flows and the employed materials. The second enumerates the material and electrical characterization tests, providing some details about setups and used instruments. Particular attention is given to the electrical testing setups and the classification of the input stimuli for characterization in DC and pulse mode.

## 2.1 Device fabrication

All the devices presented in the dissertation have a common basic structure, which consists in a metal-insulator-metal trilayer (MIM structure). The two metal layers are defined as bottom and top electrodes respectively (BE and TE), while the oxide is called active layer, since is where the switching process takes place. Additional layers were inserted to improve the device performances or to understand particular properties of the material.

### 2.1.1 Definition of the fabrication processes

Two different processes were developed, as reported in Figure 2.1: the first one is based on the use of a shadow mask to pattern the TEs, the second uses lithographic steps in order to design single cross-point devices. The main difference between the

two processes is the related complexity, in terms of step number and chemical reactions/contamination on the device.

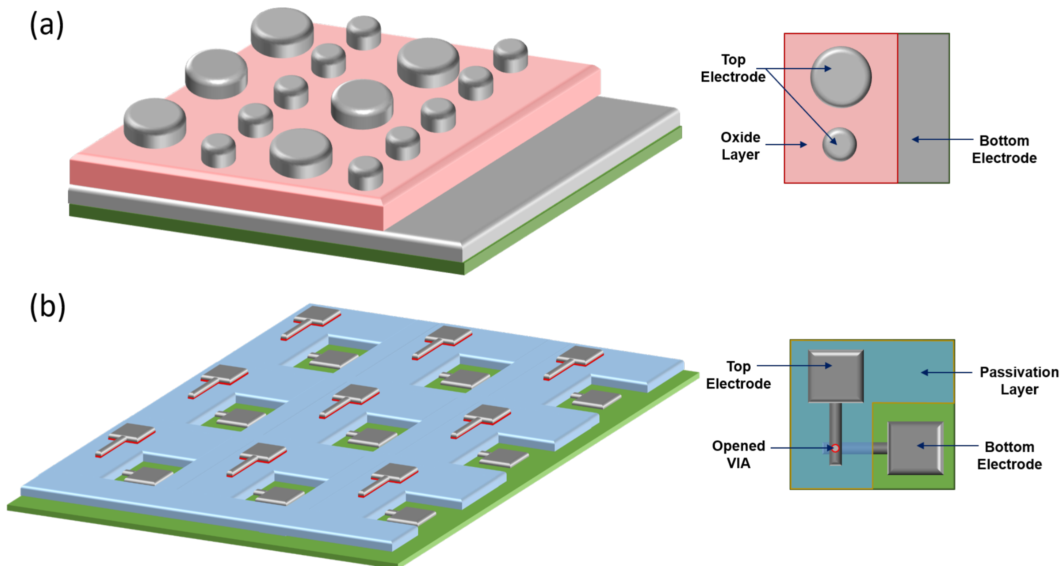


Figure 2.1: Illustration of the developed process for device fabrication: (a) reports the shadow-mask process; (b) reports the single-cell lithographic process.

In the first process (Figure 2.1a), the BE is deposited directly on a Si <100> p-type wafer. Then, the wafer is diced in 1x2 $cm^2$ dies, in order to differentiate the active layer and TE depositions. All the devices on the same die have common BE and active layer, while the TEs are patterned using the shadow mask. Two TE sizes are defined with a radius of 500 $\mu$m and 1 mm, respectively. The reduced number of process steps makes the shadow mask a simple and fast process to preliminary study the memristive properties of different oxides, understanding the role of the used material and the impact of its physical/chemical properties on the CF dynamics and switching kinetics. The process main advantages are: the fast device testing and the lower exposition to external factors (e.g. chemical products in lithography and etching chemistry), which can contaminate the material under study. Large dimensions of electrodes and common BE are the main constraints of shadow mask process. In fact, the size in the order of millimeters contributes to the increase of parasitic capacitance, which leads to an high overshoot in the current transient under voltage stimuli. The effect is a fast decrease in life-time of the devices. Moreover the big dimensions result in higher device to device variability

of electrical performances.

The lithographic process (Figure 2.1b) was developed at *Microelectronic Systems Laboratory* (EPFL, Lausanne), taking advantage of the *CMi* cleanroom facility. It uses conventional lithography and etching steps to define single-cross point devices, with different active areas. $HfO_2$ is selected as the material for the active layer. The choice of $HfO_2$, which is broadly employed in memristor device fabrication, in conjunction with the lithographic process was aimed to study in details the electrical device performances, with particular focus on pulsed systematic measurements and neuromorphic applications. In fact, low overshoot, high device reliability, decrease in device to device (D2D) and cycle to cycle (C2C) variability are the main advantages of this process.

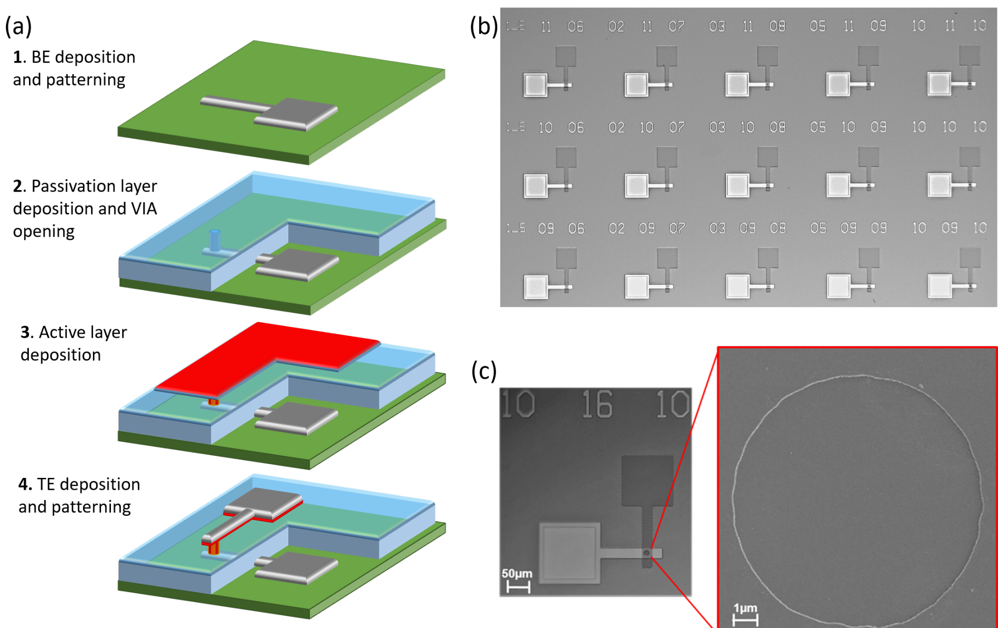


Figure 2.2: (a) list of the main steps for the lithography fabrication process, including: 1.BE deposition and patterning, 2.passivation layer deposition and VIA openind by wet etching, 3.Active layer deposition, 4.TE deposition and patterning by litoghraphic process and RIE; (b) Micrografic image of a portion of die, the number on top indicates: VIA dimension, line and column number, to identify the single device; (C) Zoom on the single device and SEM imaging of the open 10 $\mu$m VIA.

The main steps of the process are schematized in Figure 2.2a; additional details about the fabrication process flow are reported in Appendix A. The steps relative

to the BE and passivation layer depositions and patterning are performed on a 4 inches Si <100> p-doped wafer, which is then diced in 1x1 $cm^2$ dies. The active layer, the TE and the eventual additional layers are deposited on the single die. The BE is deposited on the Si substrate, on which a 500 nm $SiO_2$ film is grown by wet oxidation in order to insulate the devices from the substrate. Then the BE is patterned in single-line electrodes of 20 $\mu$m width, distributed on the die in 20 line x 20 columns, by standard lithographic process and reactive ion etching (RIE). A silicon based passivation layer is grown by low pressure chemical vapor deposition (LPCVD), to reduce the leakage current and define the size of the active areas. In the passivation layer, vertical interconnected accesses (VIA) are opened in correspondence of the cross point of the electrodes. On each die, five different VIA sizes are opened: 1 $\mu$m, 2 $\mu$m, 3 $\mu$m, 5 $\mu$m and 10 $\mu$m by lithographic patterning and buffered hydrofluoric acid (BHF) wet etching. Then, the wafers are covered by a protective resist and diced. The depositions of the active layer and TE are performed consecutively in order to avoid solvent contamination on the exposed oxide, which can modify its chemical composition at the interface. In fact, the oxide-TE interface is the one with the higher impact on the device electrical response. Finally the cross-like structure is defined by a lithographic process similar to the one used for BE. Figure 2.2b,c show micro-graphic images of a portion of the die and a zoom on the single cross-point devices. The extended dimension of the two electrodes fulfills the needing of external contact during electrical measurements.

### 2.1.2 Materials and deposition methods

The Table 2.1 summarizes all the fabricated samples, indicating the employed materials, thicknesses and process type. In particular, $TiO_2$ and ZnO based devices were fabricated by shadow mask process and $HfO_2$ ones by lithography. Technical information about the deposition tools and parameters used for different materials are reported below.

**BE deposition** Pt bottom electrode is deposited by DC sputtering at room temperature in Ar atmosphere. For the shadow mask samples, an adhesion layer of Ta (10 nm) is inserted between Si substrate and Pt. Ta(10 nm)/Pt(200 nm) are deposited in a *Kurt J.Lesker PVD 75* reactor without breaking the vacuum ($10^{-4}$ bar). The employed power are 7.4 $Wcm^{-2}$ for Ta and 5.9 $Wcm^{-2}$

Table 2.1: Summary of the fabricated and tested samples; the table reports the employed materials, the layer thicknesses and the kind of processes for each set of samples. The shadow mask samples were realized at Politecnico di Torino, while the lithography ones at EPFL.

| | | **BE** | **Oxide Layer** | **Buffer** | **TE** | **Process** |
|---|---|---|---|---|---|---|
| S1 | material | Pt | $TiO_2$:$Al_2O_3$ | / | Pt | Shadow mask |
| | thickness (nm) | 100 | 30 | / | 200 | |
| S2 | material | Pt | ZnO | / | Pt / Cu | Shadow mask |
| | thickness (nm) | 100 | 50 | / | 200/100 | |
| S3 | material | Pt | ZnO:$Al_2O_3$ | / | Cu | Shadow mask |
| | thickness (nm) | 100 | 50 | / | 100 | |
| S4 | material | Pt | $HfO_2$ | Ti | TiN | Lithography |
| | thickness (nm) | 125 | 5 | 3 | 56 | |
| S5 | material | Pt | $HfO_2$ | Ti / $Al_2O_3$ | W | Lithography |
| | thickness (nm) | 125 | 30 | 3 | 100 | |

for Pt and the deposition rates are 1.3 Å/s and 4.8 Å/s, respectively. For the lithography process instead, Pt is deposited with a 5 nm Ti adhesion layer in a *SPIDER 600* reactor, using 15 sccm Ar flux and with a measured deposition rate of 4.6 Å/s.

**Active layer deposition** The oxide layers are deposited by ALD, using a *Beneq TFS200* reactor, which is based on a flow-through type reaction chamber, located inside a cold wall vacuum reactor. The metal organic precursors used for the deposition are: Titanium tetrachloride ($TiCl_4$), trimethylaluminum (TMA), diethylzinc (DEZ) and tetrakis(ethylmethylamino)hafnium (TEMAH). For all the process $H_2O$ is used as co-reactant. The chamber temperature is targeted for each process in order to optimize uniformity and deposition rate, while the inert gas fluxes are kept constant to 250 sccm and 600 sccm. Further details on ALD specific processes are reported in the following chapters.

**TE deposition** Cu is deposited by thermal evaporation through a Cu target on

W crucible, using the evaporation current of ∼110 A for a deposition rate of 1-2 Å/s. Pt deposition follows the same procedure described for the BE. TiN is deposited by RF magnetron reactive sputtering in the *DP650* chamber at 200 W. When a Ti 3 nm layer is deposited between $HfO_2$ and TiN, the same tool is used and the vacuum is not broken in order to avoid the thin film contamination in atmosphere.

## 2.2 Device characterization and testing

The link between the physical/chemical properties of the involved materials and the switching behavior under electrical stimuli is essential part of this work. To this purpose, material and electrical characterizations were carried on the device, taking advantages from several different techniques and instruments.

### 2.2.1 Material Characterization

Material characterization has two fundamental roles. First of all, the definition of ALD deposition parameters for new processes and the optimization of the thin film growth, targeting the specifics required for the devices. Secondly, it has been proved that the switching kinetics and the electrical performances of the devices are influenced by the oxide structure [87], stoichiometry [88] and morphology [89]. Therefore, the investigation of the involved materials is crucial to reach a deeper comprehension on the memristive phenomenon.

Morphology, thickness and preliminary composition of the structures are investigated by field-emission scanning electron microscopy (FESEM *Zeiss Merlin*), equipped with an INCA Oxford Energy x-ray spectroscopy detector (EDX) for elemental analysis. Also atomic force microscopy (AFM) is employed to evaluate the surface uniformity and the nano-metric roughness of the thin films deposited by ALD. Finally for the ultra-thin films of $HfO_2$(5 nm)/Ti(3 nm) and $HfO_2$(5 nm)/$Al_2O_3$ (3 nm), where the SEM resolution results not sufficient, a high resolution transmission electron microscopy (HRTEM) imaging is employed, using a *FEI Titan Themis* instrument.
A complete information about layer composition and stoichiometry are achieved by X-ray photo-electron spectroscopy (XPS *PHI 5000 VersaProbe system*), using

a monochromatic Al K$\alpha$ source (energy of 1486.6 eV). The XPS measurements in depth profile utilize an Ar ion gun (2kV) to etch progressively the thin film.
The micro-crystalline structure and crystal orientation are investigated by X-ray diffraction (XRD *Panalytical X'Pert Pro Diffractometer*) and Raman spectroscopy (*Renishaw inVia micro-Raman*). The XRD tool uses a Cu K$\alpha$ radiation ($\lambda$ = 1.54059 Å) and operates in Bragg-Brentano configuration. In the Raman spectrophotometer, the samples are excited with a red laser source ($\lambda$ = 785 nm) with tunable exposure time and number of iterated acquisition. The tool is equipped with a cooled CCD camera.
Concerning the resistivity of the thin film, Hall measurements in Van Der Pauw geometry are realized using an *H500 MRR* controller. The measurements are performed at room temperature in a vacuum chamber at 10 mTorr with a four probe contact. During measurements, a magnet generating a magnetic field of 6500 Gauss is used.

### 2.2.2 Electrical Characterization

I–V electrical measurements are performed using a two-point contact probe station at room temperature, with grounded BE and biased TE. In this configuration, DC measurements in voltage sweep mode and pulsed measurements are carried out. Two different parameter analyzer are employed: the *Keithley 4200* semiconductor characterization system at Politecnico di Torino and the *Keysight B1500* semiconductor device analyzer at the EPFL.

The main purposes of DC characterization is the first study of the memristive properties of the devices. The impact of materials (structure, morphology and chemistry) and programming conditions on the device electrical response is tested through DC measurements. The DC test setup is schematized in Figure 2.3a. For both the instruments, triaxial cables are used to connect the source measure units (SMU) of the parameter analyzer to the probes to reduce the parasitic capacitance and have good resolution on the low-current measurements. Current compliance limitation is provided by the internal tool of the parameter analyzers.

Pulse measurements are used to test the performances in terms of writing speed, endurance, dependence on pulse parameters and synaptic behavior. The pulse

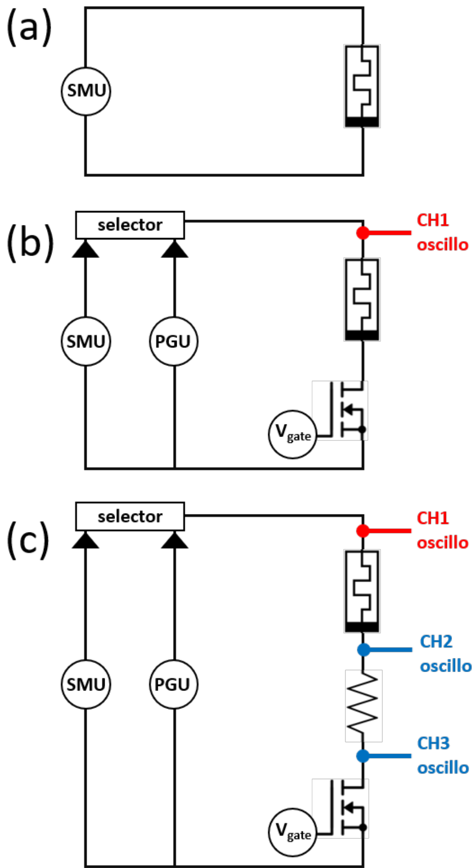


Figure 2.3: (a) Schematic of the setup used for DC measurements for both *Keithley 4200* and *Keysight B1500*. The tests are controlled by the software *KITE* and *EasyEXPERT*, respectively; (b)-(c) Schematic of the AC measurement setup; the tests are controlled by a custom Python code.

setup, shown in Figure 2.3b, represents the configuration of *Keysight B1500* device. The two evident differences from the DC setup consist in the addition of a selector and a transistor (nMOSFET - IRLB8721PbF). The selector box is added to switch fast between the SMU module and the high-voltage semiconductor pulse generator unit (SPGU). The transistor role is to provide an external current limitation, whose threshold is tunable by $V_{gate}$ control. This is fundamental to obtain reliable measurements, because the feedback of parameter analyzer internal tool for $I_{cc}$ limitation is quite slow in forcing the compliance limit ($\sim 50 - 100\,\mu$s), resulting in no current limitation for faster pulses. Gate, source and drain of the transistor

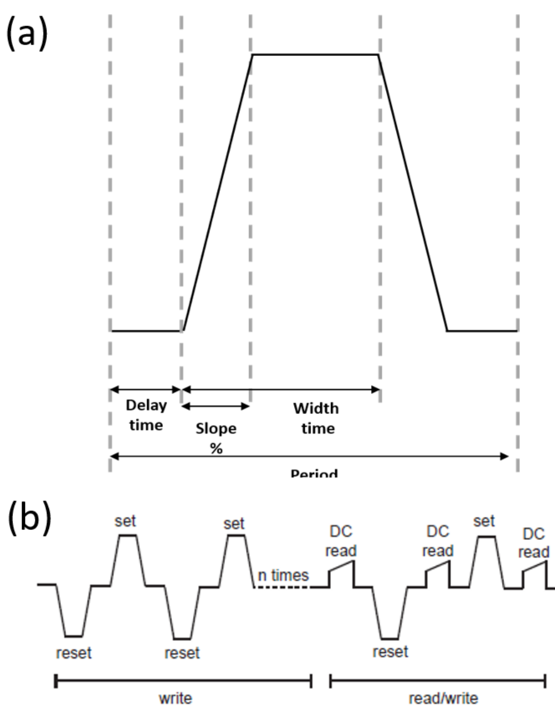


Figure 2.4: (a) Parameters controllable by users during the pulse setting; (b) Writing/reading scheme for pulse measurement (taken from [90]).

are controlled by different SMUs. In positive polarity (SET) the current modulation is controlled by $V_{gate}$ and $V_{source}$ is connected to ground, while in negative polarity (RESET) the transistor is ignored, forcing $V_{drain}$ node to ground, since the RESET operations do not require a strict $I_{cc}$ control. This avoids the transistor operations in reverse polarity, where it acts as a diode with a fixed voltage drop of 0.6 V. The AC setup solves the limits in $I_{cc}$ current overshoot through the external transistor, but the parasitic capacitance of connection cables determines a limit in the minimum pulse width. For pulse faster than 100 ns a progressive distortion of the pulse shape and eight is notable. In order to measure the current during pulses in *Keysight B1500*, the setup presented in Figure 2.3c is used. The current is evaluated measuring the voltage drop across a series resistance through the oscilloscope. The resistance value is selected carefully for each device to avoid any interference with the SET process and to reduce the measurement noise at the same time. In particular, the selected values for the series resistance are:

- 1 kΩ for the $Pt/HfO_2/Ti/TiN$, $Pt/HfO_2/W$, $Pt/HfO_2/Ti/W$ devices
- 150 Ω for the $Pt/HfO_2Al_2O_3/W$ device

Different testing routines were created using Python code for the AC measurements, taking advantage from the previously developed Python instrument/computer interface through GPIB communication and basic tests. During the endurance pulse measurements, the writing is performed by pulses in both the polarity with controllable period, voltage amplitude, width and slope of the voltage transient(Figure 2.4a). Rise and fall time are symmetric and are defined as the transient between 10% and 90% of the maximum voltage amplitude, while the pulse width is composed by signal ramp and voltage plateau. The range of value for the pulse width is (1 ms - 100 ns) and in this range the slope value is varied from 10% to 80%. A read operation is carried out with user-defined periodicity, in order to determine the resistance value before consecutive writing, as presented in Figure 2.4b. The read operation consists in the resistance evaluation as the mean of 50 $V_{forced}/I_{measured}$ values obtained on a DC ramp between 200 mV and 250 mV. Pulse train measurements for neuromorphic computing follow a scheme similar to the endurance one: a train of consecutive pulses with fixed or growing voltage amplitude is performed and the periodicity of reading can be controlled.

# Chapter 3

# $TiO_x$:$Al_2O_y$ Based Memristors

**Reference paper**: *Effects of single-pulse* $Al_2O_3$ *insertion in* $TiO_2$ *oxide memristors by low temperature ALD* [91]

In this chapter, the concept of ALD doping at low temperature is introduced and applied in the $TiO_x$:$Al_2O_y$ memristor realization, in order to tune the switching properties of $TiO_2$ devices through insertion of $Al_2O_3$ partial layers. Siles et al.[76] firstly inspected the $TiO_2$ ALD doping procedure for the purpose of tuning the resistive switching response of $TiO_2$-based memristors, opening the way to further investigations. Two series of samples were prepared. The first series includes the multi-layer structures used to optimize the ALD growth parameters and to study the structure and chemical composition of $TiO_2$-$Al_2O_3$ mixed compounds, essential for the doping procedure implementation. The second series of samples includes the $Al_2O_3$-doped devices for electrical characterization, which consist in MIM structures with two Pt symmetric electrodes and an $Al_2O_3$-doped $TiO_2$ oxide layer. Different doping concentrations are obtained by changing the periodicity of TMA-$H_2O$ single cycle insertion in the $TiO_2$ matrix. The multi-layer samples are extensively analyzed in the first section of the chapter, with a particular focus on the optimization of the ALD doping process. While, in the second section, the electrical properties of Pt/$TiO_x$:$Al_2O_y$/Pt structures are presented, focusing on the variation of switching voltages and resistance states.

## 3.1 $Al_2O_3$ doping via ALD

### 3.1.1 Process definition

The two sample sets are deposited at 100 C°, using $TiCl_4$ and TMA as metal precursors and water as reactant. For the $TiO_2$ cycles, the pulse duration for $TiCl_4$ and $H_2O$ are set to 400 ms, while for TMA the pulse duration is 150 ms. The deposition schemes utilized for multi-layers and doped samples are reported in Figure 3.1a. All the films are deposited on a <100> Si wafer substrate coated by sputtered Pt(100 nm). Figure 3.1b depicts a multi-layer from the first series of samples, which is composed of a repetition of $TiO_2$ and $Al_2O_3$ layers of equivalent thickness. Varying the thickness of each single layer from 2.5 nm to 20 nm, four different typologies of samples were realized. Regarding the second series of sample, a representative sketch is presented in Figure 3.1c. The fabrication process follows the ALD doping procedure of the super-cycle (Section 1.3.2), which consists of a single TMA/$H_2O$ cycle deposited after n $TiCl_4$/$H_2O$ cycles. The doping concentration is defined by the periodicity of the $Al_2O_3$ cycle in the film, targeted by the n number of $TiO_2$ cycles in a super-cycle.

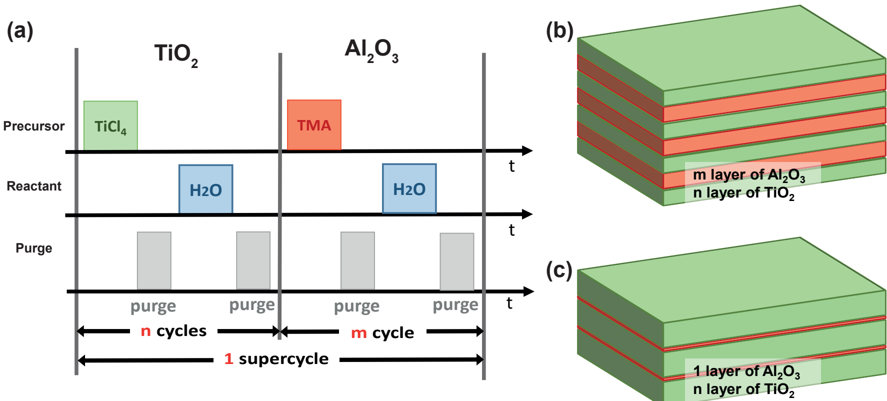


Figure 3.1: (a) Diagram of the deposition process used for the realization of multi-layers and doped samples. For the doping procedure the m number of TMA cycles is set to 1, while the n number of $TCl_4$ cycles defines the doping concentration; (b) Illustration of the multi-layer structures used for chemical and physical characterization (first series of samples); (c) Illustration of the ALD doped structures used for electrical characterization (second series of samples). Figure from [91].

### 3.1.2 Optimization of the growth parameters

The calibration of deposition parameters and the study of the mixed compounds is performed, considering the dissimilarity in structure and surface reactivity of the two oxides. The multi-layer structures used in this section are summarized in Table 3.1. Considering that $TiO_2$ and $Al_2O_3$ present the significantly different GPC of 0.7 Å/cycle [92] and 1.2 Å/cycle [93] respectively, the number of cycles for each layer in the multi-structure is targeted in order to obtain the same thickness for the two oxides (as it is visible in the column *Recipe* of Table 3.1).

Table 3.1: $Al_2O_3$ - $TiO_2$ multi-layer structures. Last column of the table presents the recipes used for the ALD process; total thickness and single-layer thickness are reported in nm.

| **Sample** | **Total Thick.** | **Layer Thick.** | **Layer Number** | **Recipe** |
|---|---|---|---|---|
| ML1 | 52.5 | 2.5 | 21 | (36 TiCl4 cycles + 21 TMA cycles)x10 + 36 TiCl4 cycles |
| ML2 | 55 | 5 | 11 | (71 TiCl4 cycles + 42 TMA cycles)x5 + 71 TiCl4 cycles |
| ML3 | 70 | 10 | 7 | (143 TiCl4 cycles + 83 TMA cycles)x3 + 143 TiCl4 cycles |
| ML4 | 60 | 20 | 3 | 214 TiCl4 cycles + 125 TMA cycles + 214 TiCl4 cycles |

Regarding the deposition of hetero-layers, the difference in nature and number of the reactive sites on the $Al_2O_3$ and $TiO_2$ surfaces might cause a change in the adhesion and early stage growth of the single layers. Several works [94, 95] have studied the interaction of $Al_2O_3$ and $TiO_2$, reporting a strong affinity in the formation of Ti-O-Al bonds. However the stable alloy $Al_2TiO_5$ is created just in the temperature range of 1000°C - 1450°C [96]. Once the first $TiO_2$ layer is deposited, the ions movement and chemisorption in the first-half cycle of the TMA process is favorable in the direction perpendicular to the horizontal plane, where the surface active sites operate as diffusion paths for the $Al^{3+}$ ions. The same process happens when the following $TiO_2$ layer starts growing on the $Al_2O_3$. Therefore, at the $TiO_2$-$Al_2O_3$ interface, a homogeneous distribution of the two species and

a negligible variation of the growth rate are expected. In order to quantify this variation, the comparison between expected and measured thickness is performed by SEM imaging in cross section (Figure 3.2). To this purpose, an *average GPC* (aGPC) is defined as ratio of the thin film thickness and the total number of cycles:

$$aGPC_{expected} = \frac{thickness}{total \ \#_{cycles}} \qquad aGPC_{measured} = \frac{thickness_{measured}}{total \ \#_{cycles}} \tag{3.1}$$

The difference between the expected aGPC and the measured one results in a small decrease of the growth rate of ∼0.1 Å/cycle, which is taken into account for the realization of the sample for the electrical characterization in order to obtain the desired thickness.

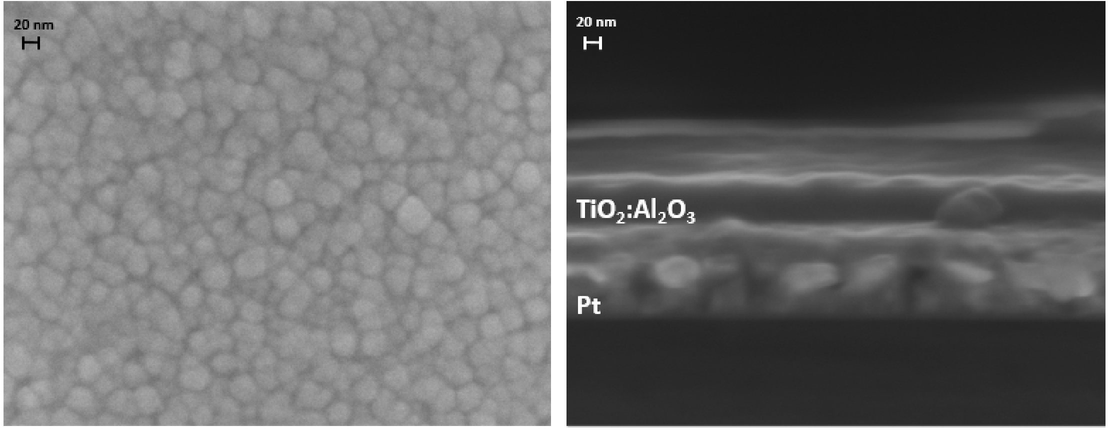


Figure 3.2: FESEM images in top view (a) and cross section (b) of sample ML4. From the cross section image, an evaluation of the film thickness was performed. The expected aGPC was 0.82 Å/cycle, while the measured aGPC, given by the ratio between the total number of cycles (739) and the measured thickness ((53±2)nm) is (0.71±0.02) Å/cycle.

Concerning the definition of each single layer and the diffusion of the metallic ions in the adjacent layers, the low thermal budget produced by the deposition at 100 C° avoids the diffusion of $Ti^{4+}$ and $Al^{3+}$ ions. To investigate this hypothesis, XPS measurements in depth profile are carried on. The depth profiles for ML4 and ML3 are reported in Figure 3.3a. From the left panel of Figure 3.3a, an evaluation of the film stoichiometry is elaborated and the O:Ti and O:Al relative quantities are evaluated for each layer, reveling the expected values of 2.1±0.4 for $TiO_2$ and 1.4±0.1 for $Al_2O_3$. In the right spectrum of Figure 3.3a, a relative mismatch in the

two oxide is visible, which could be due to a limit in the instrument resolution for ultra thin films. During the depth profiling sputtering, the residual removed species may precipitate again on the sample surface and be detected by the instrument. However, the different consecutive layer can still be distinguished. The presence of distinguishable $TiO_2$ and $Al_2O_3$ layers implies a minimum penetration of one species into the other. These is particularly interesting, because it confirms that during the doping procedure, the single $Al_2O_3$ layer does not diffuse in the $TiO_2$, creating a localized barrier inside the oxide film.

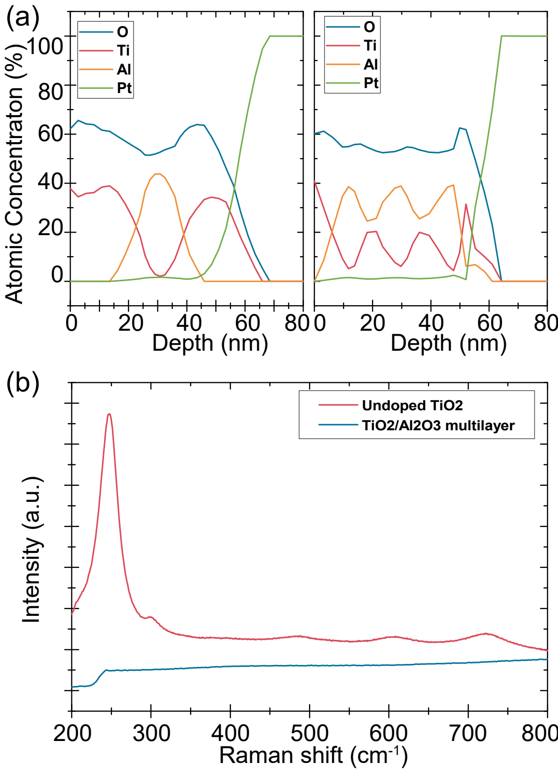


Figure 3.3: (a) XPS measurements in depth profile for two different multilayer structures: the left spectrum is referred to ML4, while the right one to ML3; (b) Raman spectra for a pure $TiO_2$ and one representative multi-layer sample (all the doped samples presented similar spectra) [91].

The change in structure and crystal contents of the multy-layers in comparison with the pure $TiO_2$ is investigated by Raman spectroscopy. The Pt layer deposited under the oxides avoids the presence of Si contribution in the Raman spectra. As it is visible in Figure 3.3b, the pure $TiO_2$ via ALD is poly-crystalline in the anatase phase also at a low deposition temperature, while the multi-layers are all

amorphous. This means that the micro-crystal nucleation starts roughly after the 20 nm of $TiO_2$ thickness. Since in the doping procedure the thickness of the n consecutive $TiO_2$ layers never reaches 20 nm due to the presence of periodically inserted $Al_2O_3$ single layers, the active layer of $TiO_x$:$Al_2O_y$ memristors can be considered amorphous.

## 3.2 Electrical properties of $TiO_x$:$Al_2O_y$

### 3.2.1 Samples for electrical characterization

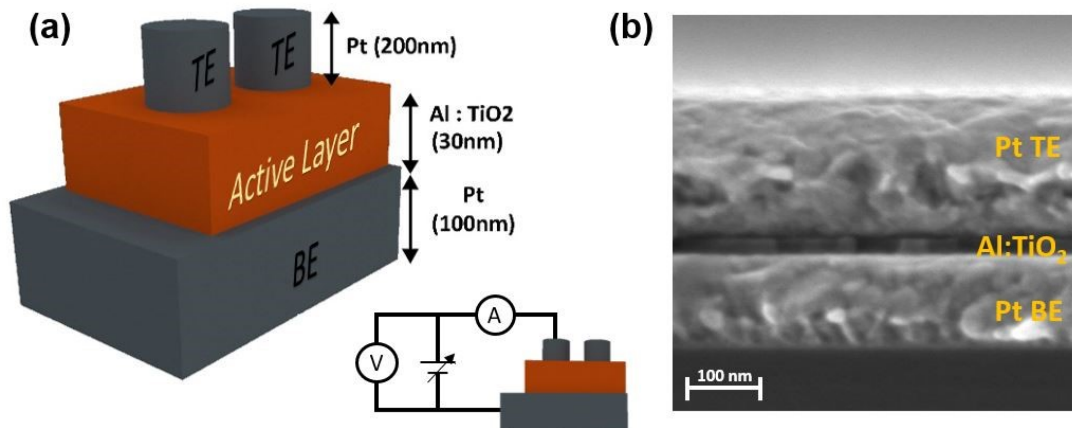


Figure 3.4: (a) Scheme of the devices fabricated for electrical characterization; (b) SEM image in cross section of the structure of the devices. Figure from [91].

In order to investigate the switching properties of the $Al_2O_3$-doped $TiO_2$ devices, Pt(100 nm)/$TiO_x$:$Al_2O_y$(30 nm)/Pt(200 nm) structures are fabricated by shadow mask process (description of the process is available in Section 2.1) and tested in DC voltage sweep. Figure 3.4 reports a schematic representation of the samples and a SEM image in cross section, displaying the device structure. The low-temperature deposition and the doping guarantee an amorphous oxide layer, which allows a better reproducibility of the device fabrication and increases the content of impurity in the layer. The abundance of defects facilitates the vacancies-based CF formation, decreasing the forming voltage [83, 97]. Four sets of devices are fabricated varying

the $Al_2O_3$ number of layers inside the $TiO_2$ film, as reported in Table 3.2. The $Al_2O_3$ content is reported in the table in two different way: (i) *Layer Doping Percentage* (LDP) which considers the number of TMA cycles over the total number of cycles for the process, (ii) *Thickness Doping Percentage* (TDP) which takes in account the different GPC. LDP gives an idea of the number of $Al_2O_3$ partial layers in the film and is the one considered in the following analyses.

Table 3.2: $TiO_x$:$Al_2O_y$ doped structures used for electrical characterization. The number of super-cycles for the oxide deposition is targeted to obtain a thickness of 30 nm. *Layer Doping Percentage* (LDP) and *Thickness Doping Percentage* (TDP) for $Al_2O_3$ in $TiO_2$ are reported.

| **Sample** | **LDP** (%) | **TDP** (%) | **Recipe** |
|---|---|---|---|
| Undoped | 0 | 0 | 375 cycles of TiCl4 |
| Doped5 | 5 | 8 | (19 cycles of TiCl4 + 1 cycle of TMA) x 22 |
| Doped10 | 10 | 16 | (9 cycles of TiCl4 + 1 cycle of TMA) x 43 |
| Doped20 | 20 | 30 | (4 cycles of TiCl4 + 1 cycle of TMA) x 75 |

### 3.2.2 I-V characteristic and doping effect

The mechanism involved in the switching behaviour of Pt/$TiO_x$:$Al_2O_y$/Pt devices is the VCM (Section 1.2.2), associated to the formation of a conductive filament of Vö through oxygen ion migration and redox reactions at the electrode/oxide interface. Since the mobility of oxygen ions is conditioned by the presence of defects induced by ALD doping inside the active layer, the insertion of $Al_2O_3$ plays a crucial role in the switching behavior of devices. The bipolar I-V characteristics are obtained applying a DC voltage ramp, limiting the $I_{cc}$ during forming and SET operations in negative polarity. The alteration of oxide composition and structure requires different testing condition to allow a stable switching. The compliance value must be changed accordingly to $Al_2O_3$ concentration inside the active layer: $I_{cc}$ starts from 0.8 mA for the undoped to 80 mA for the 20% doped samples. A forming step is required in order to firstly build the conductive filament. Pt/$TiO_x$:$Al_2O_y$/Pt devices exhibit the best response to negative forming at low voltage (1 V for the Undoped, Doped5 and Doped10 samples and -1.3 V for the

Doped20), which defines the switching polarity of SET and RESET operations. Figure 3.4 reports the I-V characteristics of a representative device for each of the four sets of samples reported in Table 3.2. All the samples show a counter-eightwise switching, with the SET process in the negative and RESET process in the positive voltage polarity. The insets of Figure 3.4 report the HRS and LRS values for ten indicative cycles.

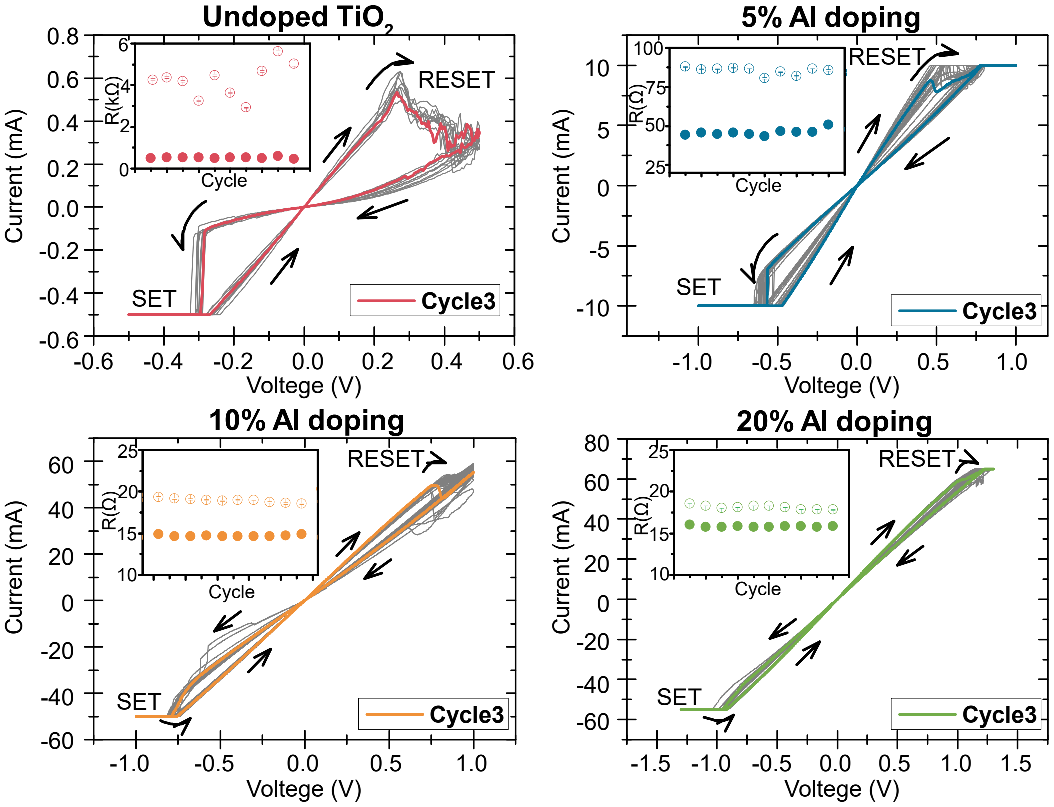


Figure 3.5: I-V characteristics for the four undoped, 5% doped, 10% doped and 20%doped devices. One representative cycle is underlined for each stuck, while the other cycles are reported in grey. The four insets show HRS and LRS value for ten consecutive cycles. Adapted from [91].

Comparing the I-V curves, one can notice easily the variation in electrical response as an effect of the ALD doping procedure. The main effects of the increase in $Al_2O_3$ concentration inside the active layer are: an increase of the $V_{set}$ and $V_{reset}$ values, a reduction of the two resistance states, particularly evident in HRS decrease, and a stabilization of the HRS value over cycles.

In order to explain the changes in electrical response, it is fundamental to provide an insight into the variation of the CF dynamics during SET and RESET procedures under the oxide layer modification by the insertion of $Al_2O_3$ partial layers. The ALD doping procedure defines the insertion of periodically distributed $Al_2O_3$ barrier layers, increasing the number of localized trap states and defects in the oxide. The $O^{2-}$ migration under the applied voltage is altered by the presence of these local traps and the ion mobility is remarkably reduced [75]. In fact, only a part of the mobile charges injected in the oxide contributes to the formation of the conductive filament, while the remaining part fills empty trap states. This defines an increase in the energy required for filament formation-rupture and a consequent variation of $V_{set}$ and $V_{reset}$ absolute values. In particular, $V_{set}$ changes from -0.30 V for the Undoped sample, to -0.60 V for the Doped5, -0.80 V for the Doped10 and -0.95 V for the Doped20, while $V_{reset}$ increases from 0.20 V for the Undoped sample, to 0.22 V for the Doped5, 1.00 V for the Doped10 and 1.18 V for the Doped20. A quadratic dependence of switching voltages as a function of $Al_2O_3$ LDP has been observed, as reported in Figure 3.6a.
Considering the effect of the trap states on the charge injected by the electrodes

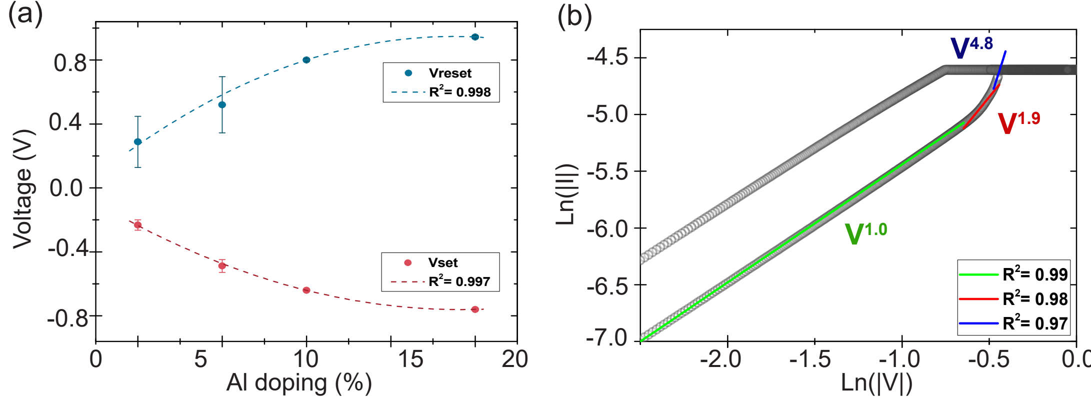


Figure 3.6: (a) Switching voltages ($V_{set}$ and $V_{reset}$) depending on the $Al_2O_3$ doping concentration. The dashed lines represent the two quadratic trend, which are used to fit the data. The fit goodness is evaluated through the determination coefficients ($R^2$), reported in the graph; (b) Representative I-V characteristic in $\ln(|V|) - \ln(|I|)$ scale for the 5% doped sample; the SCLC transport mechanism is confirmed by the three distinguishable regimes: ohmic (green fit), trap unfilled (red) and trap filled (blue). Figure from [91].

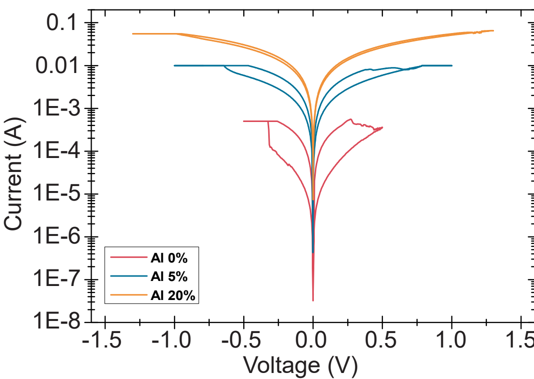


Figure 3.7: I-V characteristics in logarithmic scale for different doped samples. The increase in current compliance limitation is visible. Figure from [91].

under bias, space-charge-limited conduction (SCLC) can be considered as the dominant transport mechanism in the switching kinetics of Pt/$TiO_x$:$Al_2O_y$/Pt devices. The linear fit of the I-V curves in ln(|V|)-ln(|I|) scale confirms this hypothesis (Figure 3.6b), revealing a good accordance with the SCLC, which is described by the equation:

$$J_{SCLC} = \frac{9}{8}\,\epsilon_i \mu \theta\,\frac{V^2}{d^3} \tag{3.2}$$

Where $\epsilon_i$ is the oxide permittivity, $\mu$ the carrier mobility, $\theta$ the ratio of free and trapped charges and $d$ is the insulator thickness [36, 98]. From Figure 3.6b, the three different regimes typical of SCLC are visible: the ohmic region for low applied voltage ($I \propto V^1$), the tap unfilled region ($I \propto V^2$) and the trap-filled region($I \propto V^5$). The second region starts when the injected charges become dominant and start to fill the trap states, until the threshold voltage is reached. The filament is completely formed and an abrupt current change is observed (third region). The increase of localized barrier states due to $Al_2O_3$ partial layers requires a higher threshold voltage to pass from unfilled to trap-filled regions, as it is confirmed by $V_{set}$ and $V_{rest}$ quadratic increase in absolute value.
Although the $Al_2O_3$ barriers and the ion mobility reductions impose an increase of the $I_{cc}$ limit in order to stabilize the formed CF, as it is visible in Figure 3.7, this $I_{cc}$ variation might play a role in the resistance state variation. In particular for VCM, the LRS decrease dependency on $I_{cc}$ limit is well known [12], while the HRS value is just slightly influenced by this factor. The HRS drastic decrease, from $\sim 5\,\mathrm{k}\Omega$

in the Undoped sample to less than $100\,\Omega$ in the Doped20, has to be attributed to the rather high doping values, which are used in this work to understand and investigate the change in switching dynamics caused by ALD doping. But one should mention that doping concentrations typically used in semiconductors are generally at least one order of magnitude lower than the values employed here. The HRS reduction is explained by the increase of free-carrier density, which is related to the creation of defects by non-stoichiometric phases at the $TiO_2/Al_2O_3$ interfaces, and the formation of a stable $Al_2TiO_5$ compound, when the temperature increase caused by switching is sufficiently high. Concerning the $Al_2TiO_5$ stable compound, the thermal budget in the $TiO_2$ is sufficient for the structural recombination, if we consider that temperatures higher than 1000°C have been reported in simulations [11] during the RESET operation. In fact, when the CF is formed, the current passing through the filament determines a increase of the internal temperature by Joule heating. The lower electron affinity of $Al_2TiO_5$ compared with the pure $TiO_2$ [99, 100] determines the increase of mobile carrier in the oxide. Finally, it is important to remember that $Al_2O_3$ and Al-Ti-O compounds act as oxygen diffusion blocking barriers, limiting the filament re-oxidation. This explains the reduced variability of HRS for the doped samples.

The study of the electrical response of the Pt/$TiO_x$:$Al_2O_y$/Pt devices here presented demonstrates that $TiO_2$ oxide memristors can be tuned by $Al_2O_3$ doping via ALD. A fine regulation of switching voltages and resistance state values adds a degree of freedom in the memristor performance modulation through the combination of different binary oxides by ALD doping, producing devices with highly defined and tunable electrical properties and improved stability.

# Chapter 4

# ZnO Based Memristors

Zinc oxide is a semiconductor, with a wide direct band-gap of ~3.3 eV, in which the native n-type doping arises from the large amount of defects, in particular oxygen vacancies and Zn interstitial, created during the deposition. Among numerous metal oxides, ZnO presents interesting properties, such as high electron mobility, controllable electrical response, chemical stability, electro-chemical reactivity, good transparency, and bio-compatibility [101, 102]. Moreover, ZnO growth can be controlled in order to obtain different structures (e.g. nanowires, nanotubes and nanorings), taking advantages from several fabrication techniques [103, 104]. ALD allows the deposition of conformal, stoichiometric ZnO at low temperature, which usually shows a poly-crystalline structure[105].
In this chapter ZnO deposition through ALD is investigated in order to define the optimum growth parameters and determine the typical GPC. The characterizations of the deposited material in terms of morphology, structure, chemical composition and stoichiometry are presented in Section 1. The second section of the chapter is dedicated to study the electrical behavior of ZnO and the resistive switching properties of the material in response to DC voltage ramps and AC pulsed measurements.

## 4.1 ZnO deposition via ALD

### 4.1.1 Process definition

One of the most commonly used precursors for ZnO deposition via ALD is the dietil zinc (DEZ), thanks to its chemical properties and in particular the high reactivity with $H_2O$. The two equations describe the reactions that take place in the two half processes of the ALD cycle (deposition scheme is presented in Section 1.3):

$$\begin{aligned} &OH^{\bullet} + Zn(CH_2CH_3)_2 \rightarrow OZn(CH_2CH_3)^{\bullet} + C_2H_6 \\ &OZn(CH_2CH_3)^{\bullet} + H_2O \rightarrow OZnOH^{\bullet} + C_2H_6 \end{aligned} \tag{4.1}$$

where the $OH$ groups on the substrate surface act as the starting point for the first-half reaction. The deposition temperature window and the pulse doses for the precursors were investigated in order to properly control the thin film growth and properties. These two parameters play a crucial role in the film uniformity and conformability, defining a region of values in which the growth nearly reaches the ideal ALD behavior. Figure 4.1 reports an example of growth alterations respect to the nominal self-limiting ALD deposition (Figure 4.1a,b) due to a temperature out from the window (Figure 4.1c,d) and a wrong DEZ precursor dose (Figure 4.1e,f). The high temperature results in an island-growth, as it is visible from the SEM images in Figure 4.1c, and a consequent increase in the film roughness and decrease of the film uniformity. The vaporized metal precursor can be partially decomposed by the high thermal energy, introducing additional CVD components that act as nucleation centers for the islands. On the other side, the main effect of low temperature is the reduction of the surface reactivity. A not complete coverage of the substrate and a significant reduction of the GPC were observed for temperature lower than 70°C. Concerning the pulse dosing, the saturation of DEZ inside the deposition chamber induces the partial condensation of precursor on the surface, preventing the effective purging of the chamber, while a compact and uniform deposition is not guaranteed if the precursor is insufficient (Figure 4.1e,f).
Two different set of sample were deposited to find the best growth conditions. In the first, DEZ pulse duration decreases from 0.5 s to 0.2 s, keeping constant the $H_2O$ pulse duration of 0.5 s, the purging times of 2 s and the number of cycles of

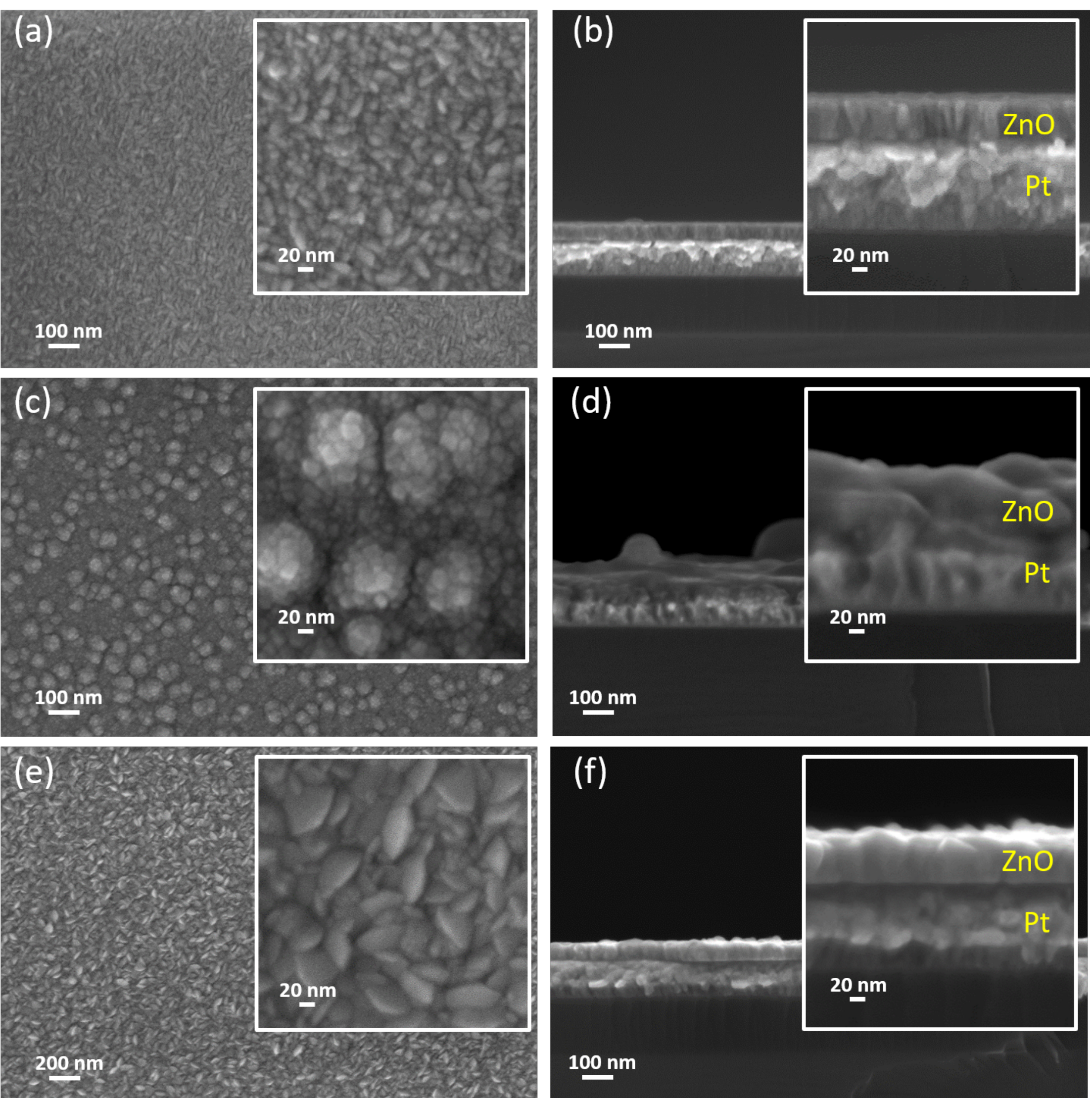


Figure 4.1: SEM images in top view and cross section for: nominal ZnO growth via ALD (a,b), in which the recipe consists in: $DEZ_{pulse}$=0.2 s, $H_2O_{pulse}$=0.5 s, Ar purging=2 s; island-growth of ZnO for a temperature of 250°C, out of the temperature window (c,d); irregular growth and not compact coverage of ZnO for a DEZ concentration higher than the needed one (e,f).

250. The second set consists in depositions at different temperatures from 100 to 250°C; also in this case the number of cycles is kept constant at 250. In Figure 4.2 the film thickness depending on deposition temperature and DEZ pulse duration is reported. The GPC (in red) is evaluated for the different conditions, revealing

a slight dependence from temperature inside the window of 70-200°C, and a high variability outside (measure at 250°C). The small decrease of GPC at low temperature can be explained by the lower decomposition rate of $H^+$ ions from $H_2O$ molecules [106]. The best ZnO growth recipe was found to have a pulse duration of 0.2 s and 0.5 s for DEZ and $H_2O$ under a 250 sccm Ar flux, a purging time of 2 s for both the half-cycles, carried on in a vacuum chamber at 7 mbar (a typical ALD recipe is reported in Appendix B). In this condition the GPC is 2.2 Å/cycle.

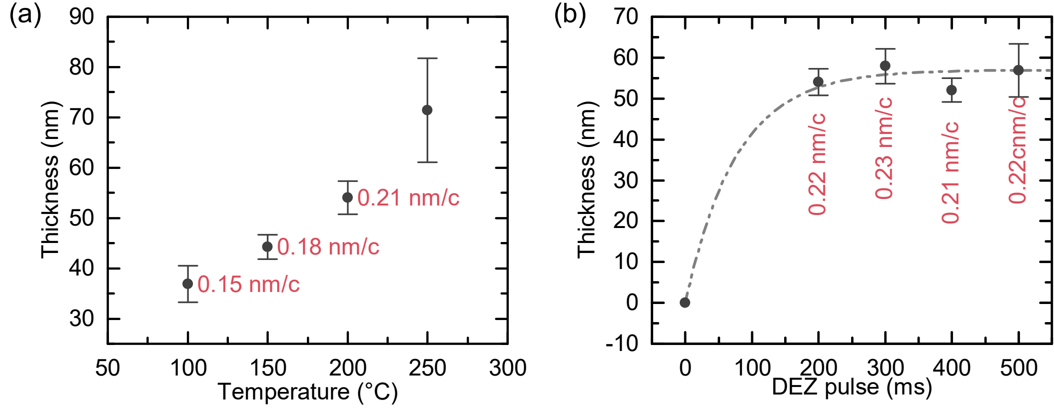


Figure 4.2: ALD Film thickness depending on the deposition temperature (a) and DEZ pulse duration (b); each point of the graphs and relative errors are the mean value and mean standard deviation on 30 repeated measurements, 10 in the center and 20 at the two edges of the sample)

### 4.1.2 Material properties

ZnO thin films deposited via ALD are typically poly-crystalline even for low temperature deposition (100°C) and amorphous structures are obtained only in particular conditions such as very thin films and specific substrates. ZnO belongs to the group of hexagonal wurtzite, with 6 mm symmetry in the space group $C_{6v}(P6_3mc)$ [107, 108]. In particular, regarding ZnO via ALD, three main factors influence the nano-crystal size and orientation, which are the deposition temperature, the film thickness and the substrate orientation. The substrate used in this study are $Si/SiO_2/Ta(10\,nm)/Pt(100\,nm)$, in order to grow films comparable with the ones used for the electrical characterization, while temperature and thickness can be modulated to obtain different poly-crystal structures.

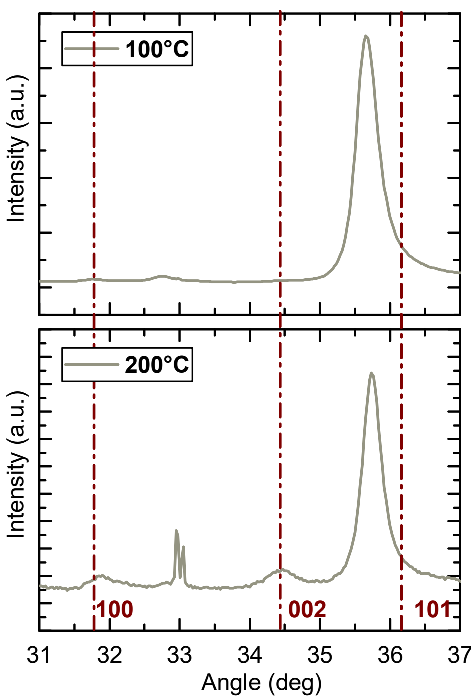


Figure 4.3: XRD patterns for 50 nm ZnO deposited at 100°C (a) and 200°C (b) on a $Si/SiO_2/Ta(10\,nm)/Pt(100\,nm)$ substrate. In (a) graph the direction $< 101 >$ is predominant with the peak at (35.72±0.01)°, while in (b) three different peaks are present, placed at (31.93±0.01)° ($< 100 >$), (34.44±0.01)° ($< 002 >$) and (35.77±0.01)° ($< 101 >$).

The two preferred growth directions in ALD deposited ZnO are along c-axis and a-axis, but several works show that these preferred orientations of crystal grains can be modified controlling the deposition temperature [109, 110]. The effect of temperature is visible in Figure 4.3, which reports the XRD spectra for 50 nm ZnO deposited at 100°C and 200°C. For samples deposited at 100°C, the strongest contribution is represented by the $< 101 >$ diffraction peak, located around the 36.3° $2\theta$ position. When the deposition temperature increases, the relative intensity of $< 101 >$ peak is reduced and the contribution of the $< 100 >$ and the $< 002 >$ peaks becomes visible, which are positioned at 31.8° and 34.4°, respectively. A quantitative analysis to determine the the relative quantities for the different orientations is performed by calculation of the normalized area of each curve through Voigt fit of the peaks. The contributions of the different orientations are: 5.5% for $< 100 >$, 11.3% for $< 002 >$ and 83.2% for $< 101 >$. It is well known that the

$< 002 >$ orientation (c-axis) is the preferential one in ZnO thin films deposited by different techniques, while $< 100 >$ direction (a-axis) is usually associated to the breakdown of negatively charged hydrocarbon ligands in DEZ [111].

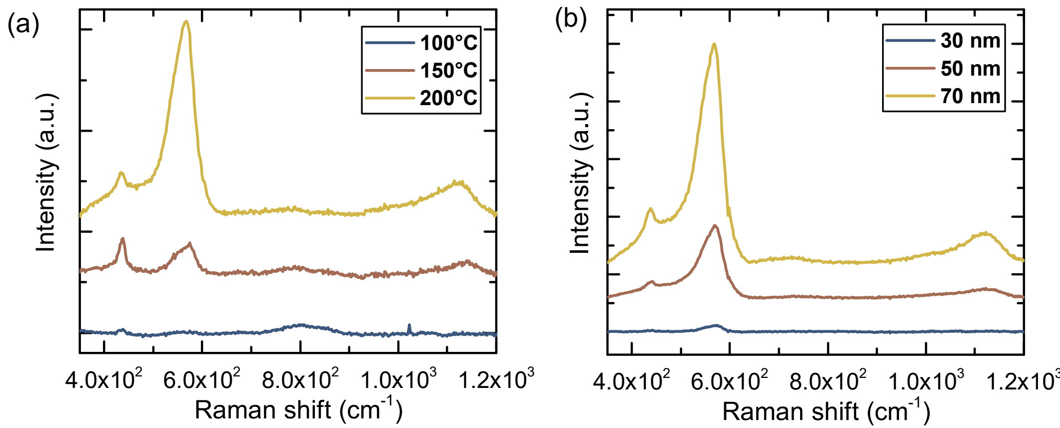


Figure 4.4: Raman spectra for: 50 nm samples deposited at different temperatures(a), and samples deposited at 200°C with different thicknesses (b). (c) Reports the typical Raman spectrum for poly-crystalline ALD ZnO, underlaying the possible viration odes and their position. The technique employed to analyze the different contribution by dismemberment of convoluted peaks is reported in (d).

Figure 4.4a shows the variations of Raman spectra as a function of the deposition temperature, while the dependence on film thickness is presented in Figure 4.4b. It is clearly visible that the crystal content increases with film thickness and high temperature. In the first case it is a result of the structural growth around nanocrystal nucleus, while in the second the higher thermal energy plays an important role. According to the group theory, the Raman active modes for ZnO are the $A_1$ (z direction) and $E_1$ (xy direction) polar modes, having longitudinal and transversal optical components (LO and TO), and the two $E_2$, $E_2$(high) and $E_2$(low) modes. The Raman active modes for ALD deposited ZnO and their positions are indicated in Figure 4.5a. The two higher peaks, positioned at $\sim$435 cm$^{-1}$ and $\sim$ 570 cm$^{-1}$, are connected with the $E_2$ and $A_1$(LO) vibrational modes, and their intensity increases as a function of temperature and film thickness. $E_2$(high), which is the strongest mode in hexagonal-wurtzite crystal structures [108], is an indicator of the crystal content of the film. The high intensity of $A_1$(LO) is attributed to the presence of defects in the thin films [107]. Since the ZnO deposited in this study does not

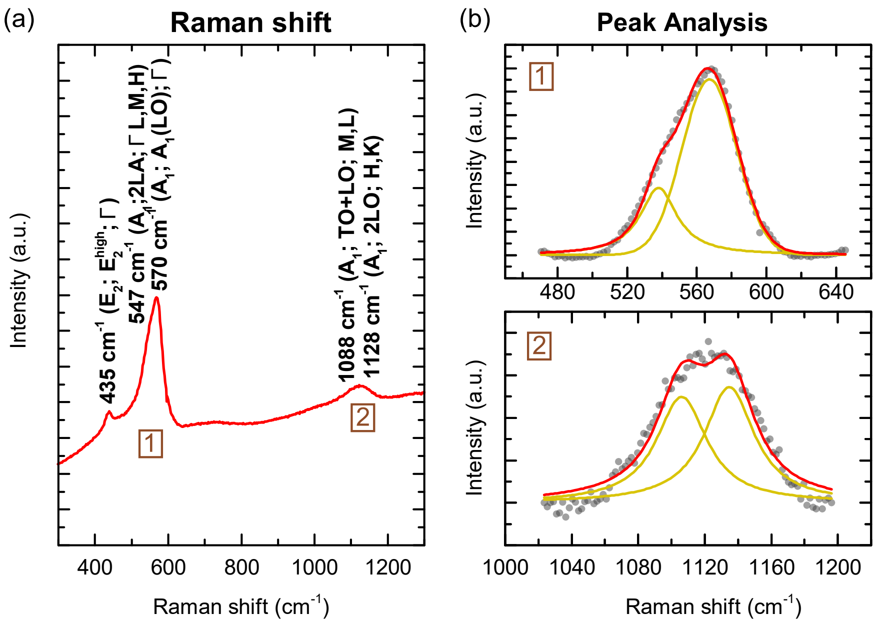


Figure 4.5: (c) Typical Raman spectrum for poly-crystalline ALD ZnO (the spectrum is obtained from a 70 nm thin film deposited at 200°C). On the spectrum, the main vibration modes and their positions are presented; (b) Technique employed to analyze the different contribution by dismemberment of convoluted peaks extracted from (a).

present external contamination or impurities, as it is explained by XPS analyses below, we can assume that the $A_1$(LO) is related to intrinsic defects.
As a confirmation, an XPS depth profile measure is performed on a 50 nm sample deposited at 200° (Figure 4.6), providing a rough idea of the stoichiometry of the thin films. A zoom on the ZnO section shows a slight deficiency of oxygen (44%-47%) respect to the nominal value. The presence of residual H inside the film, due to the trapping of $H_2O$ molecules from reactant, is inspected by studying the O–H and Zn-O bonding from XPS. The H trapping could cause incomplete reactions of DEZ during the consecutive cycle, inducing defects that decrease carrier concentration and mobility [110, 112]. Figure 4.7 shows O1s spectra of ZnO for the film surface and bulk, obtained before and during the depth profiling, respectively. In the surface peak, the O1s spectrum is fitted by the convolution of two Gaussian curves, where the expected peak positions are at 530.4 eV for Zn–O bonding energy and 532.5 eV for O–H bonding energy (Figure 4.7a). The presence of the shoulder at 532.5 eV is a proof of the presence of OH molecules on ZnO surface, while no

evidence of residual H is detected in the bulk (Figure 4.7b).

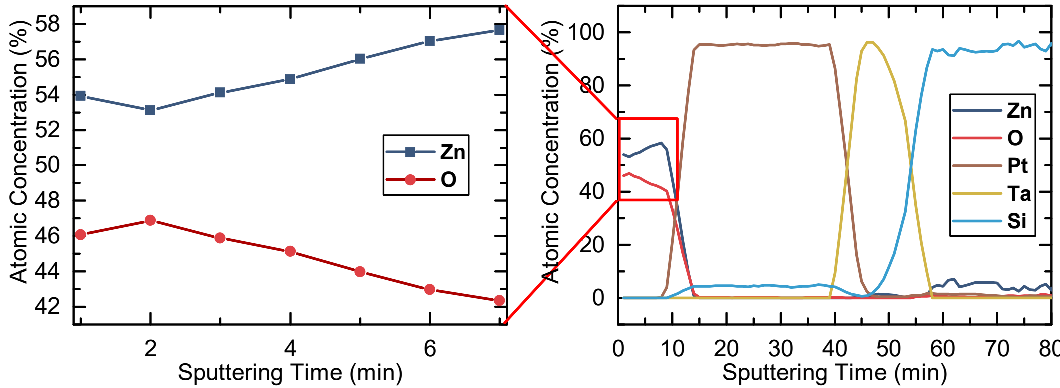


Figure 4.6: XPS depth profile of a ZnO thin film of 100 nm thickness on a Si/Ta/Pt substrate; the graph on the left report a zoom of the profile in the ZnO area, in order to better visualize the film stoichiometry.

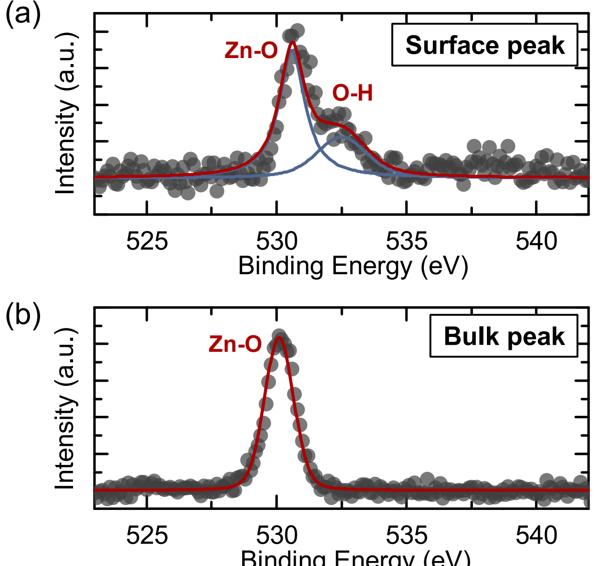


Figure 4.7: XPS high resolution measurement of the O1s peak at the surface (a) and bulk (b). In (a) the two Gaussian curves are centered in (530.6±0.2) eV and (532.5±0.5) eV, while in (b) one peak is visible at (530.10±0.03) eV.

Moreover, the different signal-to-noise ratios obtained for the surface and bulk peaks of Figure 4.7 suggest that a thin layer of adventitious material could have deposited

as a result of the sample exposition in atmosphere. In particular, adventitious carbon, including a variety of hydrocarbons species with singly and doubly bound oxygen functionality, is commonly detected on the surface of the thin films [113]. As a proof of the adventitious carbon, in Figure 4.8the XPS surface analysis for the ZnO thin film reveals a the presence of a non-negligible carbon peak (284.8 eV). This contamination can be reduced through in-situ XPS measurements, made after ALD deposition without breaking the vacuum.

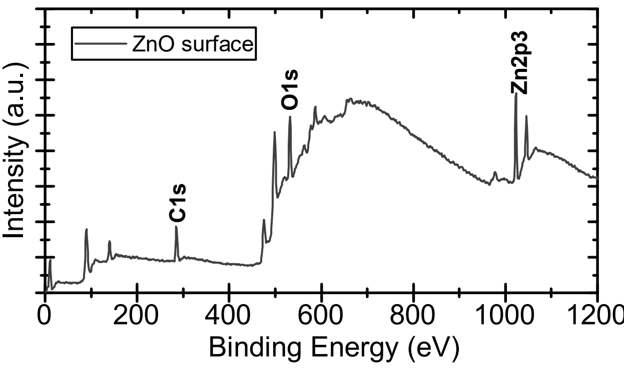


Figure 4.8: XPS surface analysis for a ZnO sample deposited at 200°C, the three reference peaks for Zn, O and C are marked.

## 4.2 DC Electrical Characterization

Two different categories of samples were fabricated for electrical characterization, using the shadow mask process described in Section 2.1. The samples consist of a 1x2 $cm^2$ Si/$SiO_2$ substrate on which a Ta(10 nm)/Pt(100 nm) BE is deposited by sputtering. The ZnO is then deposited by ALD and partially etched in diluted HCl, in order to access the BE. The TE patterning through shadow mask defines different devices on the same substrate. A particular shadow mask process is used for the samples described in Section 4.2.2, including the use of a SiN passivation layer and a lithographic step to pattern the TE active area. Figure 4.9a shows an SEM image in cross section of a Pt/ZnO/Cu device. The first sample set, consisting in Pt/ZnO/Pt structures, belongs to the category of VCM memories, whose working principle is described in Section 1.2.2. The second includes the Pt/ZnO/Cu devices, which can be classified as ECM cells (Section 1.2.2). Figure 4.9b schematize the

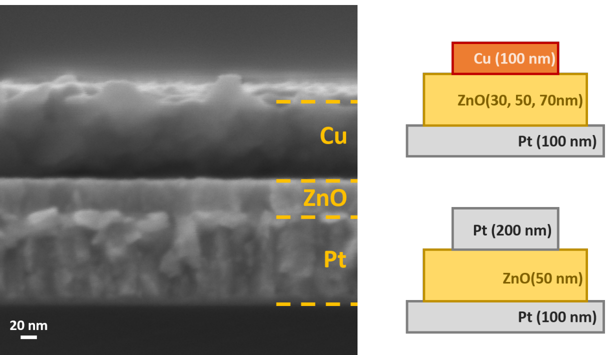


Figure 4.9: SEM image in cross section of one of the devices used for the electrical characterization and schematic representation of the stacks.

two tested stack and present the layer thicknesses.
The testing configuration for all the samples consists in grounded BE and biased TE.

### 4.2.1 Pt/ZnO/Pt structures

The I-V characteristics on 50 consecutive cycles in voltage sweep are reported in Figure 4.10a. The device presents a bipolar switching behavior, with SET operation in negative voltage polarity and RESET in positive. The current compliance is limited to 7 mA during the SET in order to avoid the device final break-down. The forming initial operation is not required for these devices, as has already been reported by previous works on ZnO-based memristors [114–116]. In fact, the CF formation is facilitated by the high quantity of ZnO intrinsic defects, especially oxygen vacancies (Vö), which create a conductive path in the poly-crystalline oxide matrix, without the requirement for high energy. The presence of the crystal grains determines an accumulation of defects along the grain boundaries and, under the applied electric field, charge trapped in these aligned defects can overcome the barrier potential and create the CF [114]. When CF is formed the device switches from HRS to LRS and the current increases. The opposite RESET operation is determined by the rupture of CF through the thermal increase due to Joule heating effect. Figure 4.10b reports the values for HRS and LRS for 50 consecutive cycles. With the HRS mean of $\sim 700\,\Omega$ and the LRS mean of $\sim 80\,\Omega$, the operating window is less than 10.

The main disadvantage of these devices is related to the completely symmetric structure, made of two inert electrodes. This condition generally determines a fast degradation of the device performances [117]. The bipolar switching is induced by the random trap distribution within the CF region, starting from the anode interface. The imbalanced migration of oxygen and the CF rupture point variation over switching cycles significantly affect the endurance, leading this kind of devices to a quick break down. In fact, it is worth noting that the filament gap is positioned within the CF depending on the filament shape (generally the narrower CF part firstly break due to self-accelerated thermal dissolution) and on the previous RESET transitions [41]. The absence of a constriction point in CF shape adds a degree of variability to the Pt/Zn/Pt devices.
Low endurance and small operating window make the devices not suitable for electronic applications. Therefore, the Pt/ZnO/Cu structures have been proposed, to overcome the described limitations.

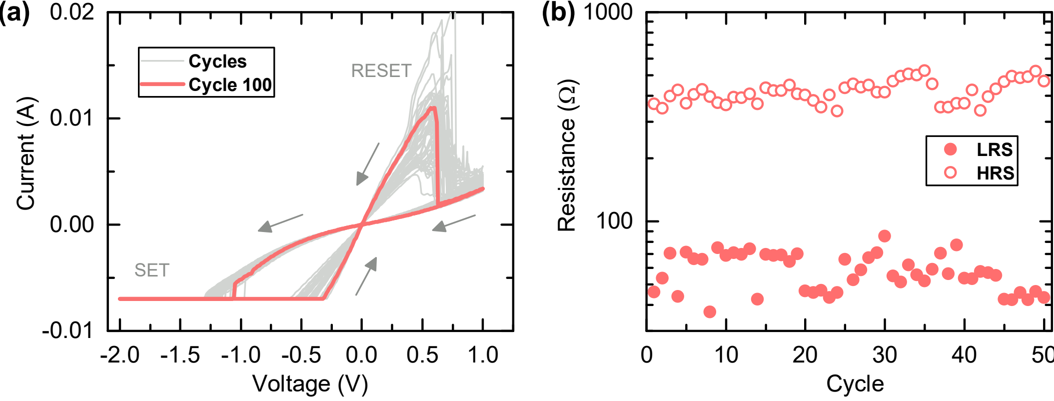


Figure 4.10: (a) I-V characteristic for the Pt/ZnO/Pt stack for 50 consecutive cycles. SET is in negative voltage polarity and RESET in positive; (b) HRS and LRS values for the 50 cycle, measured as the slope of a linear fit between 0 and -0.1 V.

### 4.2.2 Pt/ZnO/Cu structures

The resistive switching of Pt/ZnO/Cu devices is related to the migration of $Cu^{2+}$ ions after a partial anodic dissolution at the active layer/TE interface, which allows the diffusion of metal cations toward the inert BE. However, also the intrinsic

defects of ZnO films participate to the switching, as it will be explained in the next Section 4.2.3. For all the following tests, an initial forming is required. During the forming operations the voltage is fixed at 3 V and the current limitation varies in the range of mA ($I_{cc}$ range between 1 mA and 50 mA), in order to firstly create a stable CF. Coherently with ECM process, which is field-dependent [118], a bipolar switching behavior is observed with SET in positive voltage polarity and RESET in negative. During the SET operations, the $I_{cc}$ is maintained at the same level as the forming one. Among several factors, the mobility of carriers, the CF dimensions, the temperature reached during RESET and the active area dimensions can strongly influence the reduction process near the active TE and the migration of metal cations through the oxide [11, 40, 76]. Different aspects of the Pt/ZnO/Cu were inspected, in order to find an optimum device in terms of electrical response, i.e. resistance state stability, operating window, switching voltages and resistance retention over time.

#### The Impact of Film Thickness

The electrical response of devices with three different thicknesses of the active layer, corresponding to 30 nm, 50 nm and 70 nm, are inspected. The current is limited in positive polarity, where the SET takes place. Figure 4.10 reports the I-V characteristics for the Pt/ZnO(30 nm)/Cu, Pt/ZnO(50 nm)/Cu and Pt/ZnO(70 nm)/Cu stacks. A variation in the resistance state values and stability is notable. The Pt/ZnO(30 nm)/Cu device presents the narrowest operating window, with a LRS of $\sim 20\,\Omega$ and a HRS of $\sim 70\,\Omega$. Although the stability of the two states is good, the resistance ratio is too low to obtain two distinguishable resistance states. This is due to the low resistivity of the ZnO (30 nm) and to the high density of defects in the film. The Pt/ZnO(50 nm)/Cu device exhibits a stable, repeatable switching between the LRS of $\sim 20\,\Omega$ and the HRS of $\sim 170\,\Omega$. Voltages lower than 1 in absolute value are required to SET and RESET the device. Finally, Pt/ZnO(70 nm)/Cu presents a not stable behavior, with a LRS of $\sim 80\,\Omega$ and a highly noisy HRS, whose value changes randomly over cycling.
Considering the I-V graphs of Figure 4.11 and taking into account the intrinsic doping of ZnO films, one can argue that the mechanism involved in the resistance switching for Pt/ZnO/Cu devices is defined by a competition between ECM, which play the major role, and VCM behavior. It has been demonstrated that the two

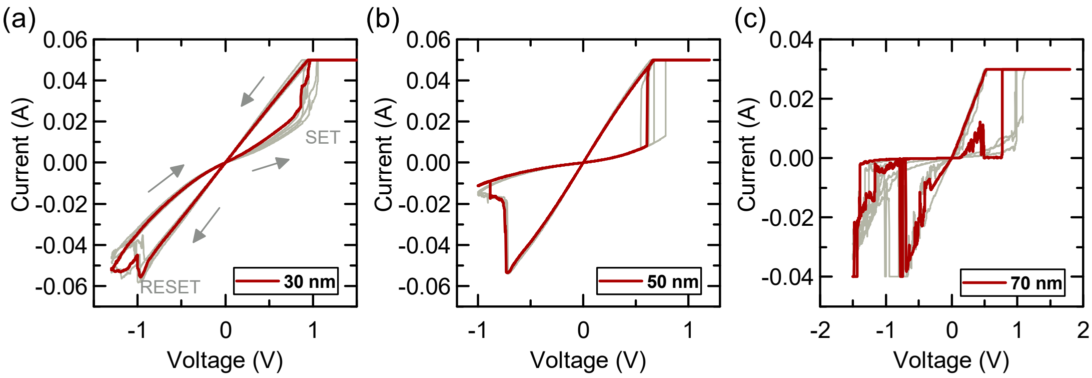


Figure 4.11: I-V characteristics for devices with different thicknesses of the active layer. The curves correspond to: Pt/ZnO(30 nm)/Cu (a), Pt/ZnO(50 nm)/Cu (b) and Pt/ZnO(70 nm)/Cu (c) stack response.

process can coexist in particular conditions [119] and participate both to the CF formation. VCMs show a strong dependence of switching parameters on the thicknesses of ZnO samples, due to the higher grain size and consequent low defects density. Contrarily, ECMs do not show any direct dependence of switching on the oxide thickness, since the filament rupture by temperature increase takes place in a critical area, which is not altered by the thickness variation [120, 121]. In our devices, the Vö defects along the grain boundaries, which are more abundant in the thinner film, participates to the CF formation, resulting in lower switching voltages and HRS values. In fact, when a comparable energy is provided to the different systems, the higher number of free carrier determines the formation of a filament with a wider diameter, which is just partially ruptured during the RESET, resulting in a lower HRS.

An other effect of the increase in film thickness and crystal content is the large fluctuations in the HRS. This can be explained by the filamentary model, observing that the higher grain size makes the formation of multi-branch CF possible. During the RESET operations, some partial filaments may still persist in HRS resulting in a high resistance state variability [120]. The ZnO thickness of 50 nm has been selected as the best compromise between a high operating window and a low resistance state variability, which means a good balance between free-carrier density and crystal dimension inside the film .

### The Impact of Current Compliance Limitation

The SET process can be divided in a nucleation and a growth step. During the nucleation, the partially ruptured CF is rebuilt by ion migration along grain boundaries under the effect of the positive bias on the active electrode (TE). When the CF is formed, the growth step begins involving the increase in CF lateral dimensions along the conductive path [11], until the $I_{cc}$ is reached and the parameter analyzer tool stops the voltage increase. Therefore, the $I_{cc}$ control allows a modulation of the CF diameter, involving changes in the device performances.

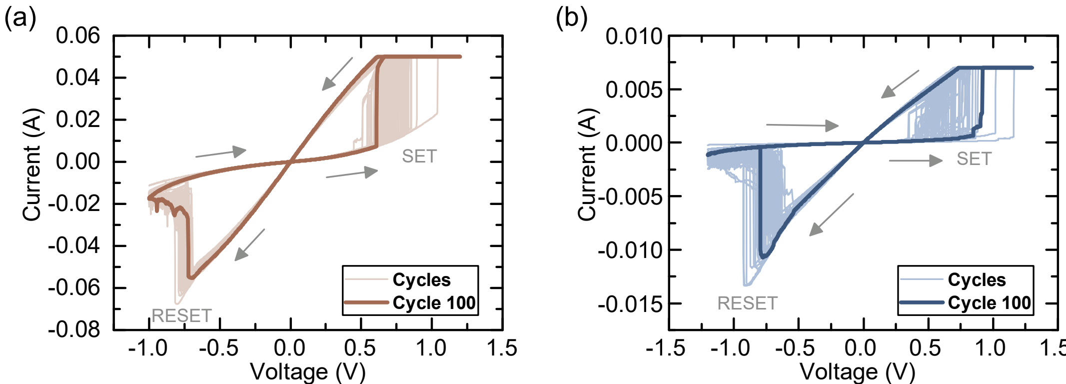


Figure 4.12: I-V characteristics for the Pt/ZnO/Cu stack for 100 consecutive cycles, with two different $I_{cc}$ limits, respectively of 50 mA (a) and 7 mA (b). Set is in positive voltage polarity and RESET in negative.

Figure 4.12a reports the I-V characteristic for 100 consecutive cycles of a Pt/ZnO (50 nm)/Cu device with a current compliance limitation of 50 mA. The high stability in the device electrical response, notable in the overlapped IV, is confirmed by statistical analysis (Figure 4.13a-e). The cumulative probability distribution (Figure 4.13d) of LRS and HRS over 100 cycles reveals a narrow distribution of the data around the mean values of 15 Ω and 170 Ω. Regarding switching voltages, the mean value for $V_{set}$ is 0.7 V and for $V_{reset}$ is -0.8 V. Both the switching voltages present a small variability over cycling (Figure 4.13b). In Figure 4.12b the I-V characteristic for 100 consecutive cycles of a Pt/ZnO(50 nm)/Cu device with an $I_{cc}$ of 7 mA is presented. The LRS is increased, coherently with the reduced filament dimension, at 90 Ω. However the biggest change is visible in the HRS, whose mean value results in 2980 Ω, showing that the reduced CF dimensions are crucial also during RESET operation when enough energy is provided to the device to completely break the

filament. The increased operating window results in a lower stability of the HRS and wider distribution of switching voltages (Figure 4.14a-d).

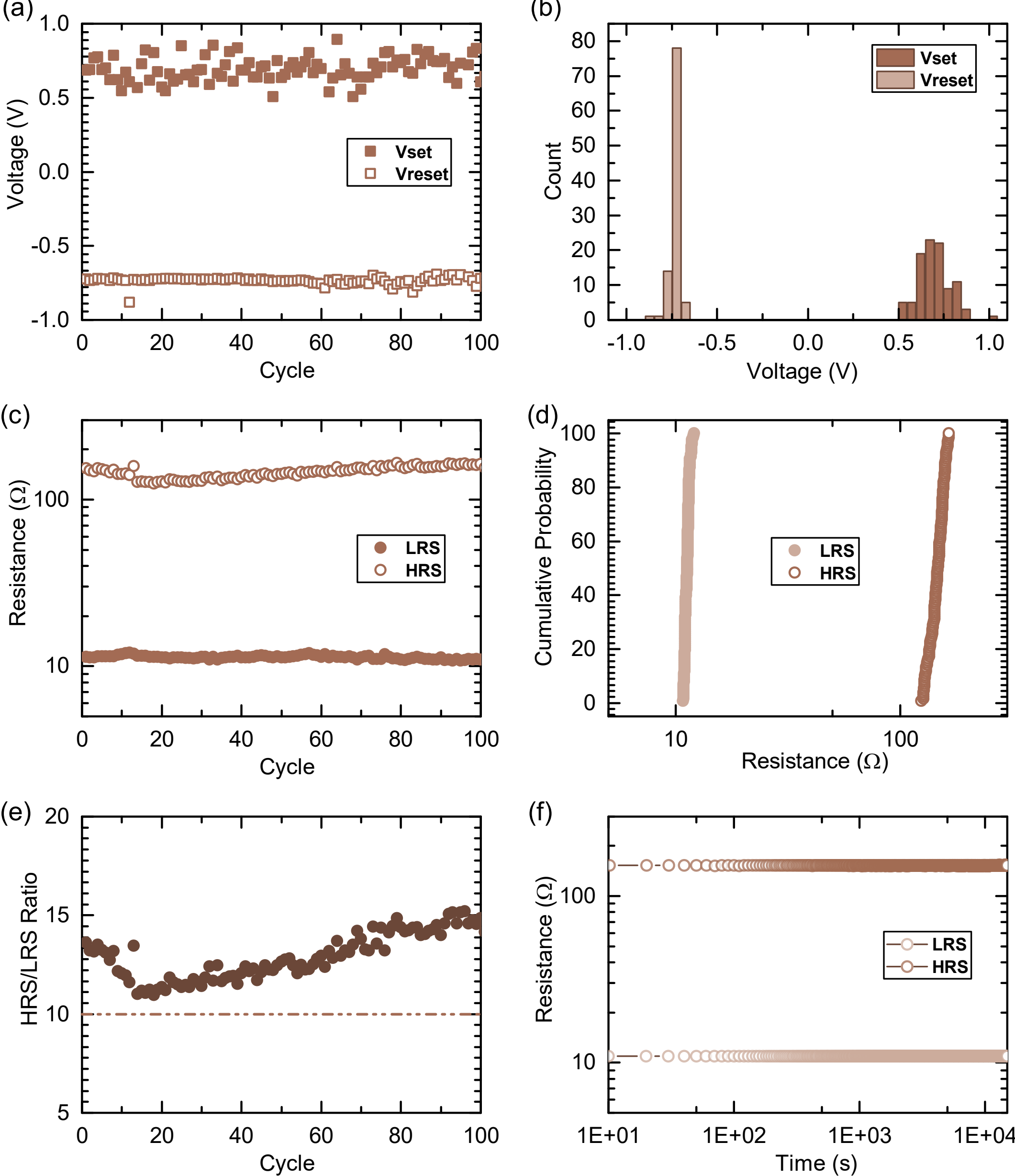


Figure 4.13: Switching parameters for the sample measured at $I_{cc}$ =50 mA: $V_{set}$ and $V_{reset}$ values and distribution are reported in (a)-(b), resistance states values, cumulative probability distribution and HRS/LRS ratio are reported in (c)-(d)-(e), retention of HRS and LRS is presented in (f).

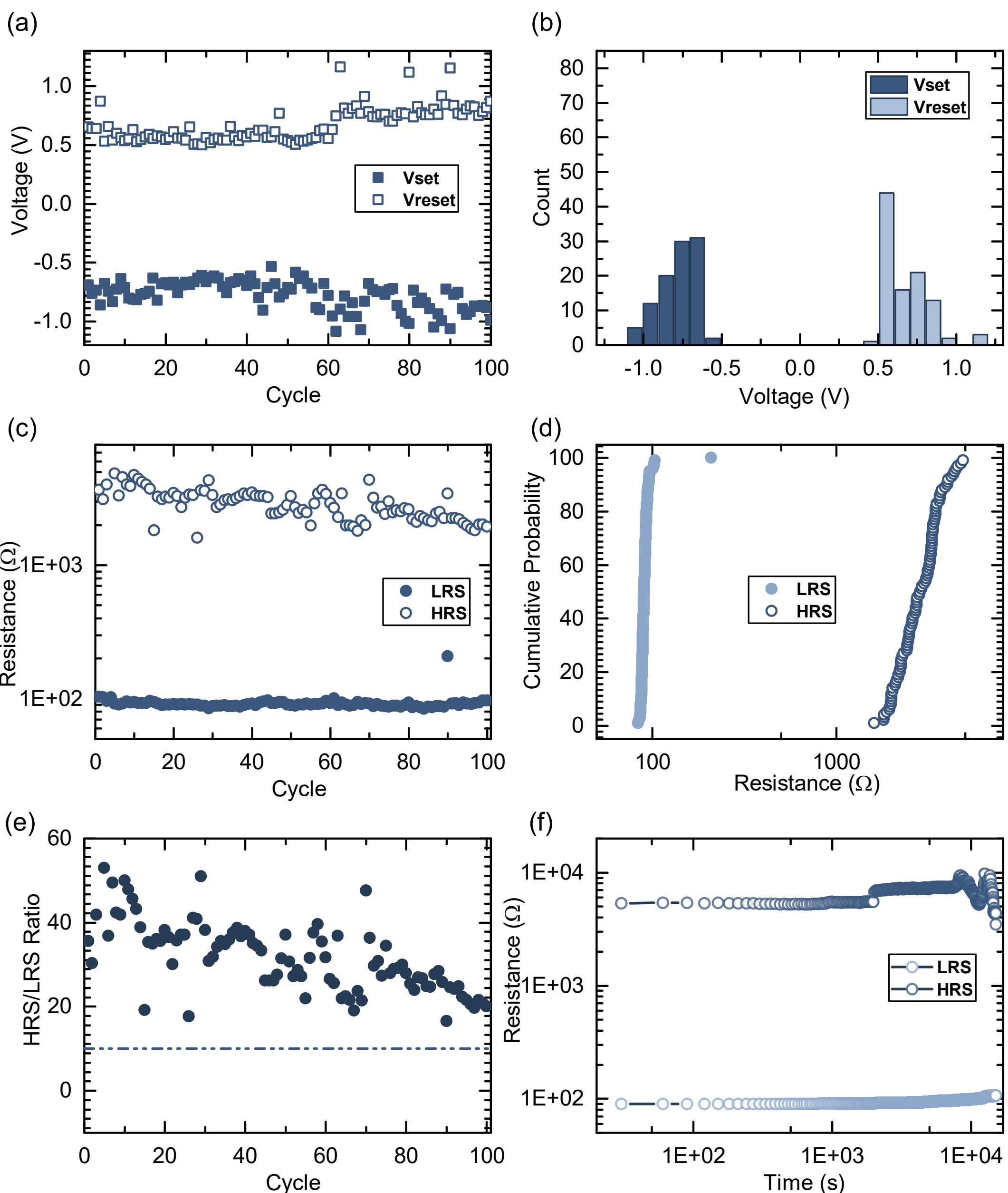


Figure 4.14: Switching parameters for the sample measured at $I_{cc}$ =7 mA: $V_{set}$ and $V_{reset}$ values and distribution are reported in (a)-(b), resistance states values, cumulative probability distribution and HRS/LRS ratio are reported in (c)-(d)-(e), retention of HRS and LRS is presented in (f).

In both cases, the resistance ratio is higher than 10 (Figure 4.13e and 4.14e), indicating that there is no overlapping of LRS and HRS and the devices are suitable for

nonvolatile memory applications. Finally the retention of the HRS and LRS value is inspected for both the configuration as reported in Figure 4.13f and Figure 4.14f.

### The Impact of Electrode Size

Direct measurements of filament dimensions reveal a diameter in the order of 10-20 nm [19]. Since these dimensions are considerably smaller than the electrode area, CF formation and rupture are defined by a localized conduction effect [101]. Therefore, the dimension of the electrodes should not influence the switching behavior of the device in a pure filamentary switching mechanism [114]. In order to prove the filamentary switching, two different shadow mask samples were realized, defining two different active areas with diameters of 0.5 mm and 5 $\mu$m respectively.

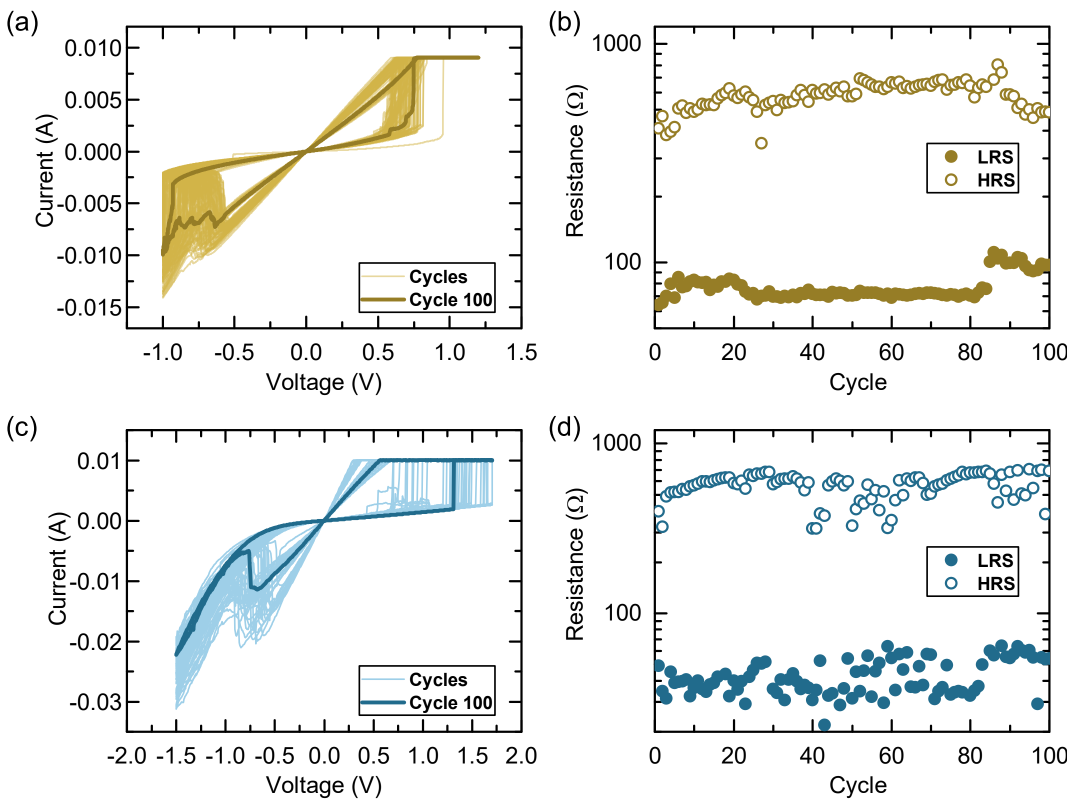


Figure 4.15: I-V characteristics and resistance state values over 100 cycles for two sample with the different active areas of 0.5 mm (a,b) and 5 $\mu$m (c,d).

Figure 4.15 reports the I-V characteristics and the resistance state values for the two different samples. The differences in I-V characteristics and in particular the higher variability over cycling of the 5 $\mu$m devices are due to the addition of an external lithographic step with consequent chemical contamination of the surface, adding a degree of uncertainty on the switching behavior. However, one can notice that the samples present similar HRS and LRS values and comparable switching voltages. The similarity in the electrical response of the devices with 0.5 mm and 5 $\mu$m active areas proves that switching is mainly based on the filamentary model, since filament dimensions and kinetics are not influenced by the size of the active area.

### 4.2.3 Device comparison and mechanism discussion

In order to summarize the DC characterization results for the Pt/ZnO(50 nm)/Pt and Pt/ZnO(30, 50, 70 nm)/Cu stacks, the Table 4.1 reports the obtained switching parameters and electrical performances. The Pt/ZnO/Pt devices show a stable switching, with SET and RESET polarities dependent on the initial voltage input. However, the best switching performance is observed in correspondence of the SET in negative polarity. This can be explained by the different oxygen incorporation at the sputtered Pt TE and the ZnO film interface respect to the BE/ZnO one. The fact that the device majority presents a forming-free behavior is an indicator of the abundance of intrinsic defects, in particular oxygen vacancies, in as-grown ZnO. The low cycle to cycle variability of the resistance states in this stack is determined by the presence of grain boundaries, which define a path along with the Vö filament is formed. The CF confinement requires also similar energy over cycling to be broken and rebuilt. The main issue of Pt/ZnO/Pt devices is related to the device symmetric structure, resulting in lower reliability and short life time. It is widely accepted that asymmetric structures, in which the filament formation can be orientated, result in a better stability and longer endurance. Several works report, for example, the enhancement of the device performances by layer addition to break the symmetricity of the device [32, 122–124].
The presence of pre-existing oxygen vacancies and the poly-crystalline structure in ZnO film deposited at 200°C plays an important role also in the switching behavior

Table 4.1: Mean value and standard deviation (as error) for the LRS and HRS values, HRS/LRS ratio, $V_{set}$ and $V_{reset}$ over cycling, DC endurance and retention. The table report the values for the Pt/ZnO(50 nm)/Pt and Pt/ZnO(30,50,70 nm)/Cu stacks

| **Structure** | **Switching Parameters** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **$I_{cc}$ (mA)** | **LRS (Ω)** | **HRS (Ω)** | **Ratio** | **$V_{set}$ (V)** | **$V_{reset}$ (V)** | **End. cycle** | **Ret. (s)** |
| Pt/ZnO(50 nm)/Pt | | | | | | | | |
| | 7 | 60 ±1 | 417 ±7 | 7.5 ±0.3 | -0.86 ±0.24 | 0.68 ±0.02 | <100 | - |
| Pt/ZnO(30 nm)/Cu | | | | | | | | |
| | 50 | 19.4 ±0.2 | 40 ±3 | 7.5 ±0.3 | 1.0 ±0.2 | -1.1 ±0.1 | ∼100 | - |
| Pt/ZnO(70 nm)/Cu | | | | | | | | |
| | 30 | 70 ±30 | 1.0k ±0.4k | 40 ±20 | 1.1 ±0.3 | -1.0 ±0.2 | 20 | - |
| Pt/ZnO(50 nm)/Cu | | | | | | | | |
| | 7 | 90 ±10 | 2.8k ±7 | 32 ±0.7k | 0.67 ±10 | -0.78 ±0.12 | ∼100 | $10^4$ |
| | 10 | 80 ±10 | 460 ±50 | 7 ±1 | -0.86 ±0.24 | 0.68 ±0.02 | ∼200 | - |
| | 50 | 11 ±1 | 146 ±11 | 13 ±1 | -0.89 ±0.11 | 0.72 ±0.15 | ∼400 | $10^4$ |

of Pt/ZnO/Cu devices. Concerning the film structure, the diffusion of the electrochemically active Cu through grain boundaries is highly facilitated [125]. Although $Cu^{2+}$ ions constitute the main contribution to the creation of a conductive bridge between the two electrodes, we can assume that the high number of oxygen vacancies participates to the process. The result is an intermixed filament in which Cu and Vö cooperate in the CF formation. Similar conclusions are reported in different works [19, 126]. The Cu-Vö mixed filament can result in a low state stability, which increases proportionally to the CF lateral size. The samples tested with high $I_{cc}$ limitation are more stable in term of C2C variability. A study about the transport mechanism of Pt/ZnO/Cu devices during RESET will be presented in the next chapter (Section 5.2.3).
The optimum in term of device performances is identified in the Pt/ZnO(50 nm)/Cu

stack.

## 4.3 AC Electrical Characterization

Pulse measurements were performed on Pt/ZnO(50 nm)/Cu memristors using the Keithley 4200, in order to investigate how the internal resistance state can be tuned gradually. In particular, the device ability to mimic the synaptic behavior is demonstrated by proving long term potentiation and depression (LTP and LTD), in which the reading is performed after every pulse at 0.1 V. The control of conductance decrease (depression) and increase (potentiation) by pulsed measurements is achieved by trains of consecutive identical pulses in negative and positive polarity respectively. The Keithley 4200 allows to control the pulse rise time, pulse width and voltage amplitudes in both polarities ($V_{neg}$ and $V_{pos}$), which are crucial parameters to control the amount of energy provided to the system to accomplish the RESET and SET operations. To obtain a gradual resistance variation and not a sharp change, the energy provided to the system has to be modulated carefully, finding a good balance between voltage amplitude and pulse timing [67, 127, 128].

### 4.3.1 Effect of the pulse timing

Figure 4.16 shows the current variation during a 2 ms pulse cycle: reset occurs in negative polarity and is characterized by a gradual slow current change, while SET is a sharp process in positive voltage polarity.
In our devices a trade-off between the resistance saturation value and the pulse timing of the stimuli appears to exist. However, the voltage amplitude has a high impact on the gradual resistance control. Fixing the negative and positive pulse amplitudes to -1 V and 1 V, which are the minimum voltage values to obtain a sharp HRS $\leftrightarrow$ LRS transition, the pulse timing effect is inspected. In order to modulate the pulse timing, rise time (and the symmetric fall time) is targeted to be half of the pulse width, and the delay between consecutive pulses is set as $t_{width} + 2 * t_{rise}$. In this way it is possible to define a pulse frequency as $1/(t_{pulse} + t_{delay})$. The pulse frequency is increased from 250 Hz (2 ms of pulse width) to 25 kHz (40 $\mu$s of pulse width) and the LRS and HRS values are measured in correspondence of 0.1 V. In Figure 4.17a, three representative I-V curves from pulsed cycles are presented for

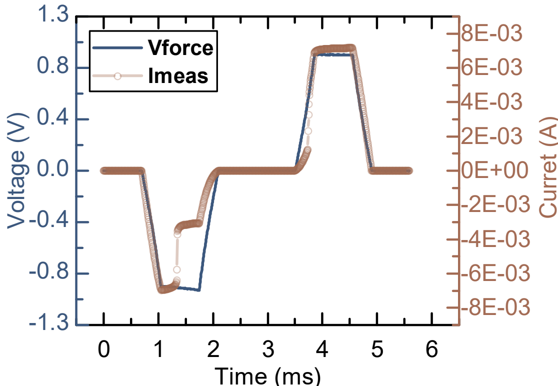


Figure 4.16: Representative pulsed measurement: forced voltage and measured current are reported. $V_{neg}$ and $V_{pos}$ are fixed at -1 V and 1 V respectively and the $I_{cc}$ is fixed at 10 mA and is never reached.

different pulse width, showing a strong voltage snap-back and snap-forward during SET and RESET transitions, respectively. As reported in literature [129–131], these effects are related to the presence of an internal resistance in series with the device. In our case, the behavior is notable only during pulsed measurement and has to be attributed to the testing system. In fact, the SPGU module for pulse generation of Keithley 4200 adds a series resistance to the system, which is not negligible compared to the low operating range of resistance for ZnO.

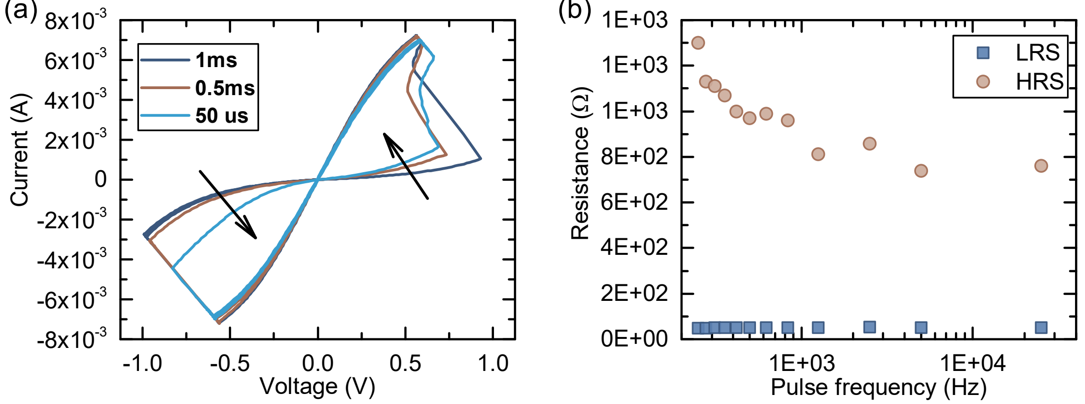


Figure 4.17: (a) I-V characteristic from different pulse timing; (b) HRS and LRS values depending on the pulse frequency, during the measurement the following conditions are used: $V_{neg} = -0.9$ V and $V_{pos} = 0.9$ V, $I_{cc}$ is fixed at 10 mA.

As it is visible in Figure 4.17b, in the range 2 ms - 40 $\mu$s the LRS is not influenced by the pulse timing while HRS value decreases from 1.3 k$\Omega$ to 750 $\Omega$, maintaining however a resistance ratio higher than 10. The energy provided during RESET is not sufficient to create a complete filament rupture and a part of ions remains in the filament path, leading to an HRS which is lower than the nominal one. The presence of a partial filament facilitates the next CF formation during the SET, which requires a lower quantity of energy. This explains the invariant LRS value depending on the pulse timing. For pulses at a frequency higher than 25 kHz, the number of pulses needed to reset the device increases (about 20 pulses are required for a frequency of 50 kHz) and also the SET requires more then one pulse to be completed.

### 4.3.2 Modulation of conductance - LTP and LTD

The pulse timing is fixed for all the following measurements at 5 $\mu$s rise time and 10 $\mu$s pulse. With the purpose of identifying the best voltage region for the gradual weight modulation, different combinations of pulse voltage amplitudes and pulse number are tested. In fact, decreasing the applied voltage, one can observe that the number of conductance multi-state increases and an higher number of pulses is needed in order to reach the conductance threshold. The potentiation/depression procedures for different voltages are repeated on the same device. After each test, the device is brought back to the pristine condition. Figure 4.18 reports the conductance variation in response to different pulse amplitudes. The effect for the higher voltages is a digital response, in which the first pulse dominates the conductance change and allows to reach the threshold value in an abrupt way. While, decreasing the applied voltage, the conductance modification becomes more gradual.
The best analogue variation is obtained for a voltage amplitude of -0.8 V in negative and 0.7 V in positive polarity, employing a train of 100 pulses for both potentiation and depression. Figure 4.19 shows a representative measurement in this conditions. The measured current as a function of the applied voltage for 100 consecutive negative and positive pulses are reported in Figure 4.19a,b.
The conductance continuously decreases during the negative pulses, as a direct consequence of the slower kinetics of the RESET operations, while during the potentiation a first high jump is obtained and than the variation becomes gradual

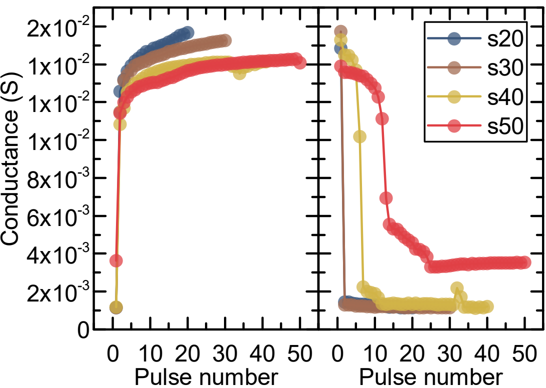


Figure 4.18: Potentiation and Depression procedures for different pule amplitudes and pulse number. Blue line is the response of the device to $V_{reset} = -1V$, $V_{set} = 1V$ and $number_{pulse} = 20$; brown line corresponds to $V_{reset} = -1V$, $V_{set} = 0.9V$ and $number_{pulse} = 30$; yellow line corresponds to $V_{reset} = -0.95V$, $V_{set} = 0.8V$ and $number_{pulse} = 40$; red line corresponds to $V_{reset} = -0.9V$, $V_{set} = 0.75V$ and $number_{pulse} = 50$.

(Figure 4.19c,d). This asymmetry, which is an intrinsic behavior of filamentary memristors and is due to the different physical mechanisms involved in RESET and SET [13, 127], determines a better control on depression with a higher number of available states. Moreover, one should observe that in both the LTD and LTP the conductance variation does not follow a linear trend. This is still an open issue in the realization of memristor able to behave as synapses.

As a final remark, these measurements demonstrate the ability of ZnO-based memristors to mimic the synapses behavior. However, systematic tests are still needed to define a standard procedure in view of neromorphic applications. To this purpose, a new device geometry has to be defined including a lithography process and external $I_{cc}$ limitation, in order to reduce the device active area and the leakage current. The goal of this work was to provide a proof of concept of the feasibility of reliable ZnO-based memristor, whose resistance can be gradually modulated by train pulse input stimuli for future application on neuro-inspired circuits.

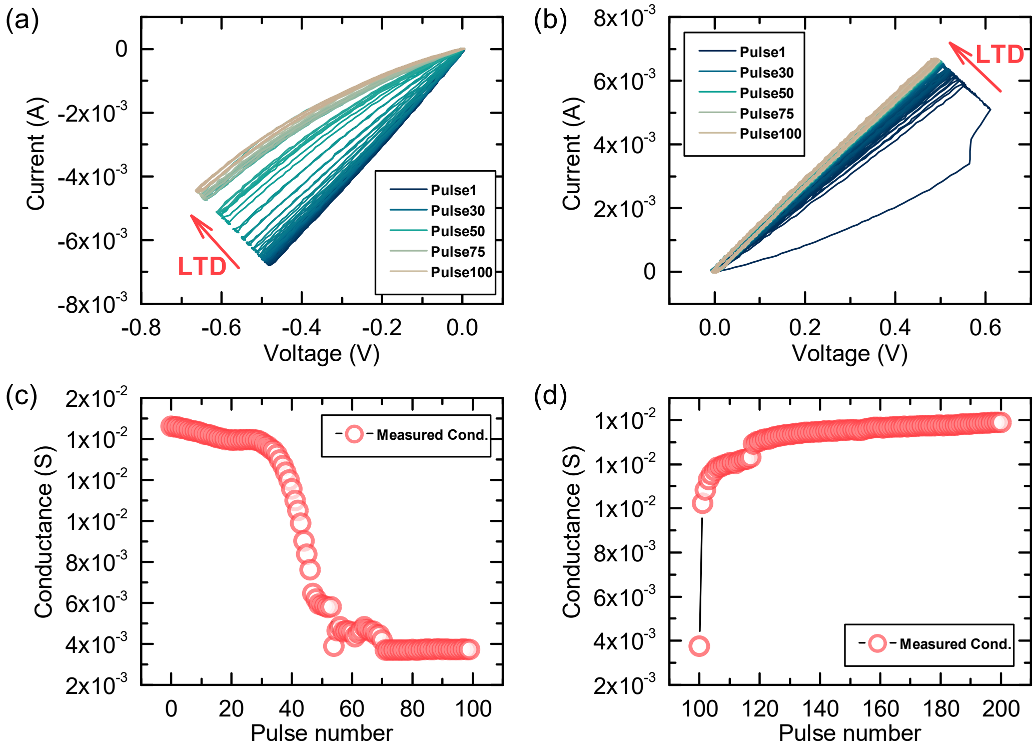


Figure 4.19: I-V characteristics of 100 consecutive pulses and correspondent conductance values for a depression (a-c) and a potentiation (b-d) operations. During the measure: $V_{neg} = -0.8\,V$, $V_{pos} = 0.7\,V$ and pulse width $= 10\,\mu s$

# Chapter 5

# $ZnO_x$:$Al_2O_y$ Based Memristors

The creation of native defects, Zn interstitial and Vö, during the ALD deposition affects ZnO-based memristor performances. In particular, for ECM-based devices, the abundance of intrinsic defects determines a participation of Vö in the switching kinetics of the device, resulting in high C2C variability and fast device degradation. The main purpose of doping is to introduce compensator defects in the ZnO films, decreasing the native defect concentration. The result is the increase of oxygen concentration and improvement of insulating behavior of the film.
Among different doping agents, such as Co, Ce and Mn, and techniques [77, 78, 101, 132], we inspected the effect of the insertion of single $Al_2O_3$ layers in the ZnO, associated with the ALD doping concept. This doping technique implies a reduction in the poly-crystalline content of ZnO structure, which can have a role in the switching performances. In the first part of the chapter, the parameters for ALD doping are reported, understanding the impact of $Al_2O_3$ on the ZnO morphology, structure and physical and chemical properties. The effect of doping on the electrical responses of the $ZnO_x$:$Al_2O_y$ memristors is reported in the second section, in terms of switching performances and behavior stability over cycling.

## 5.1 $Al_2O_3$ doping of ZnO

### 5.1.1 Definition of the growth parameter

The doping of ZnO via ALD is achieved following the procedure described in Section 1.3.2: a single TMA-$H_2O$ cycle is periodically inserted between a fixed number of DEZ-$H_2O$ cycles (Figure 5.1a). The pulse duration is adjusted to 0.2 s - 0.5 s for the DEZ-$H_2O$ cycles and 0.15 s - 0.15 s for the TMA-$H_2O$ ones, while the purging time is fixed at 2 s in both cases. All the samples are deposited on a Si/$SiO_2$/Ta/Pt substrate, in order to be comparable with the one used for memristor device realization. The Pt layer of 100 nm is deposited by sputtering, adding a 10 nm Ta adhesion layer without breaking the vacuum. The temperature for the ALD process is set at 200°C. The superposition in the temperature windows of ZnO (70-200°C [110]) and $Al_2O_3$ (150-400°C [81]) facilitates the deposition of homogeneous mixed compounds, guaranteeing good adhesion of the two different oxides one on top of the other. However, the different surface reactivity, the interruption of the growth during the first stages and the chemical reactions between mixed precursors can affect significantly the growth. In order to define the best ALD deposition parameters, samples with different $Al_2O_3$ content (AZO films) were deposited and characterized. The list of samples used for material and electrical testing is reported in Table 5.1. By varying the relative proportions of $Al_2O_3$ and ZnO cycles, samples with 1% 5% 10% 20% and 30% $Al_2O_3$ doping content are obtained. The total number of cycles is targeted in order to obtain a film thickness of 50 nm. The Table reports the thickness measured on the SEM cross section images and the growth per super-cycle (GPS).
The two oxides present dissimilar growth rates in the respective temperature windows: the estimated GPC for ZnO is 0.22 nm/cycle, while for $Al_2O_3$ is 0.12 nm/cycle. Moreover, in the early stage of the growth, $Al_2O_3$ has short nucleation period respect to ZnO, which requires ∼4-6 cycles to reach the nominal growth rate, as it has been demonstrated by by Elam et al. [133] through in situ measurements during ALD deposition. The delay in ZnO growth may be due to the slow initial evolution of ZnO nano-crystals; when the crystal core is formed, the growth and the increase of the crystal sizes are faster an give rise to the nominal GPC for ZnO [83]. In both cases, the initial nucleation depends on the hydroxyl groups on the substrate surface, whose concentration is higher on the initial substrate that has

Table 5.1: AZO structures used for material and electrical characterizations. The table presents: the doping percentage (evaluated as the ratio between $Al_2O_3$ and ZnO cycles in a super-cycle), the measured thickness, the calculated growth per supe-cycles (GPS) and the recipe used for the ALD process.

| **Sample** | **Doping %** | **Thickness (nm)** | **GPS nm/sc** | **Recipe** |
|---|---|---|---|---|
| ZnOpure | 0 | 46 | 0 | 227 DEZ cycles |
| Doped1 | 1 | 51 | 21.8 | (22 DEZ+ 1 TMA)x2 +27 DEZ cycles |
| Doped5 | 5 | 49 | 4.34 | (19 DEZ+ 1 TMA)x11 +7 DEZ cycles |
| Doped10 | 10 | 50 | 2.13 | (9 DEZ+ 1 TMA)x23 +7 DEZ cycles |
| Doped20 | 20 | 31 | 0.98 | (4 DEZ+ 1 TMA)x50 +2 DEZ cycles |
| Doped30 | 30 | 30 | 0.56 | (2 DEZ+ 1 TMA)x90 +2 DEZ cycles |

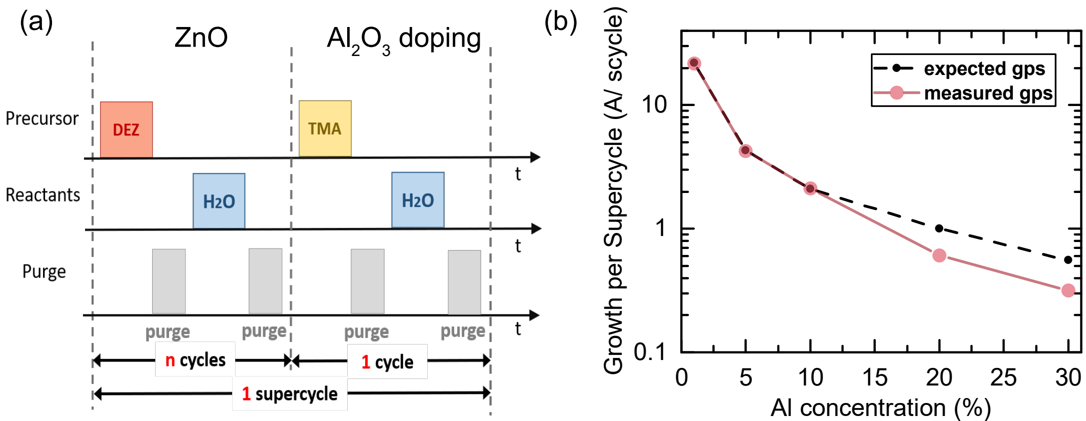


Figure 5.1: (a) Diagram of the deposition process used for the realization of $Al_2O_3$ doped ZnO samples. The n number of DEZ-$H_2O$ cycles defines the periodicity of $Al_2O_3$ insertion and the final doping concentration; a super-cycle is composed by n DEZ/$H_2O$ and 1 TMA/$H_2O$ cycles. (b) Comparison between expected and evaluated GPS depending on the $Al_2O_3$ doping percentage.

been exposed to air. Figure 5.1b reports a comparison between evaluated GPS and the expected one, defined as: $GPS_{expected} = (0.22\,nm \cdot n) + (0.12\,nm \cdot 1)$, where n is the number of consecutive ZnO cycles in a super-cycle. For $Al_2O_3$ doping lower than 20%, the measured GPS does not differs from the expected, while for higher dopant concentrations the growth is reduced. The main factor influencing

this growth change is the nucleation delay of the ZnO on the $Al_2O_3$ single layer. A finite number of DEZ/$H_2O$ cycles is required to start the nucleation and, during this step, the GPC is significantly reduced respect to the bulk value. Therefore, when the periodicity of $Al_2O_3$ insertion becomes lower than 10 cycles, the ZnO deposition never reaches the nominal GPS and the total film thickness is reduced. Moreover, the thickness reduction can also be attributed to a partial etching of the ZnO, which interacts with the $Al_2O_3$ precursor. During the AZO film deposition, when the TMA is introduced in the ALD chamber on the ZnO layer, which acts as substrate, the chlorides groups of TMA interact with Zn molecules, following the reaction:

$$ZnOH^{\bullet} + A(CH_3)_3 \rightarrow Al(OH)(CH_3)^{\bullet} + Zn(CH_3)_2 \tag{5.1}$$

This reaction determines a partial etching of the ZnO oxide film during ALD process, involving the formation of a volatile $Zn(CH_3)_2$ compound by the exothermic reaction of the Zn extracted from the hydroxylated ZnO surface and the TMA (activation energy = -81 kcal/mol) [133]. QCM measurements performed by Elam et al. revealed a negative growth rate, as a proof of this etching reaction. The combined effects of nucleation delay and surface etching are particularly evident when the number of consecutive ZnO cycles is lower than 5, i.e. for the Doped20 and Doped30 samples, in which film thickness and GPS are significantly reduced respect to the expected ones (Figure 5.1b).

The Al content inside the film in % is evaluated by EDX measurements ad compared with the ideal one [86, 134]. The ideal at.% Al concentration is calculated using the formula:

$$GPS_{expected} = \frac{100}{(\rho_{Zn}/\rho_{Al}) \cdot (n - \tau + \tau \cdot exp(-n/\tau) + 1)} \tag{5.2}$$

where $n$ is the number of ZnO cycles in a super-cycle, $\tau$ is the number of cycles needed to reach the ZnO nominal growth rate (approximated at 5), $\rho_{Zn} = 8.84\,10^{14}\,\mathrm{cm}^{-2}$ and $\rho_{Al} = 4.44\,10^{14}\,\mathrm{cm}^{-2}$ are the planar atomic densities of Zn in ZnO and Al in $Al_2O_3$, respectively [86]. Therefore, the evaluation takes in account the atomic density dependence on the number of consecutive cycles for ZnO, while the Al density is assumed to be constant across all the samples, since one single TMA-$H_2O$ cycle is deposited in each super-cycle. The values of Al% concentration

calculated by 5.2 are compared with the one extracted from the EDX data (Figure 5.2), revealing a good accordance between the two data sets, which is a further confirmation of the ZnO reduced GPC in the early stages of the growth.

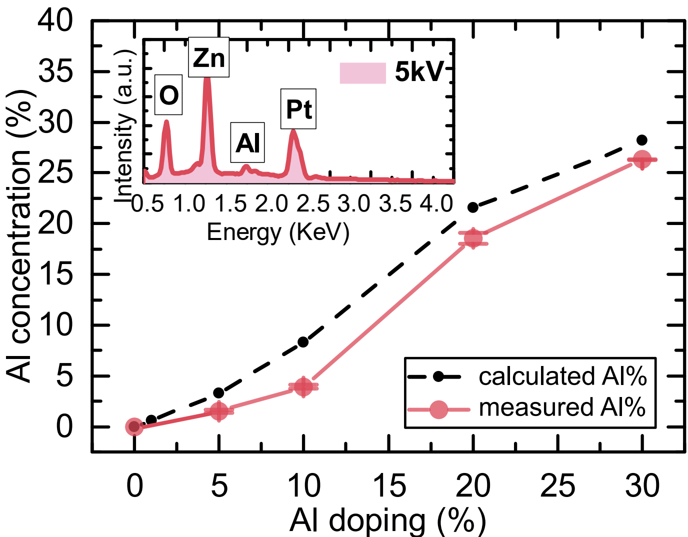


Figure 5.2: Al concentration inside the AZO films depending on the $Al_2O_3$ doping percentage. The Al concentration calculated through Equation 5.2 is reported in black, the one measured from the EDX spectra is reported in red. The inset reports a representative EDX spectrum used to evaluate the element concentration, using an e-Beam energy of 5 kV. The reference peaks are: O K$\alpha$ (0.518 keV), Zn K$\beta$ (9.577 keV) and Al K$\alpha$ (1.469 keV).

### 5.1.2 Physical and chemical properties of AZO thin films

ZnO and $Al_2O_3$ deposited via ALD exhibit very dissimilar physical and electrical properties. In particular, ZnO is poly-crystalline and has low resistivity, while $Al_2O_3$ films are amorphous and insulating [85]. Therefore, the properties of the mixed compound can be tuned over a wide range of values.
A rough idea of the AZO film structure can be obtained from the SEM images in top view and cross section reported in Figure 5.3. In particular, it is evident that AZO films with an Al doping % $\leq$10 are poly-crystalline, with a dimension of crystal grain in the order of $\sim$30 nm. Increasing the $Al_2O_3$ content, the crystal size is reduced and the columnar structure typical of pure ZnO films disappears. At high

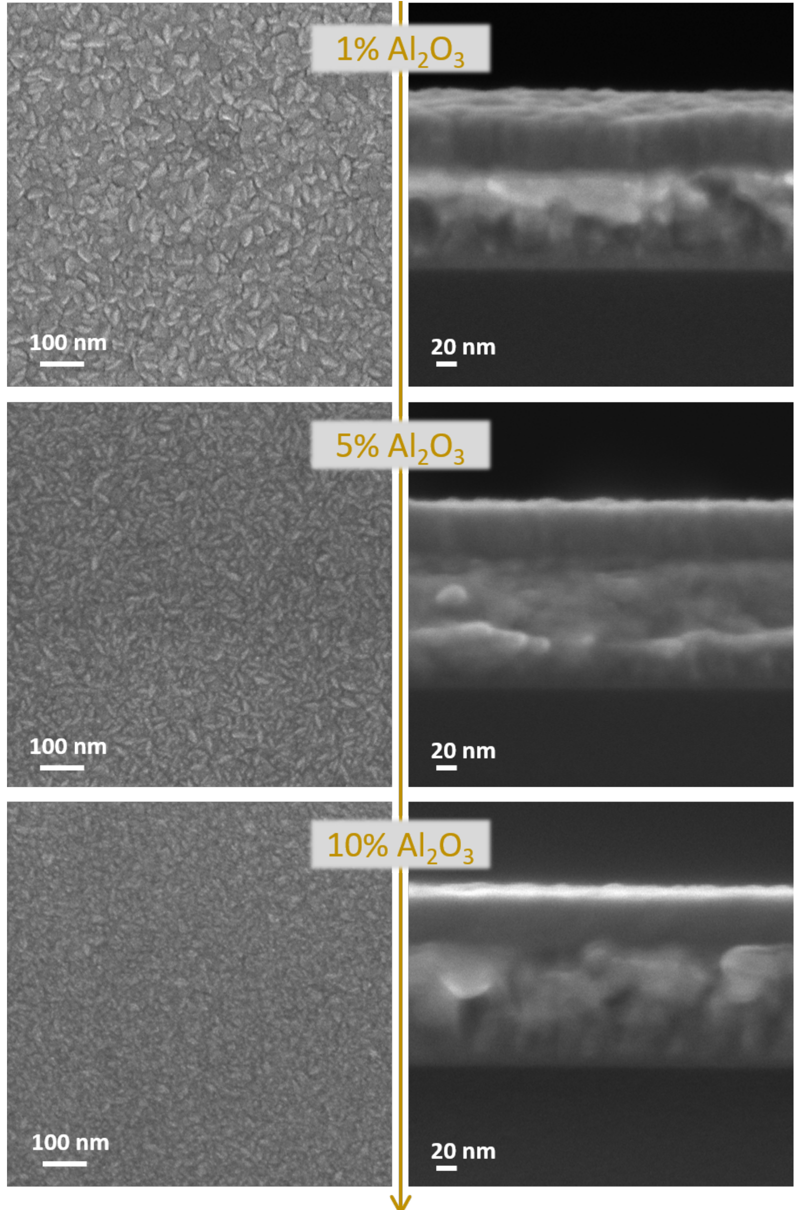


Figure 5.3: SEM images in top view (left) and cross section (right) for the 10 Doped, 5Doped and 10Doped samples. In the cross section images, the $SiO_2$/Pt/AZO is visible.

Al doping concentrations (Al doping % $\geq$20), the abundance of $Al_2O_3$ ALD cycles induces the amorphous phase. Since the weakening of the poly-crystal structure, as a result of the excessive dopant, may deteriorate the switching behavior, reducing performance stability and C2C reliability [79, 135, 136], in this study the maximum

considered Al doping is the 10%.
The structural properties of the mixed compounds are inspected through XRD spectroscopy. Figure 5.4 reports the XRD patterns obtained for the AZO films compared with the pure ZnO, showing a change in the crystal size and orientation depending on the $Al_2O_3$ content. The constant thickness of the films guarantees a correct comparison of the samples, since crystallization behavior is thickness dependent for ZnO (Section 4.1.2).

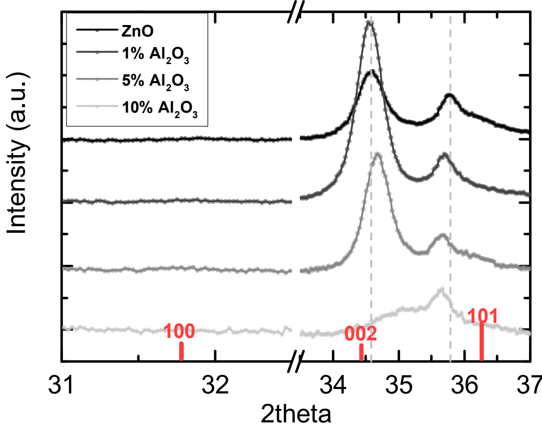


Figure 5.4: XRD spectra for the pure ZnO and the AZO films (Doped1, Doped5, Doped10). In red the reference peaks and relative intensity are reported.

For low $Al_2O_3$ concentrations, the $< 002 >$ peak is the dominant orientation but also the $< 101 >$ is evident. When the doping is higher, the $< 101 >$ peak becomes dominant reaching a maximum at Doped10. For doping higher than 10%, no peaks are present, indicating that material is completely amorphous. To explain the progressive amorphization of the film depending on the $Al_2O_3$ insertion, it is important to consider that the crystallization along the c-axis ($< 002 >$) consists in an alternation of $Zn^{2+}$ and $O^{2-}$ columns and results in a charged surface, with positively and negatively charged terminations. The a-axis growth ($< 100 >$), instead, is determined by consecutive $Zn^{2+}$ and $O^{2-}$ rows and the surface is neutral [85]. During ALD growth, the single $Al_2O_3$ layer can disturb the energy of the surface by altering the charge balance of c-axis oriented crystals, determining a progressive relaxation of the vertical-aligned growth. The shift of the two XRD peaks is due

to a stress that can be attribute to the presence of $Al^{3+}$ ions which act as substitutional defects in the ZnO matrix. Considering that the $Al^{3+}$ ionic radius (54 pm) is smaller than the $Zn^{2+}$ (72 pm) a stretching along the a-axis due to these defects affects the d-spacing of the ions in the system and explains the $< 101 >$ shift to lower angles. The slight shift of the $< 002 >$ peak has been attributed by Yoshioka et al. [137] to the different coordination number of 5 for the substitutional $Al^{3+}$ ions, respect to the 6 of the $Zn^{2+}$ ions. Finally, no peaks related to meta-stable mixed compounds are detected, e.g. spinel $ZnAl_2O_4$.

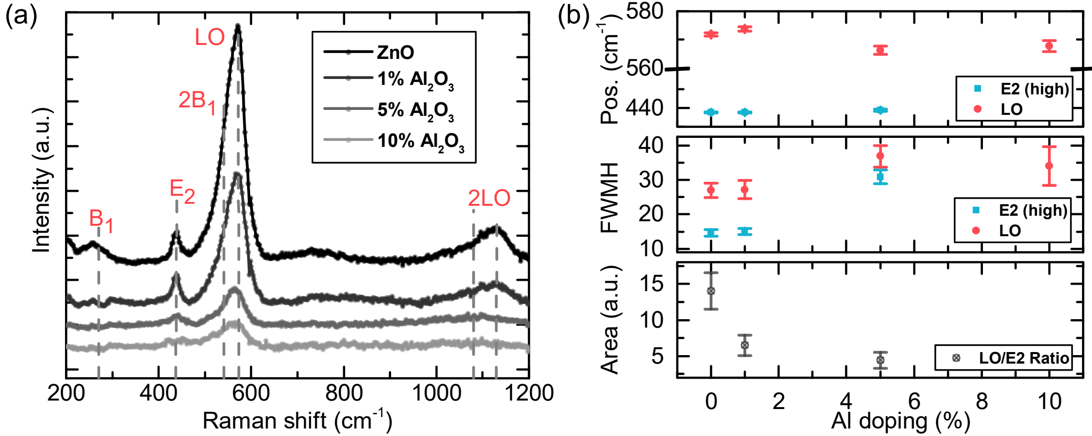


Figure 5.5: (a) Raman spectra for the pure ZnO and the AZO films; (b) The main peak position (top), their width (center) and the relative intensities (bottom) are reported. The values are extracted from the fit peak by lorentzian fit.

The observations extracted through SEM images and XRD patterns are confirmed by Raman measurements. Figure 5.5a reports the spectra for pure ZnO and AZO films (1%, 5%, 10% Al concentration). The peak at $\sim$437 $cm^{-1}$, representing the strongest mode in wurtzite crystal structure related to the $E_2$(high) mode, is evident only in the PureZnO and Doped1 samples. In the Doped5 the peak becomes very broad and weak, as an indicator of the fast amorfization of the film. Moreover, the small variation in the position of the $E_2$(high) peak and the increase in FWMH with doping (Figure 5.5b) are related to the stress due to the substitution of $Zn^{2+}$ ions by smaller $Al^{3+}$ ions [132]. The higher peak for the AZO films corresponds to the LO band one, given by the combination of $E_1$(LO) and $A_1$(LO) (583 $cm^{-1}$ and 574 $cm^{-1}$, respectively), which are commonly related to intrinsic defects in polycrystalline materials [138]. Also the silent modes $B_1$($\sim$275 $cm^{-1}$ and 575 $cm^{-1}$) are

a consequence of the breakdown of the traslational crystal symmetry and can be linked to defects and impurities[139]. The broadening and the intensity of the LO band are indicative of the change of oxygen stoichiometry inside the thin film [140]. In particular, $E_2$(high) and LO modes are oxygen-dominated vibrations, but they show an opposite trend with the absolute content of oxygen in the material. The intensity of the $E_2$(high) peak increases with oxygen content, while the intensity of the LO band decreases. Figure 5.5b reports the ratio of $E_2$(high) and LO intensities: a high value indicates an oxygen deficiency, while values lower than 1 correspond to a good oxygen-zinc stoichiometry. One can observe that the oxygen content inside the AZO films increases as a function of the doping, compensating the intrinsic defects of the pure ZnO via ALD.

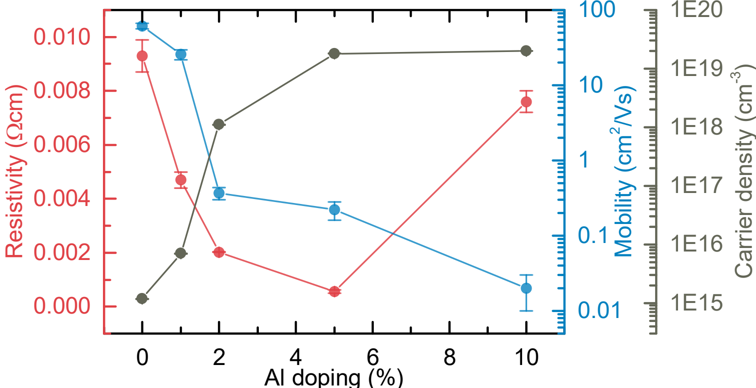


Figure 5.6: Resistivity, mobility and carrier density values for the 50 nm AZO films as a function of the $Al_2O_3$ content.

Finally the electrical properties of the AZO films are inspected by Hall measurements in Van Der Pauw geometry. To this purpose, AZO films were deposited on a 7x7 $mm^2$ glass substrate. On the edges of the square four Au 200 nm pods were deposited by thermal evaporation and used as electrodes for the four-probe contact. Figure 5.6 reports the resistivity ($\rho$), mobility ($\mu$) and carrier density ($n$) depending on the $Al_2O_3$ content of the AZO films. ZnO and AZO films are naturally n-type doped with a low resistivity, due to the intrinsic defects concentration. For the pure 50 nm ZnO film $\rho$ is $9\times10^{-3}$ Ωcm, while $\mu$ and $n$ values are 61 $cm^2$/Vs and $1.2\times10^{15}$ $cm^{-3}$. By $Al_2O_3$ insertion the resistance decreases, until a minimum value is reached at ~5% ($\rho$ =$5.6\times10^{-4}$ Ωcm), which is in line with previous reports [86,

134]. The $n$ value rapidly increases to reach a saturation at $2 \times 10^{19}\,cm^{-3}$, while $\mu$ decreases until a value of $0.02\,cm^2/Vs$ for the Doped10. The saturation of $n$ suggests that not all the Al atoms contribute to the creation of donor for high doping percentages. When $Al_2O_3$ layer concentration is below 5%, the small amount of inserted Al atoms mainly replaces Zn atoms at lattice sites as donors. While when the doping increases, the exceeding Al atoms result in the intra-grain congregation and grain boundaries segregation by forming $AlO_x$ suboxides [134, 141]. This defects are electrically inactive and can explain the trend of resistivity. Concerning the $\mu$ reduction, the dimension of the grain size is the main influencing factor. In fact, regarding the charge transport mechanism in poly-crystalline films, Ghosh el al. [142] report a linear relation between grain size and mobility. In addition, usually the increase of carrier concentration in semiconductor enhances the scattering, resulting in a $\mu$ reduction [141]. The $n - \mu$ correlation and the high density of carrier ($\sim 10^{18}/10^{19}$) are a confirmation of the degenerate semiconductor nature of AZO thin films.

## 5.2 Electrical properties of $ZnO_x$:$Al_2O_y$

The choice of the Cu TE and the 50 nm thickness for the active layer were determined by the study on ZnO-based memristors reported in Chapter 4, since Pt(200 nm)/ZnO(50 nm)/Cu(100 nm) exhibited the best performances.
The samples for electrical characterization in DC voltage sweep were fabricated using the shadow mask process described in Section 2.1. On a Si/$SiO_2$ wafer, a 200 nm Pt BE is deposited by sputtering using a 10 nm Ta adhesion layer. Then the wafer is sliced in 1x2 $cm^2$ dies. A 50 nm AZO active layer is grown by ALD on each die and partially etched in diluted HCl, in order to access the BE. As TE, a 100 nm Cu thin film is deposited by thermal evaporation and patterned through shadow mask.

### 5.2.1 I-V characteristic

The CF formation in ECM cells is determined by the anodic dissolution at the interface between the active electrode (Cu in this case) and the oxide when a positive bias is applied. The result is a metal cation diffusion from the active electrode

toward the inert one. Since the ion movement and electron mobility in the oxide layer are controlled by carrier density and film structure [21, 22], the addition of $Al_2O_3$ partial layers can be used to modulate the reduction process occurring during filament formation/rupture. Moreover, considering the high defect concentration in ZnO deposited via ALD, one should remember that also the intrinsic defects can have an active part in the switching dynamics. As described in the previous chapter (Section 4.2.3), the abundance of vacancies in as-deposited ZnO determines a competition between $Cu^{2+}$ and Vö in filament formation, which can affect the switching stability of Pt/ZnO/Cu devices, resulting in a short endurance and fast degradation. To understand the effect of $Al_2O_3$ incorporation, the 5% and 10% doped devices are tested in DC voltage sweep mode, with voltage applied on the Cu TE and grounded Pt BE. The results are compared with a pure ZnO sample. An initial forming procedure is performed at 3 V with a fixed current compliance, allowing the formation of a stable CF. In order to compare the device behavior the same $I_{cc}$ value is fixed during the switching operations at 7 mA, while the maximum applied voltage is selected for each stack to target the best electrical response. The I-V characteristics for the PureZnO, Doped5 and Doped10 are reported in Figure 5.7a-c, presenting a stable bipolar switching with SET operation in positive polarity and RESET in negative. For the PureZnO and the Doped10, 50 consecutive cycles are reported, while for the Doped5 only 30 cycles were achievable before final device breakdown. From the I-V curves, the switching parameters are extracted. The resistance state values (HRS and LRS) and the switching voltages ($V_{set}$ and $V_{reset}$ are plotted in Figure 5.7d-f and Figure 5.7g-i, respectively.
In order to visually examine the performances from the different stacks, descriptive statistic on resistance states, resistance ratio and voltages are reported in Figure 5.8a-c. Comparing the Doped5 with the PureZnO samples, the main visible effect of $Al_2O_3$ insertion is the closure of the operating window (Figure 5.8d), with the main contribution due to the decrease of HRS value from 1.5 kΩ for the reference sample to 0.4 kΩ for the doped one and a slight contribution due to LRS decrease from 70 Ω to 50 Ω. The decrease of resistance states is related to the combination of low resistivity and high carrier density, which characterize the low-doped samples. Taking in account the high abundance of donor (Zn and Al interstitial), we can assume that a large CF is formed through the migration of $Cu^{2+}$ and $O^{2-}$ ions in opposite directions. Therefore, consecutive cycles can determine CF rupture and

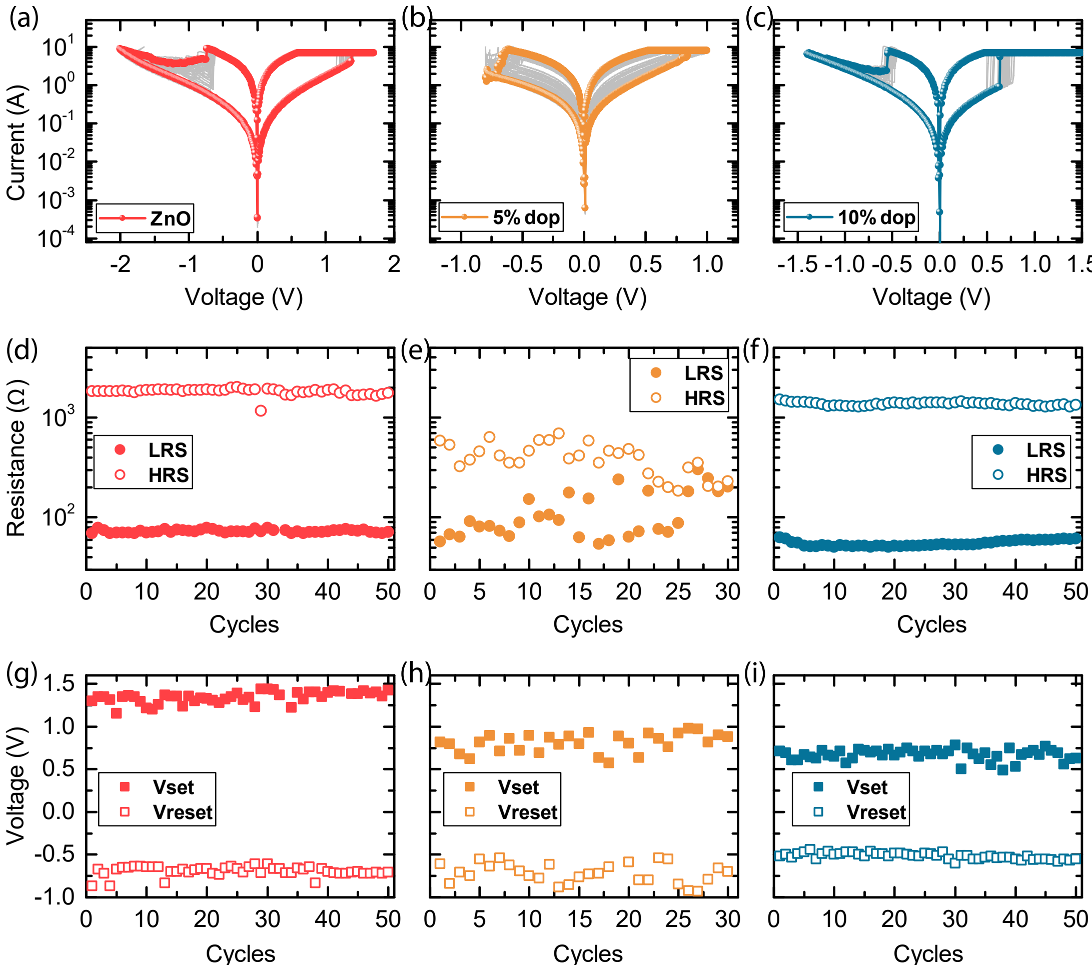


Figure 5.7: I-V characteristics in logarithmic scale for the PureZnO (a), Doped5 (b) and Doped10 (c) samples; all the device show bipolar switching with SET in positive voltage polarity and RESET in negative. HRS and LRS values, extracted by linear fit in the 0-0.1 V region, and switching voltages ($V_{set}$ and $V_{reset}$) for the PureZnO (d,g), Doped5 (e,h) and Doped10 (f,i).

reconstruction in different positions along the CF path, causing a fast deterioration of the device with the closure of the two states to an intermediate state at ∼200 Ω.

When the doping is sufficiently high to passivate the donor concentration, the result is an improvement of the switching performances. Comparable I-V curves are obtained for PureZnO and Doped10 with similar resistance window (Figure 5.8b). The visible improvement in Doped10 is the reduction of switching voltages: the $V_{set}$ decreases from 1.3 V for the pure ZnO to 0.67 V for the Doped10, while the $|V_{reset}|$

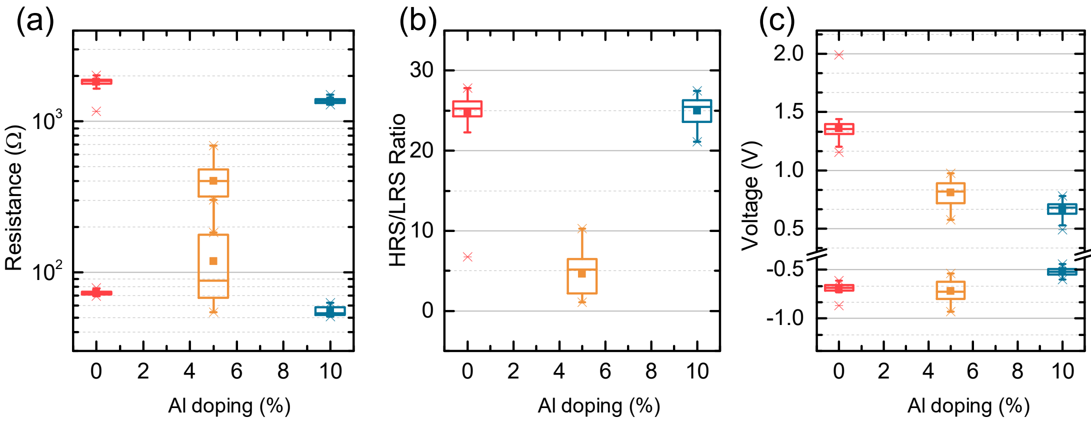


Figure 5.8: Descriptive statistic on resistance state values (a), HRS/LRS ratio, $V_{set}$ and $V_{reset}$ values depending on the $Al_2O_3$ doping. In the box plot, the horizontal lines correspond to the median, the first and third quartiles, the vertical line represents the 1%-99% range of values and the central dot is the mean value.

from 0.71 V to 0.60 V (Figure 5.8c). This improvement in power consumption can be attributed to the higher carrier density of Doped10. A comparison of the two RESET processes reveals that the PureZnO presents gradual current variation until $V_{stop}$ is reached, while the Doped10 is characterized by an abrupt current decrease in correspondence of $V_{reset}$. The sharp resistance change during RESET for the Doped10 is related to the presence of partial $Al_2O_3$ layers, which acting as localized barriers, are able to confine the CF filament. Moreover the current overshoot during RESET is slightly reduced from ∼9.5 mA to ∼9 mA as an effect of $Al_2O_3$ insertion.

### 5.2.2 DC endurance performances

Figure 5.9b,c compare the DC endurance performances for PureZnO and Doped10 devices. In order to optimize the switching, sweep amplitude and ramp are targeted for each stack. A clear improvement in device life-time is achieved as a result of $Al_2O_3$ insertion, making the ALD doping procedure an interesting technique to overcome the limitation of as-deposited ZnO thin films. It is worth noting that a crucial role in the endurance enhancement is related to the considerable reduction in device power consumption, determined by the decrease of switching voltage values (Figure 5.9a). Morover, Simanjuntak et al. [77] reported a better stability in

ECM devices as a result of the lower amount of pre-existing oxygen vacancies in ZnO-based memristors.

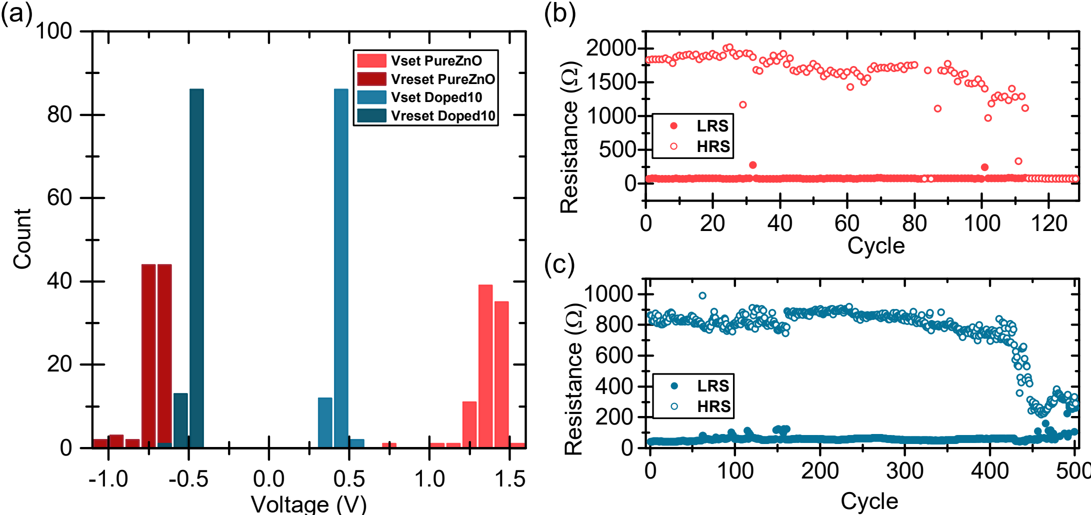


Figure 5.9: (a)Discrete distribution of $V_{set}$ and $V_{reset}$ over 100 consecutive cycles for PureZnO and Doped10. (b) DC endurance test for PureZnO; SET and RESET sweep of $0\,V \rightarrow 1.8\,V \rightarrow 0\,V$ and $0\,V \rightarrow -2\,V \rightarrow 0\,V$ respectively, and 10 s timing. (c) DC endurance test for Doped10; SET and RESET sweep of $0\,V \rightarrow 0.9\,V \rightarrow 0\,V$ and $0\,V \rightarrow -1.4\,V \rightarrow 0\,V$ respectively, and 2 s timing.

When the $Al_2O_3$ doping percentage is sufficiently high to partially compensate the ZnO native defect concentration, the electron conduction controlled by metallic bridge prevails on the one controlled by oxygen vacancies. The lower competition between ECM and VCM mechanisms leads to a better device stability and a longer life-time of the devices.

### 5.2.3 Switching Mechanism

In order to define the transport mechanism related to the switching of AZO films, two representative positive emi-cycles for PureZnO and Doped10 are plotted in $ln(|V|) - ln(|I|)$ scale and the curves are interpolated by linear fits [136], as reported in Figure 5.10.

The devices are initially in the HRS and the electrical conduction is properly described by the space-charge-limited conduction (SCLC) mechanism. In the low voltage region, where the I-V curves follow the Ohm's law (I$\propto$V), the conduction is

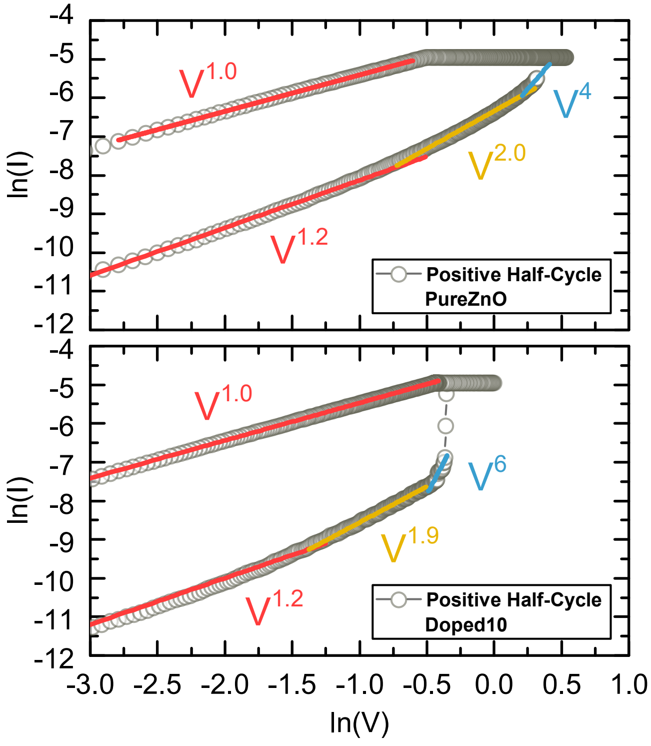


Figure 5.10: Representative I-V characteristics in ln(|V|) – ln(|I|) scale for the ZnOpure (top) and Doped10 (bottom); SCLC mechanism is confirmed in both cases by the three distinguishable regimes: Ohmic (red line), trap unfilled (yellow) and trap filled (blue).

dominated by the thermally generated carrier, while the number of injected carriers is low. With the voltage increase, the injected carriers are predominant and the SCLC typical quadratic I–V relation ($I \propto V^2$) is observed. In this region, which is governed by unfilled traps, the concentration of carriers related to the film defect is fundamental. The devices remain in HRS until the traps are completely filled by injected carriers and an abrupt current jump is observed. The filled trap region is characterized by a steep slope ($I \propto V^4$ for PureZnO and $I \propto V^6$ for Doped10). When the SET operation is completed, the LRS shows an Ohmic conduction regime, as it is proved by the slope of ∼1, coherently with the filamentary switching, where the current flows through the formed CF. Therefore, the conduction mechanism is the same for pure ZnO and AZO films, indicating that main carriers and conduction behavior are comparable, while the different carrier concentration and defect

distribution determine the observed dissimilarity in electrical responses.

The study of the electrical response of the $ZnO_x$:$Al_2O_y$ devices demonstrates that the performances of the ZnO-based memristors can be tuned by $Al_2O_3$ doping via ALD. In particular, by proper control of physical and structural properties of the AZO thin films, an improvement in DC endurance and power consumption have been observed. The conduction mechanism responsible for the switching in the AZO films remains the same as the one in pure ZnO, but the differences in defect nature, carrier density and mobility determine the dissimilarity in electrical response.

# Chapter 6

# Pt/$HfO_2$/Ti/TiN Memristors

**Reference paper**: *Analog control of retainable resistance multi-states in $HfO_2$ ReRAM* - paper submitted [143]

$HfO_2$ is a high-k dielectric been extensively used in ReRAM fabrication because of its interesting properties, including CMOS compatibility, large HRS/LRS ratio, good endurance and retention, multi-bit storage ability and high-speed operation ($< 10\,\text{ns}$) [48, 144]. The use of Ti buffer layer and TiN as electrode to improve the device performances and stability has been widely studied [145, 146]. In particular, the Ti functions as oxygen scavengers/oxygen reservoir, enhancing the $O^{2-}$ exchange at the interface with $HfO_2$. In 2011, Yu et al.[66] proposed a new electronic synapse based on a $HfO_x$/$AlO_x$ ReRAM cell, showing the great potential of $HfO_2$ to be used in the emerging neuromorphic technologies. Since then, HfOx-based synaptic devices have gained great interest in the scientific community, being employed in the realization of complex neural networks with different applications [147], such as speech or pattern recognition.

In this chapter, the properties of Pt/$HfO_2$/Ti/TiN are deeply investigated, starting from the DC characterization and the impact of $V_{stop}$ voltage and $I_{cc}$ limit on the device response (Section1). Then the AC stimulation results are reported, with a particular focus on the device performances in terms of multi-bit storage and

synaptic emulation (Section2). The study of internal filament formation/rupture and its correlation with the switching behavior of the device both in DC and AC modes are reported.

## 6.1 DC characterization

Stand-alone Pt/$HfO_2$/Ti/TiN ReRAM devices were fabricated on a Si/$SiO_2$ substrate, following the lithography process described in Section 2.1. The Pt BE is deposited by RF sputtering and patterned through standard lithography and RIE. Then, a Si-based passivation layer of 100 nm is grown by LPCVD and VIAs with the dimensions of 1 $\mu$m to 10 $\mu$m are patterned using photo-lithography and wet etching. A $HfO_2$ and a Ti layers are used as active layer and oxygen reservoir, respectively. The 5 nm $HfO_2$ film is deposited by ALD at 200°C, and the 3 nm Ti is deposited by DC sputtering at room temperature. Finally, a sputtered TiN layer is grown at room temperature as the TE without breaking the vacuum. TE patterning is done by means of photo-lithography and RIE process.

### 6.1.1 Device performances and C2C reliability

Pt/$HfO_2$/Ti/TiN devices are tested in voltage sweep mode with biased TE and grounded BE. Figure 6.1a reports the initial forming and the I-V characteristics for 50 consecutive DC cycles. A bipolar resistive switching is obtained, with the SET process in positive voltage polarity ($0 \rightarrow 2 \rightarrow 0$V) and the RESET in negative ($0 \rightarrow -2 \rightarrow 0$V). During forming and SET operations, $I_{cc}$ is fixed at 150 $\mu$A. From Figure 6.1a one can notice that all the RESET operations present a current overshoot, which in the case of forming cycle is 1.5 mA and then decreases to a value of $\sim 800\,\mu$A. The undesired current overshoot is intrinsic behavior of the ReRAMs and depends on: the series capacitance created by the contact, the transition voltage amplitude and the gap between the initial and the final (after SET) current values. The first factor can be controlled optimizing the test setup and the cell engineering, while the other two can be attenuated lowering the current compliance limit and the switching voltages. In this sense, the insertion of the Ti buffer layer and the reduction of current leakage by SiN passivation layer play an important role. In particular, the buffer layer acts as oxygen scavenging and facilitates the exchange

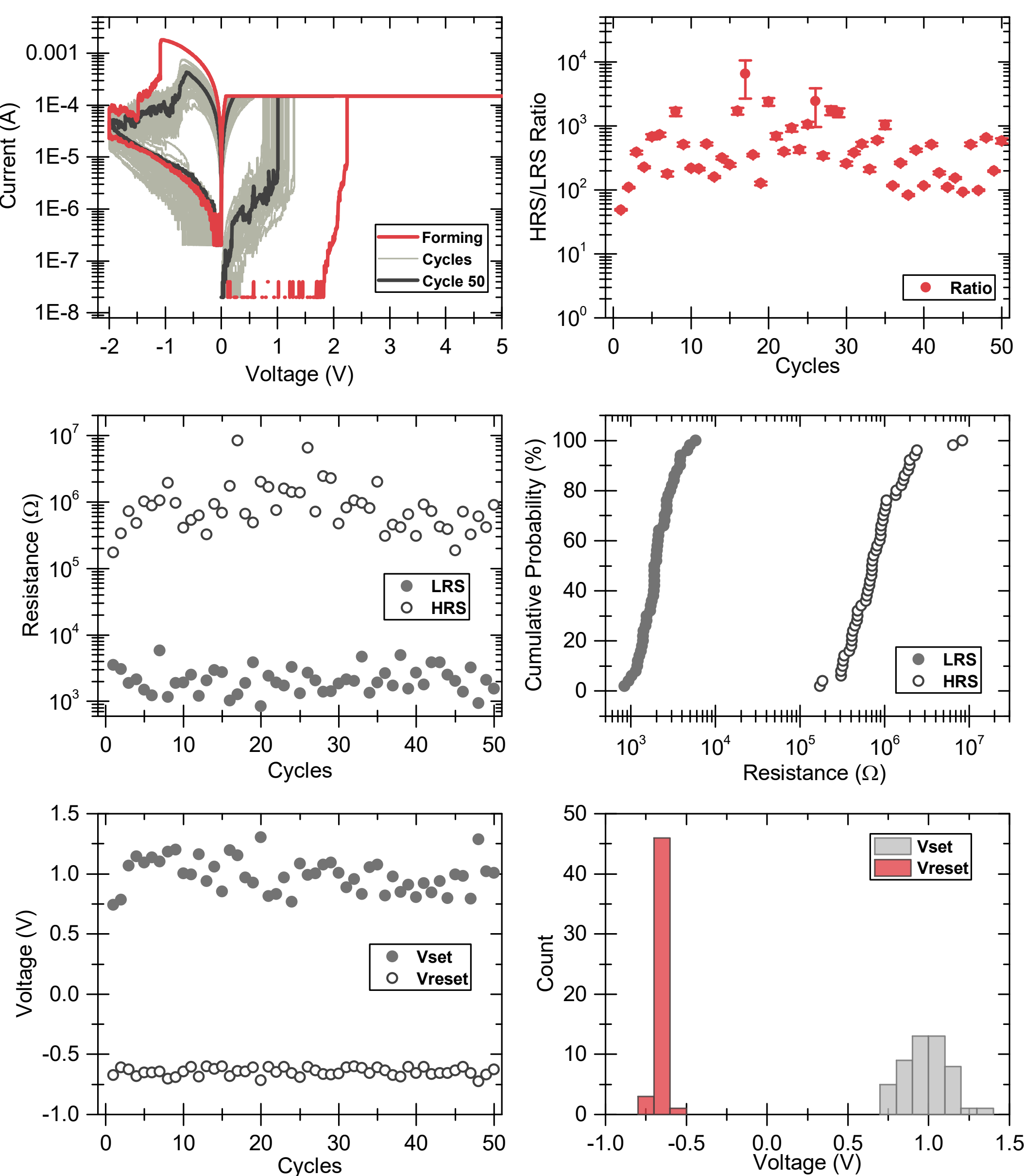


Figure 6.1: ReRAM performances by voltage sweep stimulation over 50 consecutive cycles: initial forming (red) and consecutive I-V cycles (grey) are reportes in (a), HRS/LRS ratio defining the device operating window in (b), LRS and HRS values measured between 0 and 0.1 V, their cumulative probability distribution in (c,d), $V_{set}$ and $V_{reset}$ voltage values and distribution in (e,f). For the measurement a 5 $\mu$m-VIA device is considered.

of oxygen at the $HfO_2$/Ti interface, reducing forming and switching voltages.

The response of the cell to DC sweep is evaluated by the extraction of switching parameters, i.e. HRS, LRS, resistance ratio, $V_{set}$ and $V_{reset}$, resulting in stable values over cycling and low C2C variability. The HRS value is in the range of ∼1.5 MΩ and LRS ∼3 kΩ over cycles with a HRS/LRS ratio higher than 600 (Figure 6.1b,c). The C2C variability is deduced by the cumulative probability distribution reported in Figure 6.1d, which highlights the higher HRS variation over cycling due to the internal kinetics of the RESET process. However the two states result highly separated and distinguishable. Figure 6.1e reports the switching voltages, which mean values are 0.99 V for the $V_{set\,mean}$ and -0.65 V for $V_{reset\,mean}$. The sharp distribution of the $V_{set}$ and $V_{reset}$ (Figure 6.1f) with respect to the mean values confirms the high device C2C reliability.
The I-V curves show a clear difference in the transient current during SET and RESET operations. A sharp change in current is visible in correspondence of $V_{set}$, while in negative polarity current gradually decreases. When a negative voltage is applied, the current increases until an abrupt change in correspondence of $V_{reset}$ is observed. Then the resistance starts to gradually decrease and a deeper HRS value is reached, depending on the negative voltage amplitude ($V_{stop}$). This asymmetrical behavior can be explained considering the different internal dynamics that occur during SET and RESET transitions. The SET process [11, 14, 15] begins with a nucleation step, in which the CF formation takes place by migration of $O^{2-}$ ions under the applied voltage, and continue with a growth step, resulting in an increase of the filament lateral size modulated by $I_{cc}$. When the CF is formed, the current is subjected to an abrupt increase until the $I_{cc}$ is reached. At this point, the circuit components for current limitation (i.e. transistor or resistance) regulate the voltage across the sample. Therefore, the LRS value depends on the filament size and can be modulated by $I_{cc}$, while is not influenced by positive voltage amplitude. On the other side the RESET transition shows a visible dependence on $V_{stop}$, since it is governed by electrical field and temperature [11, 16]. When the applied voltage is sufficiently high, the current flowing through the CF induces an increase of internal temperature by Joule-heating, which facilitates Vö-$O^{2-}$ recombination and determines a partial annihilation of the CF. Once the insulating gap is formed in correspondence of $V_{reset}$, the current is suddenly reduced and the temperature decreases. The result is a slow self-limiting carrier migration, which leads to a gradual increase of the gap dimension and HRS value. The maximum voltage value

defines the final HRS. Therefore, one can observe that the change of HRS during the RESET process is associated to the energy that is provided to the active layer, which is related to applied voltage amplitude and timing.

### 6.1.2 D2D reliability

The device to device variability (D2D) is inspected by DC measurements with the same voltage input stimuli on different devices. After an initial forming step at 5 V and 150 $\mu$A, 50 consecutive cycles with RESET at -2 V and SET at 2 V and 150 $\mu$A are performed for each device. The $V_{forming}$, $V_{set}$ and $V_{reset}$ values over cycling, the HRS and the LRS are evaluated. Figure 6.2 reports the descriptive statistic on 36 devices, 6 per each VIA dimension (1 $\mu$m, 2 $\mu$m , 3 $\mu$m , 5 $\mu$m and 10 $\mu$m).

No clear dependence of switching parameters on the VIA size is observed. Moreover, the good D2D reproducibility defines these devices as reliable candidates to be employed in the realization of new technology applications.

Table 6.1: Mean values ($\mu$) and standard deviation ($\sigma$) of $V_{forming}$, $V_{set}$ and $V_{reset}$, HRS and LRS values over cycling. The statistic is performed on 6 samples for each VIA dimension.

| **VIA diameter ($\mu$m)** | | **$V_{forming}$ (V)** | **$V_{set}$ (V)** | **$V_{reset}$ (V)** | **HRS MΩ** | **LRS kΩ** |
|---|---|---|---|---|---|---|
| 1 | $\mu$ | 2.4 | 1.0 | -0.72 | 3 | 5 |
| | $\sigma$ | 0.2 | 0.2 | 0.05 | 1 | 2 |
| 2 | $\mu$ | 2.38 | 0.83 | -0.66 | 7.3 | 4.1 |
| | $\sigma$ | 0.16 | 0.11 | 0.02 | 0.1 | 0.7 |
| 3 | $\mu$ | 2.36 | 0.8 | -0.64 | 1.9 | 3.2 |
| | $\sigma$ | 0.08 | 0.3 | 0.02 | 0.2 | 0.7 |
| 5 | $\mu$ | 2.25 | 0.92 | -0.66 | 2.5 | 2.8 |
| | $\sigma$ | 0.07 | 0.17 | 0.03 | 0.2 | 0.8 |
| 10 | $\mu$ | 2.20 | 0.96 | -0.65 | 6.4 | 3 |
| | $\sigma$ | 0.06 | 0.13 | 0.02 | 0.1 | 1 |

The influence of the device VIA diameter over the $V_{forming}$ is presented in Figure 6.3a. The graph shows a clear relation between the forming voltage and the device active area. When a positive voltage is applied to trigger the CF formation,

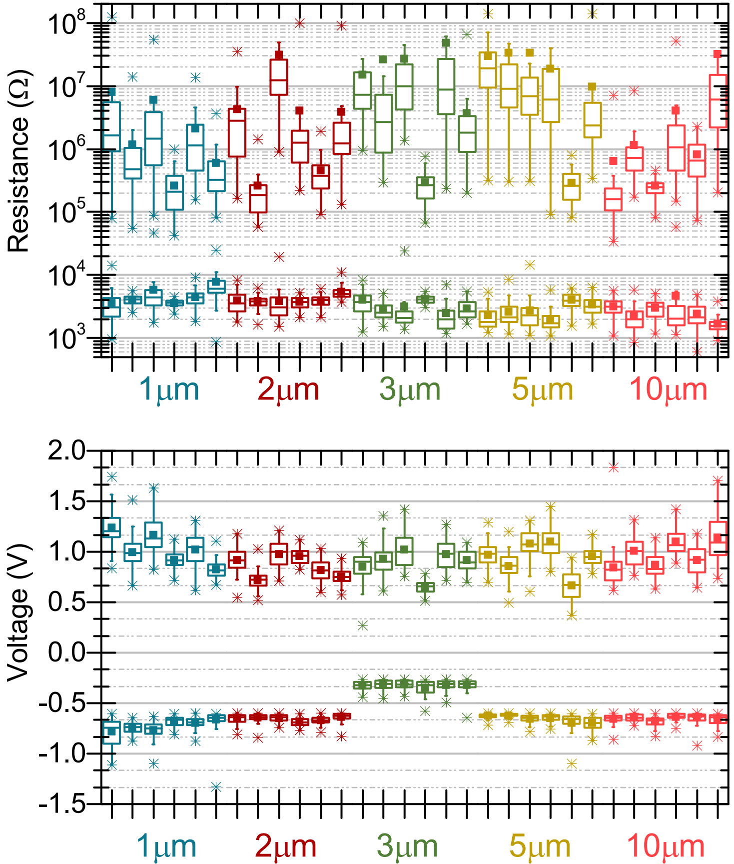


Figure 6.2: Descriptive statistic on 50 consecutive cycles for the values of resistance states (a) and switching voltages (b). The box plots sides represents the first and third quartiles, the square represents the mean value and the stars the 1% and the 99% of data.

different areas in which the concentration of Vö is higher start to grow. Among them only the first that connects the TE and BE becomes the CF, following the percolation theory [148]. It can be observed that the bigger is the device area, the higher is the probability that a vacancy clusters triggers the forming process. This is a statistical observation, independent of materials, oxide thicknesses and defect densities.

The Table 6.1 reports the mean values and standard deviations of the switching parameters for different VIA dimensions. The higher variation of HRS reported

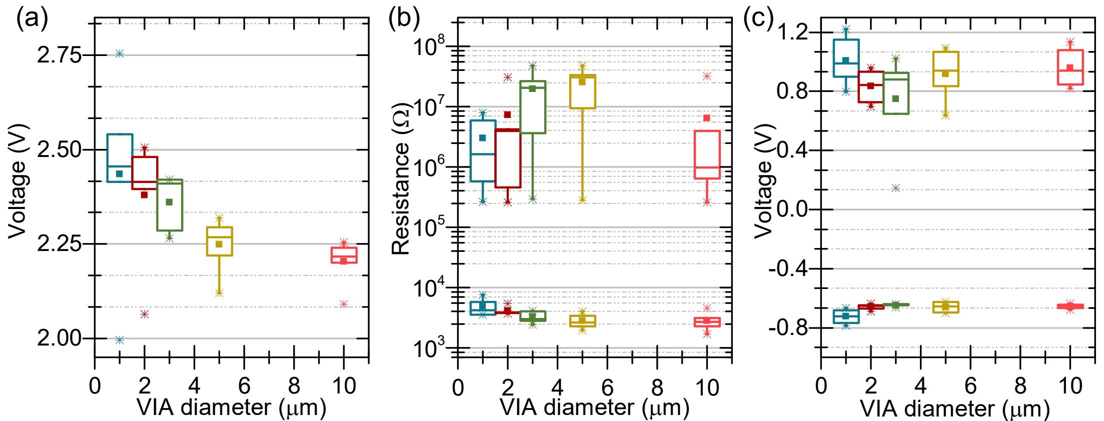


Figure 6.3: Forming voltages(a), resistance switching states (b) and switching voltages (c) depending on the device area; each point derives from the measurement on 6 devices.

in the devices with small VIA size is due to the increase of impurities in the fabrication process due to the reduction of device size, which make the process less controllable.

### 6.1.3 Resistance States Control by Voltage and Current modulation

The co-localization of storage and computing resources is an interesting property of memristor devices, which are nowadays studied for their logic-in-memory capability [149]. Several works report the attempt to modulate the resistance states by the control of the current compliance limit (LRS control) an the RESET voltage amplitude $V_{stop}$ (HRS control) [61–64, 150, 151]. The control of resistance states by tuning of the voltage sweep has been inspected for our devices. To this purpose, different DC I-V loops are performed varying the $I_{cc}$ from 150 $\mu$A to 950 $\mu$A with steps of 100 $\mu$A, and the $V_{stop}$ from -2 V to -1.3 V with steps of 0.1 V. For each parameter change, ten consecutive cycles are performed.
Figure 6.4 reports the device response to $I_{cc}$ modulation. The resistance can be tuned over 1 k$\Omega$ from ~3.23 k$\Omega$ for the lowest compliance value to ~1.16 k$\Omega$ for the highest (Figure 6.5), where the change seems to saturate. In order to increase the window of values in which LRS can be controlled, compliance limitations lower than 150 $\mu$A are needed, which causes an unstable (and often volatile) switching.

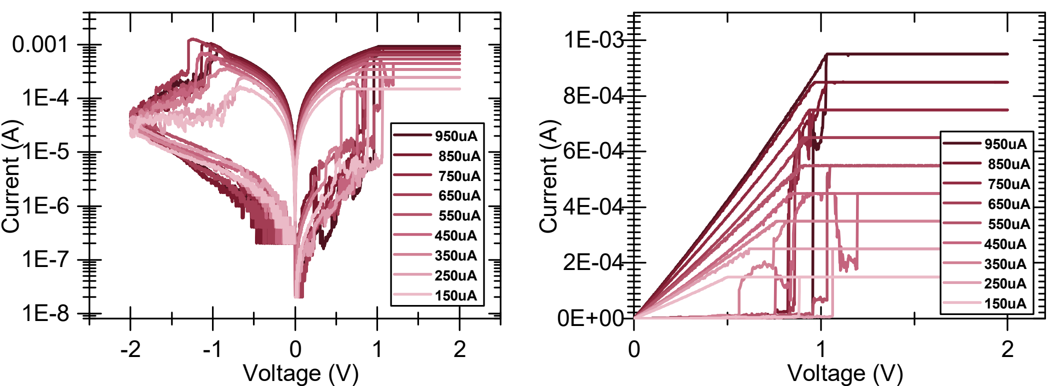


Figure 6.4: (a) I-V characteristics in logarithmic scale during current compliance variation (a representative cycle for each $I_{cc}$ is reported). During the measurements, $V_{set}$ and $V_{reset}$ are fixed at 2 V and -2 V; (b) I-V characteristics in linear scale of the positive emi-cycle for the different $I_{cc}$.

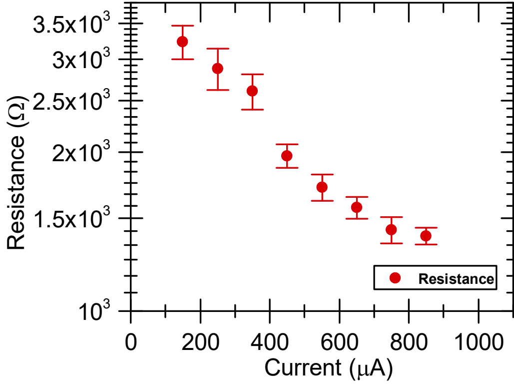


Figure 6.5: Trend of the LRS values as a function of the $I_{cc}$ limit;

Moreover, the LRS range of values is in the order of kΩ and increases the device power consumption significantly. Therefore one can observe that the control of multi-LRS states by current compliance is not efficient for our devices. A different behave can be observed by the modulation of $V_{stop}$ to control multi-HRS states. Figure 6.6a shows the I-V curves for the different $V_{stop}$ values. The HRS changes over three orders of magnitude from ∼30 MΩ, in correspondence of a $V_{stop}$ of -2 V, to 100 kΩ for -1.3 V $V_{stop}$. The $V_{reset}$ value remains constant at ∼-0.7 V, indicating that similar energies are required to break the filament, since the SET with fixed $I_{cc}$ defines similar CF dimensions in all the tests. The high impact of $V_{stop}$ on the

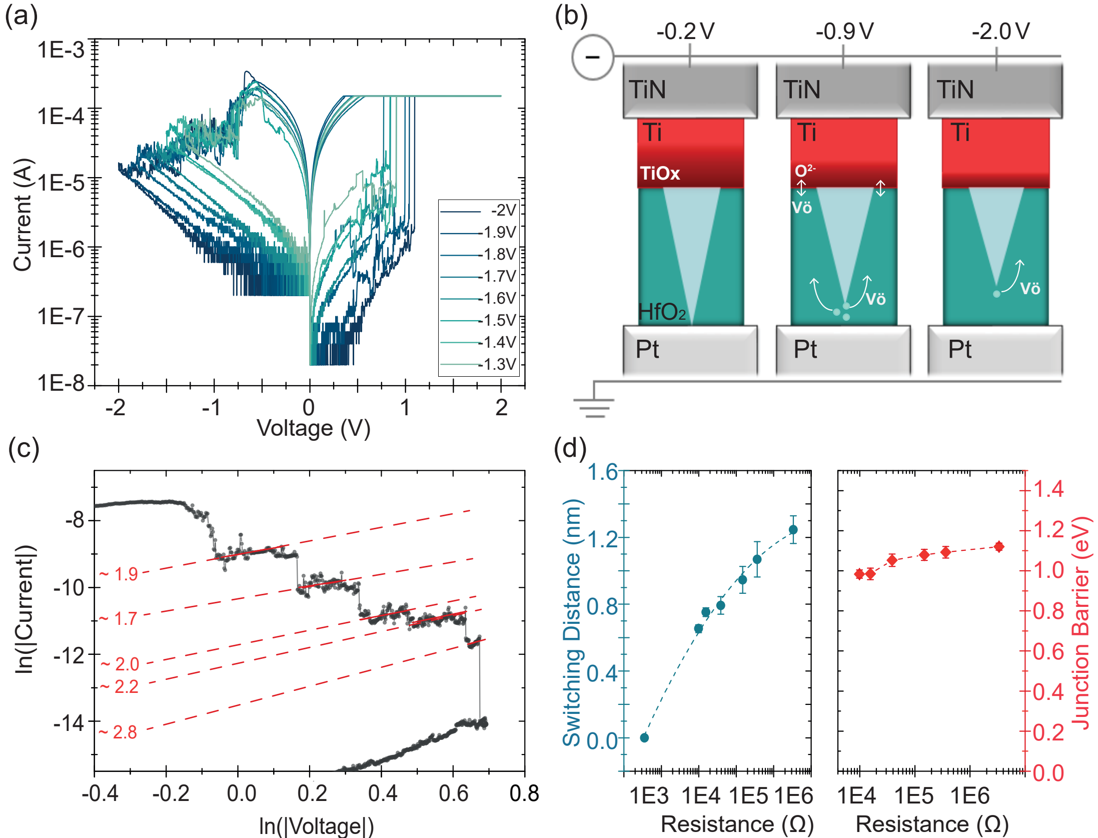


Figure 6.6: (a) I-V characteristic in logarithmic scale, a representative cycle for each $V_{stop}$ is reported, the positive voltage si fixed at 2 V with the $I_{cc}$ of 150 $\mu$A; (b) Graphical representation of the conduction mechanism and internal CF dynamics during RESET; (c) RESET semi-cycle in ln(V)-ln(I) scale for a representative cycle with $V_{stop} = -2$ V, the consecutive resistance states are interpolated by linear fit and the slopes are reported; (d) Switching distance (blue) and Pt/$HfO_2$ junction barrier (red) evaluation from Schottky-diode conduction mechanism formula. Figure from [143].

HRS tuning makes this relation particularly interesting to achieve multi-level controllable resistances. The link between internal behavior and electrical response is fundamental to achieve a good device control. A deep study of RESET dynamics in DC voltage sweep mode allows to understand the filament rupture kinetics and the transport mechanism involved in the switching.
Considering a device in its pristine state and applying a positive voltage, the Vö concentration at the Ti/$HfO_2$ interface increases, due to the oxygen exchange at the interface. In fact, Ti oxidation requires low energy, as it is confirmed by the $\Delta$G

energy of -883.3 kJ/mol [152, 153]. The $O^{2-}$ migration from $HfO_2$, assisted by the positive bias, defines the formation of a thin layer of $TiO_x$ in the interface region and of a conic-shape CF, where the rupture/built takes place at the interface with the inert BE[16]. The formation of a conductive path in the oxide alters the initial potential-barriers created by the junction of materials with different work functions [23]. The Ti/$HfO_2$ contact can be described as an Ohmic-like contact for the narrow potential barrier due to high Vö concentration, while the $HfO_2$/Pt is considerable as a Schottky-like contact, because of the narrow filament size and the high Pt barrier potential. Figure 6.6b shows a schematic representation of CF shape and evolution during the RESET. When a negative voltage is applied, the thin layer of $TiO_x$ starts to be reduced. The Vö-$O^{2-}$ recombine near the narrow CF side, until the filament breaks and the potential barrier at $HfO_2$/Pt interface increases. An insulating gap is created, which impedes the carrier transport through the oxide. To define the conduction mechanism responsible for charged carrier transport, the I-V characteristics in the negative voltage polarity are plotted in $ln(|I|)$-$ln(|V|)$ scale. Figure 6.6c shows a representative negative emi-cycle in which several multi-HRS are visible. Interpolating the different resistance states with a linear fit, the slopes are $\sim$2, revealing that the transport mechanism is attributed to the high number of injected carriers rather than the thermally generated carriers from the bulk oxide[154]. Among the electrode-limited conduction mechanisms, the plot in $ln(J/A^*T^2)$ - $\sqrt{V}$ scale and the fit of HRS reveal the best accordance with the Schottky model, described by the following equation:

$$J_{SD} = A^* \, T^2 \; exp \left[ \frac{-q(\Phi_B - \sqrt{qE \setminus 4\pi\epsilon_0\epsilon_r})}{kT} \right] \tag{6.1}$$

Where $A^*$ is corrected Richardson's Constant ($A^* = \lambda_r \cdot A_0 = 0.5 \cdot \frac{4\pi mk^2 q}{h^3}$ ($m$ is the electron mass), q is the elementary charge, $\epsilon_r$ is the oxide permittivity ($\epsilon_r = 25$ for $HfO_2$ [155]), T is the temperature during the switching operations [11] and $\Phi_B$ is the barrier height. The current flux is evaluated depending on the active area of the device defined by the VIA opening (5 $\mu$m) and the electric field is defined as $E = V/d_{SW}$, where the switching distance ($d_{SW}$) coincides with the gap height.

$\Phi_B$ and $d_{SW}$ are extracted from the linear fit, as:

$$\phi_B = -\frac{kT}{q}\, intercept \tag{6.2}$$

$$d_{SW} = \frac{q^3}{(kT)^2 4\pi\epsilon_0\epsilon_r}\frac{1}{slope^2} \tag{6.3}$$

An extended explanation of the fitting technique is reported in Appendix C.
In Figure 6.6d, the $\phi_B$ and $d_{SW}$ values are plotted as a function of the measured HRS at different $V_{stop}$. The potential barrier undergoes a small increase from ≃1 eV for HRS values in the order of 10 kΩ to 1.1 eV for HRS in the order of 10 MΩ. The constant value of barrier potential demonstrates that the resistance variation is determined by the CF evolution and not by a structural variation at PT/$HfO_2$ interface. The $d_{SW}$ increases proportionally to HRS from 0.6 nm for the -1.3 V $V_{stop}$ to 1.2 nm for the -2 V $V_{stop}$, as expected considering the dependence of the maximum applied negative voltage on the insulating gap dimension. The saturation in $d_{SW}$ trend indicates that the self-limiting migration occurs when the temperature decreases after RESET.

## 6.2 AC characterization

### 6.2.1 Endurance pulse measurements

The voltage stimuli duration can play an important role on the control of the switching resistance, since both voltage amplitude and pulse time contribute to define the energy provided to the system for the switching. In particular, passing from voltage sweep to pulses, the impact of time on the energy can alter the switching kinetics during RESET, resulting in partial not-retainable states. The impact of timing, positive voltage amplitude ($V_{pos}$) and negative voltage amplitude ($V_{neg}$) on the Pt/$HfO_2$/Ti/TiN devices is inspected by endurance pulse measurements (Figure 6.7). The endurance measurements consist of consecutive positive and negative writing pulses, in which the $I_{cc}$ is limited at 150 μA during SET operations, controlling the $V_{gate}$ of the external transistor (the setup is described in 2.2.2). The reading procedure is performed by a voltage ramp between 200 mV and 250 mV after two consecutive positive and negative pulses. The reading periodicity

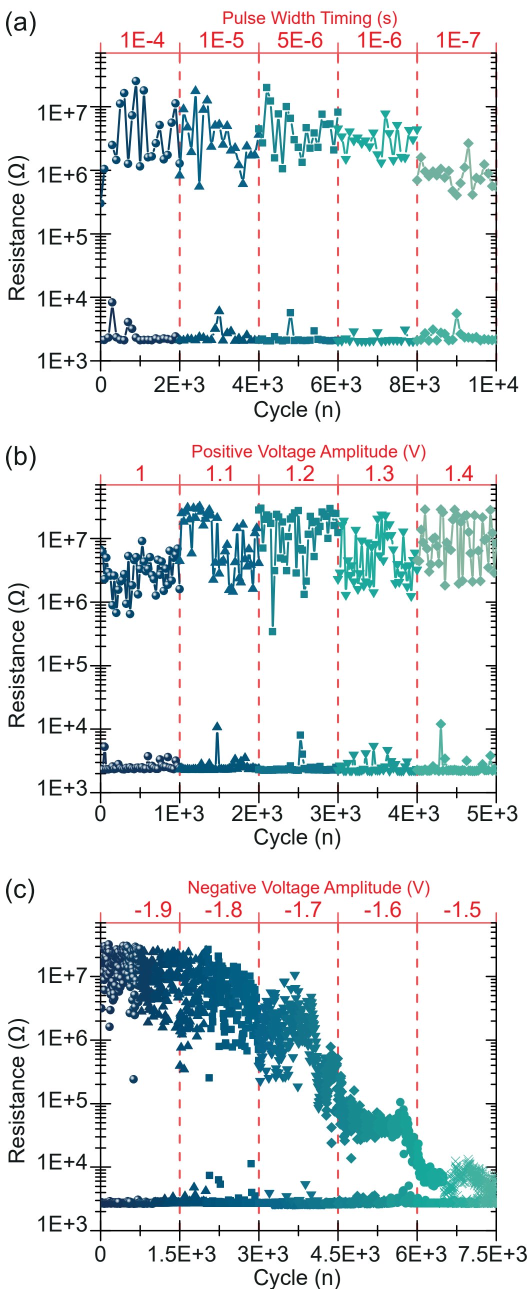


Figure 6.7: Pulse modulation effect on the resistance values: (a) Pulse width variation endurance: pulse width is decreased from 100 $\mu$s to 100 ns, reading every 50 cycles; (b) $V_{pos}$ variation endurance: $V_{pos}$ is increased from 1 to 1.4 V with 0.1 V steps and $V_{neg}$ is fixed -2V, reading every 50 cycles; (c) $V_{neg}$ variation endurance: $V_{pos}$ is fixed at 1.4 V and $V_{neg}$ varies from -2 to -1.4 V with 0.02 V steps, reading every 5 cycles. Figure from [143].

is defined by users. Figure 6.7a shows the impact of pulse timing on the HRS and LRS. During the test, the pulse width is varied form 100 $\mu$s to 100 ns with constant pulse slope of 20% $\times$ *width* and for each timing $2{\times}10^3$ cycles are performed with a reading periodicity of 50. The HRS and LRS do not show any remarkable dependency with respect to the pulse duration. However a slight HRS reduction at small pulse range ($\leq$100 ns) is visible, due to a pulse shape distortion caused by a parameter analyzer limit for fast pulses. In Figure 6.7b the effect of the amplitude of positive pulses is inspected. The pulse width and the $V_{neg}$ are fixed at 1 $\mu$s and -2 V respectively, while $V_{pos}$ varies from 1 V to 1.4 V. The resistance state trends are slightly influenced by the $V_{pos}$ change, as it was predictable by the SET internal dynamics. A strong impact of $V_{neg}$ on the HRS is visible (Figure 6.7c). For this measurement, the pulse width and the $V_{pos}$ are programmed at 1 $\mu$s and 1.4 V and $V_{neg}$ changes from -2 V to -1.3 V. Different distinguishable HRS multi-states in a wide operating window (30 M$\Omega$ - 10 k$\Omega$) can be achieved by the precise control of the pulse negative amplitude.
The high sensibility of HRS to negative voltage variations as small as $\Delta$V$\leq$-0.05 V and the low pulse to pulse variability make the HRS - $V_{neg}$ relation attractive for the fine control of stable and repeatable resistance multi-states. Therefore, this relation is further inspected.
To evaluate the repeatability of the multi-states, an endurance test is considered. During the test, a set of 250 cycles with a reading periodicity of 5 is performed for each $V_{neg}$ from -2 V to -1.3 V with steps of 0.05 V. The cumulative probability distributions for the 50 HRS for each $V_{neg}$ are reported in Figure 6.8a, showing low cycle to cycle variability, which decreases for lower HRS. The non-volatility of the multi-states programmed by pulses is proved by retention measurements for six intermediate states corresponding to -1.9V, -1.8 V, -1.7 V, -1.6 V, -1.5 V and -1.4 V (Figure 6.8b). The states have a good stability over time and no drift is registered in 2 hours of measurements. Moreover, the retention properties of the intermediate states do not show a dependency on the resistance value.
To study the filament evolution under the effect of negative pulses, the current during the negative pulses with different $V_{neg}$ has been measured. Figure 6.8c shows the current transient trend as a function of time. On the pulse rising, the device is in LRS and the current increases accordingly to the voltage amplitude until the RESET point is reached and it is subjected to a sharp change. One can notice that

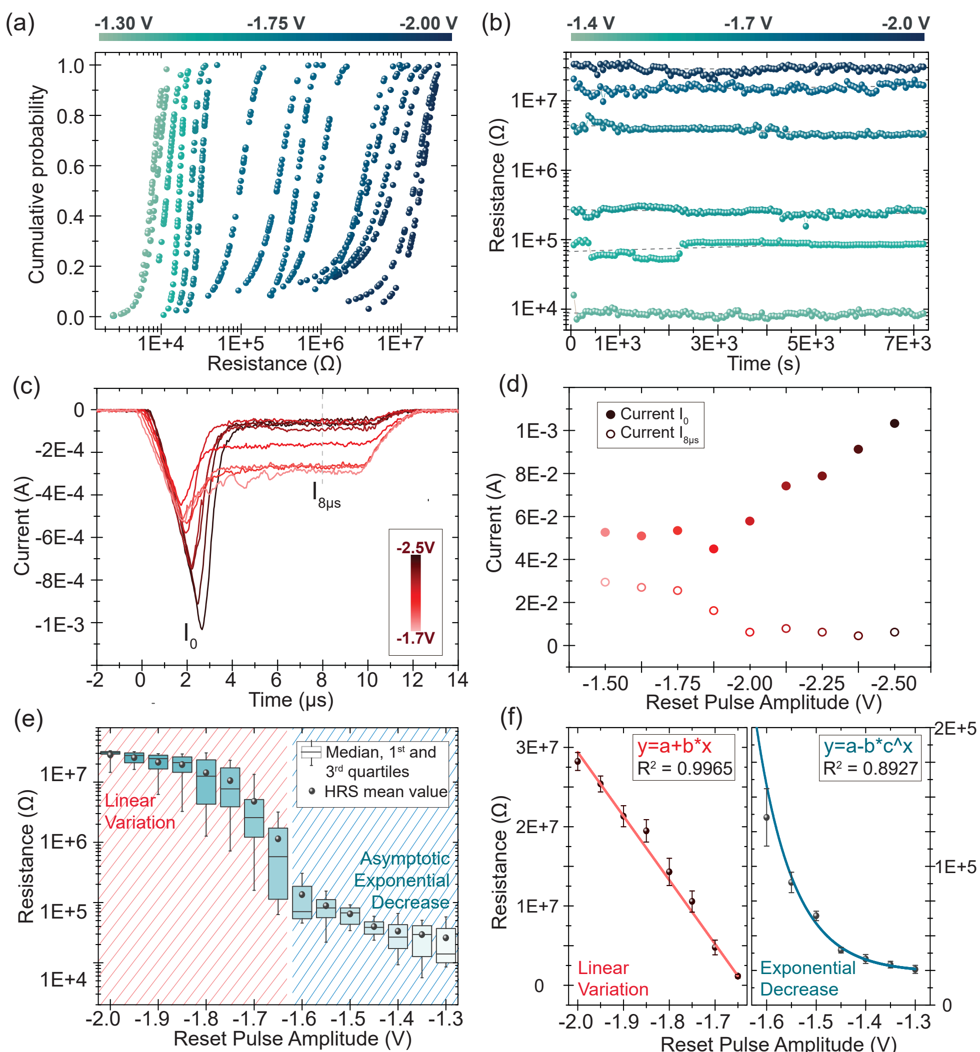


Figure 6.8: (a) Cumulative probability distribution, during the measurement V$_{neg}$ decreases from -2 V to -1.3 V and pulse width is fixed to 1 $\mu$s; (b) retention on 6 different HRS multi-states, reading is performed every 2 minutes; (c) current evaluation under different reset pulses, evaluated by the insertion of a series resistance in the testing setup (SI 1).The choice of 10 $\mu$s pulse duration is defined to minimize the parasitic effects which occur in the I measurement for faster pulses; (d) Trends for the maximum current ($I_0$) and the current after reset ($I_{8\mu s}$) measured in correspondence of 8 $\mu$s respect to the V$_{neg}$; (e) Descriptive statistics for 250 consecutive cycles for each V$_{neg}$, with a reading period of 5; (f) Mean values and relative errors for each V$_{neg}$ extracted from Figure (e). Two regimes are distinguishable: a linear trend (red) in the range [-2;-1.65] V and a decreasing exponential trend (blue) in the range [-1.6;-1.3] V. Figure from [143].

the $|V_{neg}|$ increase leads to a current change which is more abrupt and to a deeper HRS, while gradual resistance variation is visible in correspondence of pulses with small amplitude. In Figure 6.8d the currents $I_0$ and $I_{8\mu s}$ as a function of $V_{neg}$ are reported, where $I_0$ is evaluated as the maximum current reached during the pulse rise transient and $I_{8\mu s}$ is the current measured at 8 $\mu$s, when the RESET operation is completed. Since the RESET process is regulated by two main factors, which are temperature and electric field, it can be simplified in two consecutive regimes[13, 63]. During the early stage of RESET, the pulse rise determines a fast increase in temperature inside the filament, which is proportional to the current passing through the device. The maximum in transient current ($I_0$) shows a direct proportionality to the negative voltage absolute value, as it is visible in Figure 6.8d. The rupture point of conic shape filament in the thinner point and the gap formation are modulated by temperature. When the amplitude of pulses is small and the temperature does not reach high values, the ion lower diffusion determines a partial rupture of the CF, where a part of the Vö does not recombine and remains in the filament region close to the BE. The current passing through the partially ruptured filament remains higher also when the RESET operation is finished, as it is visible in the change of $I_{8\mu s}$, whose increase corresponds to the change of regime. When the thermal energy provided by the pulses is higher, a neat gap with fewer defects in CF area is obtained. The gap amplitude increases for higher $V_{neg}$ due the ion drift and the Vö- $O^{2-}$ recombination along the filament axis. From Figure 6.8d, one can notice that the current $I_{8\mu s}$ is initially high and a sudden decrease is registered when the gap becomes neat.

The HRS evolution trend as a function of $V_{neg}$ is inspected considering the endurance measurement represented by descriptive statistics in Figure 6.8e. Two different regimes in HRS gradual change are distinguishable: (i) a linear resistance variation in the $V_{neg}$ interval between -2 V and $\sim$ -1.65 V, in which the HRS passes from 30 M$\Omega$ to 100 k$\Omega$, and (ii) an asymptotic decrease from $\sim$ -1.6V to -1.3V, where the resistance tends toward 10 k$\Omega$. Figure 6.8f displays the linear and exponential fits performed on the mean value and relative errors extracted on 50 HRS values for each $V_{neg}$ data set.

### 6.2.2 Trains of ramping pulses

Taking advantage of the precise control of resistance by negative pulse amplitude modulation, the plasticity properties of our devices were tested by pulse train stimulation. In biology, long-term changes in synaptic strength (plasticity) involve the migration of $Na^+$ and $Ca^{2+}$ ions by electrochemical reactions due to the neuron excitatory and inhibitory spikes [156]. In this case, instead, the resistance change takes place through the modulation of the CNF gap inside the $HfO_2$ by $O^{2-}$ ions migration under electrical stimuli. In order to test the synaptic ability of the devices, depression is performed through a train of pulses with increasing negative amplitude from -1.2 V to -2 V with step 0.01 V (81 pulses in total), while potentiation is performed by applying a positive pulse of 1.4 V. After each pulse the resistance is measured by a reading ramp at 0.1-0.15 V. A scheme of the input stimuli for a depression-potentiation cycle (DPC) is reported in Figure 6.9a. The input parameters, i.e. $V_{neg}$ interval, consecutive pulse steps and number of pulses, are targeted to obtain the best resistance modulation. The device response to a DPC cycle in Figure 6.9b shows an analog modulation of resistance during the depression step and a digital control for the potentiation one. To study the DPC to DPC variability, 100 consecutive DPC are performed, for a total pulse number of $8.2\times10^3$. Figure 6.9c shows the first six DPC, to provide a visual estimation of the response change over time. The impact of consecutive programming cycles is quantitatively analyzed by the evaluation of data dispersion around the average resistance on 100 reading from consecutive depressions. Descriptive statistic is used to present the data distribution in Figure 6.9d. One can notice that the minor resistance variability is recorded in the region between pulses #65 and #81. In this region, which corresponds to the $V_{neg}$ interval of $< 1.85; -2 >$ V, the maximum gap dimension is reached, as it is suggested by the saturation of the resistance value. In order to define the number of distinguishable states in the programming window, taking in account the DPC to DPC variability and the noise in resistance modulation, the resistance variation between two consecutive pulses is evaluated as $\Delta R = R_{pulse_i} - R_{pulse_{i-1}}$. During the depression, the higher pulse to pulse variability is registered in the 10-20 MΩ region (Figure 6.10a). For higher resistance values $\Delta R$ starts to decrease, when the resistance saturation region is reached. The resolution between different resistance states of our devices is considered as the maximum obtained$\Delta R$ variation,

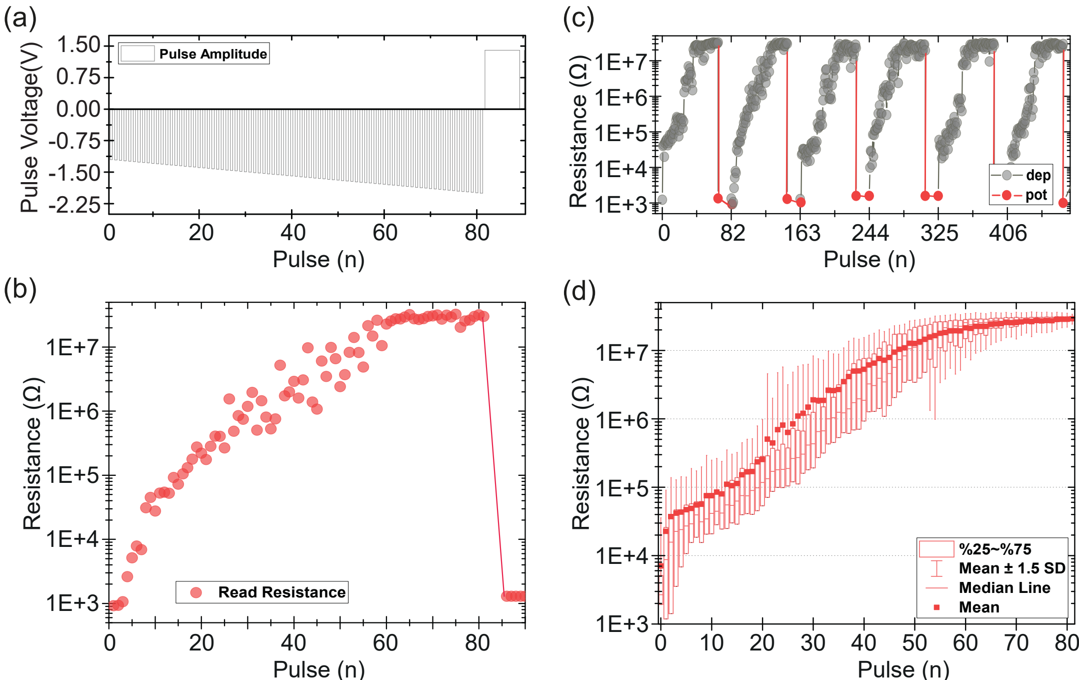


Figure 6.9: (a) Schematic representation of the voltage stimuli used for a DPC, consisting in 81 negative pulses ($V_{neg}$ from -1.2 V to -2 V with step 0.01 V and pulse width of 1 $\mu$s) and one positive pulse ($V_{pos}$ of 1.4 V and pulse width of 100 $\mu$s); (b) Example of resistance gradual control during the DPC, reading is performed after each pulse; (c) First six representative consecutive DPCs of the 100 cycles used in fig. (d); (d) Statistical analysis on 100 DPC, for a total of 8.2*$10^3$ consecutive pulses. In the box plot graph, the red squares represent the mean values, the vertical bar is related to the standard deviation, the horizontal central lines correspond to the median and the edges of the box to first and third quartiles. Figure from [143].

which corresponds to a value of 2 MΩ. Therefore, considering a resistance window of ∼30 MΩ, minimum 15 significantly distinct resistance levels are achievable. However, this methods provides a conservative estimation and can be improved by further calculation in order to reduce the discrete level size, increasing the number of significantly different states[127].

Figure 6.10b provides a comparison between the resistance and conductance trends as a function of the pulse number in linear scale. On the graph a distribution of resistance values in three regions is reported, corresponding to different regimes in accordance with the proposed pulse CF kinetics: (i)the sub-threshold region, in which the filament rupture is partial and the resistance decrease slowy, (ii) the

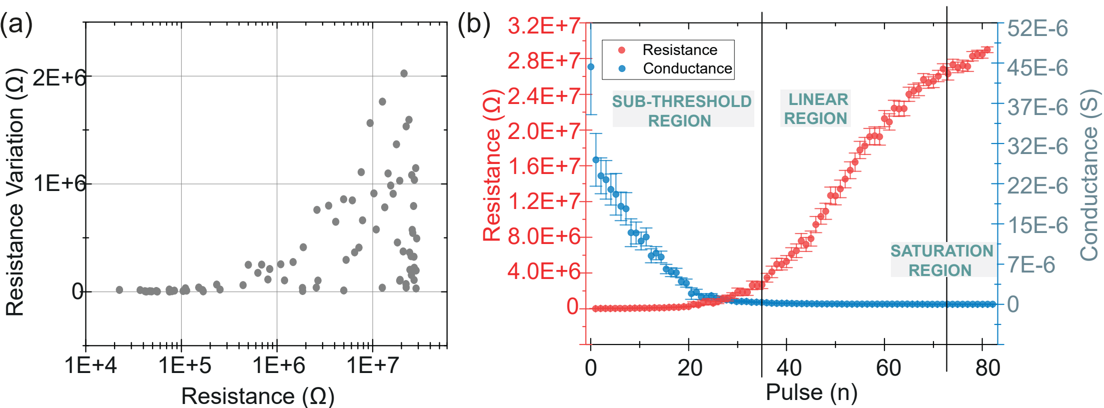


Figure 6.10: (a) Resistance variation ($\Delta R$) as a function of the read resistance ($R_{pulse_i}$) on the resistance mean values over 100 consecutive DPCs; (b) Resistance (red) and Conductance (blue) trend in linear scale; the sub-threshold, linear and saturation regions are indicated. Figure from [143].

linear region, where CF rupture is complete and the gap increase under the effect of the electric-field, (iii) the saturation region, when the gap dimension reaches its maximum value. The resistance sub-threshold region is particularly interesting for the conductance trend: the highest density of discrete conductance levels is visible, in accordance with the correspondence between fine analog conductance control and dimension of the programming window. Several works [127, 157] underline that the number of discrete conductance states is inversely proportional to the dynamic range of variation. In the sub-threshold region (resistance window of $10^2$), the conductance presents a linear variation, which is a fundamental request to obtain robust learning algorithms for ReRAM-based neural network applications [52, 158]. In fact, the presence of a linear dynamic before conduction saturation determines an increase of the distinguishable state interval. In the linear region, the resistance varies from 2 MΩ to 26 MΩ covering more than 10 different resistance states, while the conductance reaches the saturation value. The control of CF gap dimension defines a linear resistance modulation in this region, where the defined states can be used for multi-bit storage and computing.

### 6.2.3 Train of identical pulses

The device resistance modulation can be achieved also by trains of identical pulses, controlling the number of pulses and the voltage amplitude. For our devices the timing of pulses is fixed at 1 $\mu$s wit 20% slope, since the electrical response is not influenced by the pulse time and the used setup does not allow faster pulses without shape distortion. The main advantage of the pulse train stimulation is that an analog resistance modulation can be achieved during both depression and potentiation operations. This enable the online training of neural networks via bidirectional updates. However, the asymmetric behaviour of the device in response to positive and negative polarity is still an open issue [157].
To investigate the resistance gradual change, the device is firstly programmed in a determined resistance state and then a train of negative (depression) or positive (potentiation) pulses are sent to the cell. Each pulse is followed by a read operation (ramp between 0.1 V and 0.15 V). Some test monitoring resistance before and after each pulse with a ms pulse delay between consecutive pulses has been performed, to ensure that the pulse induces a resistance change which is retainable at least for a short time ($\sim$ 100 ms) and without drifts of resistance after the stimulus. Long retention test still need to be addressed.
The range of operating pulse amplitude has to be lower than the one used during pulse endurance in order to target a partial RESET (SET) operation, since the input pulse must be outside the binary resistive switching domain. The input stimuli should carry enough energy to induce a change, but not enough to obtain an abrupt resistance variation. In the intermediate range of voltage values ($V_{neg} \leq$-1.2 V and $V_{pos} \geq$1.1 V), between no resistance change and abrupt variation, the gradual control of resistance is strongly dependent on the voltage amplitude in both the polarities as it is visible in Figure 6.11, where a 0.05 V variation induces a considerable change in weight modulation. The figure reports repeated 50-pulse potentiations (Figure 6.11a,c) and 50-pulse depressions (Figure 6.11b,d) for different voltage amplitudes. After each operation the device initial conditions are restored and the test is repeated. Each test is leaded on a pristine device, in order to not consider the influence of the device ageing or the internal changes (CF shape and defects density) due to previous measurements. The devices show a resistance variation between 2 k$\Omega$ and 20-30 k$\Omega$, with an operating window of $\sim$10, which corresponds to a conductance window in the region of $\sim$10-80 mS. The conductance

value saturates after a certain number of pulses and then it oscillates around the saturation value.

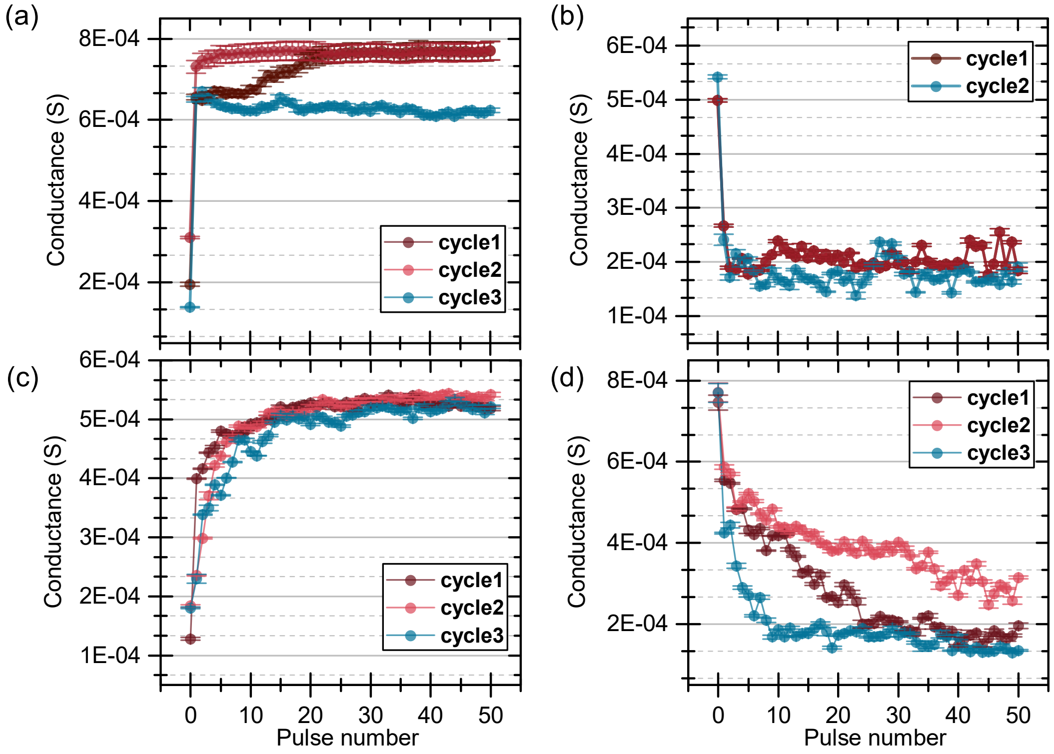


Figure 6.11: Consecutive potentiation achieved by a train of 50 pulses at 1 V (a) and 0.95 V (c). Consecutive depression achieved by a train of 50 pulses at -1.15 V (b) and -1.10 V (d). The four measurements are referred to four different cells and after each potentiation/depression the device is brought back to the initial resistance value.

One can observe that in both the polarity the conductance modulation is not locally monotonic. The conductance fluctuations are the result of the intrinsic device stochasticity. In correspondence of a $V_{pos}$ of 0.95 V, the best conductance gradual increase is achieved in terms of number of different conductance states and stability over different pulse trains. But the non-linearity of the measurements and the fast degradation need still to be addressed. Although it is well known that SET process is more difficult to be controlled, we believe that the limitation of our measurement setup could play an important role in the device degradation and pulse precise control. In particular, a better compliance control and the definition of a

different reading procedure are crucial to improve the measure quality and precision. Concerning the depression procedures, two main aspects have to be observed. On one side, conductance modulation shows an higher variability compared to the potentiation one, due the the randomicity related to the RESET kinetics, which involves a partial filament rupture driven by internal temperature. On the other side, taking advantage from the CF modulation by proper voltage control, a linear conductance variation can be achieved during depression operations.

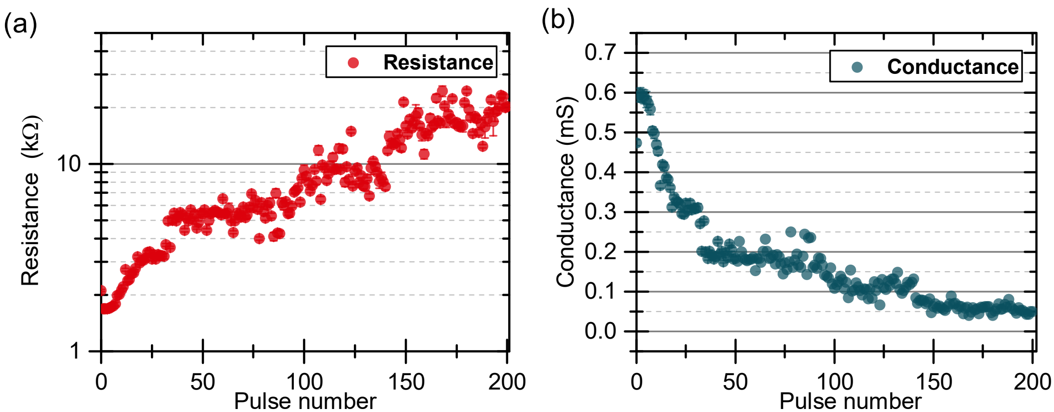


Figure 6.12: Linear resistance (a) and conductance (b) modulation obtained by a train of 200 pulses with amplitude of -1 V.

Figure 6.12 reports a linear conductance modulation obtained by a negative train pulse of -1 V amplitude. In order to complete the depression procedure and reach the conductance saturation value, the number of consecutive pulses is increased to 200. An extremely controllable linear conductance modulation is achieved.
A more accurate study on the device performances under applied train pulses is still required, in order to solve the asymmetrical behavior of the device in response to negative and positive stimuli. Moreover stability of the parameters and variability due to consecutive programming have to be inspected.

### 6.2.4 Crossbar structure

The on-going extended studies on the systematic stimulation through pulse trains are performed on a different device geometry. Unselected crossbar structures have recently shown great performances. Choi et al. [50] presented a $Ta_2O_5$-based passive crossbar array (9x2), employed into the pattern recognition through online

unsupervised learning by a generalized Hebbian algorithm. The main advantages of the crossbar structures are the parallel testing of different cross-point and the many applications in neural-network circuits.
Unselected crossbar structures were fabricated on a 4 inches Si/SiOx wafer with different TE-BE dimensions. The process followed for crossbar development, takes inspiration from the lithography process described in Section 2.1. The main fabrication steps are reported in Figure 6.13b. The reduced dimensions of the lines (connection lines are 4 $\mu$m wide and cross-point lines are 8 $\mu$m) have been selected as a compromise between the resistivity increase and the leakage current control (Figure 6.13a,c). The SiOx passivation layer is employed to reduce the leakage and pattern the device active ares through 3 $\mu$m VIA.
The crossbar single cells are firstly tested in DC voltage sweep, following a standard procedure (electro-forming + 50 cycles), which allows the formation of stable CF with repeatable rupture/formation procedures over cycling. The forming is a peculiarity of these devices and consists in consecutive sweeps with increasing I$_{cc}$ from 300 nA to 10 $\mu$A (Figure 6.14a). Using this special technique the first CF formation is achieved at a low voltage ($\leq$2 V), which is an essential constrain for the reliability of selector-free crossbar arrays. Moreover the procedure avoids high snake currents, which can cause the breakdown of the passive crossbar structure. In Figure 6.14b,c, the DC performances of the device are reported. In particular Figure 6.14b shows 50 consecutive DC cycles for a crossbar cross-point, performed at $0 \rightarrow 1.2\,V \rightarrow 0\,V \rightarrow -1.8\,V \rightarrow 0\,V$, with SET in positive polarity at ~0.9 V and I$_{cc}$ of 150 $\mu$A, and RESET in negative at ~-0.9 V. Due to the reduced dimension of the crossbar line and the higher TE resistance in comparison to the single-cell devices, the operating window results slightly reduced, with an LRS of 5.5 k$\Omega$ and HRS of 560.6 k$\Omega$. However the resistance window is still higher than 100. The distribution of the resistance states and the switching voltages extracted from DC cycles are reported in Figure 6.14c.
In pulse mode, the writing operations are performed by 1 $\mu$s pulses, which is the fastest reliable pulse timing in our testing setup, while reading is performed with user defined periodicity by a voltage ramp between 0.1 V and 0.15 V. Figure 6.14d,e report a retention test on three different resistance states and a representative pulse endurance test, consisting in 2k writing cycles with reading periodicity of 100. Although a slight drift in HRS, caused by the lower energy provided to the system

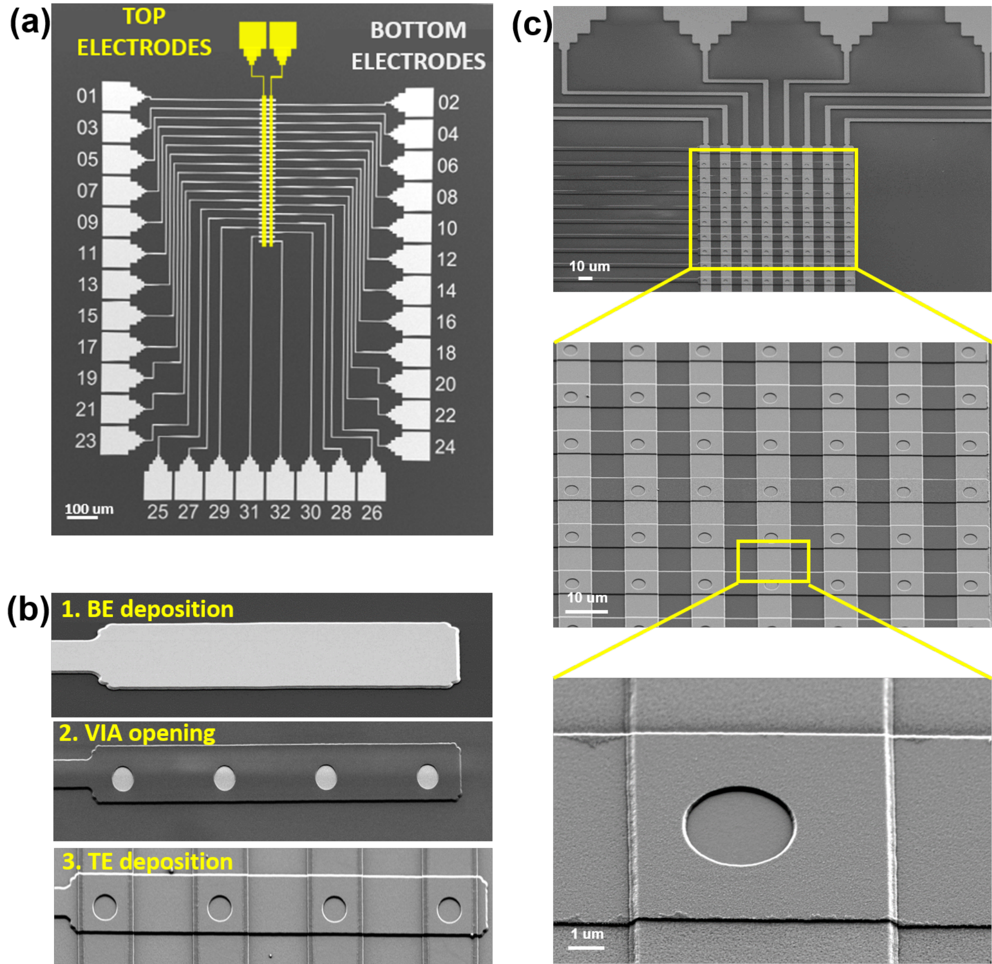


Figure 6.13: (a)SEM top view image of a 32x2 crossbar structure; each connection line is 4 $\mu$m width and the cross-point area is 8 $\mu$m, while the opened VIA have a diameter of 3 $\mu$m. (b)Process flow main steps by SEM imaging: BE deposition, passivation layer deposition and VIA opening, and TE deposition are presented for a 4x4 structure. (c) SEM magnification for a 32x4 structure. A part of the figure is taken from [159].

in the pulse mode is observed, the operating window is still higher than 10 and no failure is registered as it is proved by the bit error rate (BER) test (Figure 6.14e). Concerning the pulse train for analog resistance control, the best device response is obtained for pulse voltage amplitudes of 1.1 V and -1.5 V for potentiation and depression respectively. Each potentiation (depression) cycle consists of 100 consecutive pulses, with a reading periodicity of 5. The mean values and correspondent errors for the gradual increase and decrease in conductance for 20 consecutive DPC

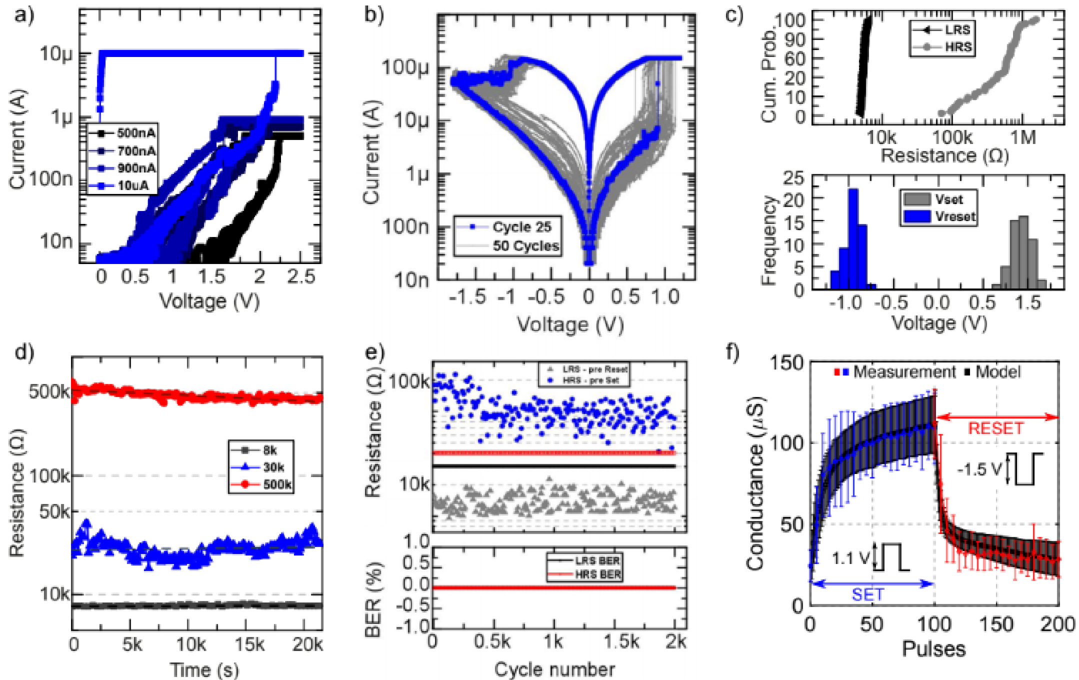


Figure 6.14: (a) Forming procedure for ReRAM cell, consisting in four consecutive steps. The compliance current Icc is progressively increased in order to avoid device break down; (b) I-V characteristic for 50 consecutive cycles in DC voltage sweep (0→1.2 V→0→-1.8 V→0), with the positive SET voltage of 0.92 V and negative RESET voltage of -0.92 V. During SET, the $I_{cc}$ is limited at 150 $\mu$A. LRS and HRS are measured at 0.25 V resulting in 5.5 kΩ and 560.6 kΩ; (c) Switching performance on 50 consecutive cycles. Cumulative probability distribution for HRS and LRS (upper panel). Frequency count of RESET and SET voltages (lower panel); (d) Retention measurements for three different resistance states. Reading is performed every 2 min; (e) Pulse endurance measurements on crossbar array over 2,000 cycles ($V_{pos}$: 1.2 V, $V_{neg}$: -1.8 V, $V_{gate}$: 1.9 V, width: 1 $\mu$s, slope: 20%); (f) Incremental weight updates. Average conductance values for 10 SET (100 pulses at 1.1 V, 1 $\mu$s) and RESET (100 pulses at -1.5 V, 1 $\mu$s) and the corresponding model fit. Reading performed every 5 cycles during the measurements. For the model, a linear interpolation is assumed to represent the missing reads. Adjusted from [159].

are reported in Figure 6.14f. Figure 6.14f also displays the fitting model for the curves, developed by the research group of professor Evangelos Eleftheriou (IBM Research, Zurich). They employed the potentiation and depression curves for the study of the in-situ learning of hybrid neuromorphic systems [159].

However, as it is noticeable from Figure 6.14f, some problem in conductance modulation still need to be addressed, as the linearity of the conductance change and the number of distinguishable states. Moreover, an improvement of the testing setup, which includes a dedicated test-board able to reduce the timing of the pulses and to limit the current compliance on chip, would determine device better performances.

# Chapter 7

# Pt/$HfO_2$/W Memristors

**Reference paper**: *Switching kinetics control of W-based ReRAM cells in transient operation by interface engineering* - paper submitted [160]

CMOS compatibility and low work function make Tungsten an interesting candidate to be employed in ReRAM electrode fabrication. Although the W low work function facilitates the resistive switching, resulting in lower power consumption and better device reliability [161], this metal has an intricate correlation with oxygen. The W oxidation encompasses a large variety of different oxidation stages, including $WO_2$, $WO_{2.72}$, $WO_{2.90}$, $WO_{2.96}$ with different Gibbs free energy ($\Delta$G), until the thermodynamically stable $WO_3$ oxide is formed ($\Delta G$ = -750 Kj mol$^{-1}$) [162, 163]. Moreover, W has smaller oxidation energy compared to low-work function electrodes (e.g. Ti and Hf) and it requires higher initial driving force to form a stable CF during the forming procedure [34]. Therefore, to benefit from chemical and electrical properties of W electrodes, these issues have to be addressed.
In this chapter, the resistive switching phenomenology of W-based ReRAMs is inspected. The improvement of switching performances is obtained by nano-scale engineering of W-$HfO_2$ interface through the insertion of $Al_2O_3$ barrier or Ti oxygen scavenging layers. In the first section the device performances in DC are tested, comparing the Pt/$HfO_2$/W, Pt/$HfO_2$/$Al_2O_3$/W and Pt/$HfO_2$/Ti/W responses in terms of switching parameters, C2C and D2D variability. The second section shows the device response to pulse measurement, with a particular attetion to the effect

of time on the different stacks. Finally, in the third section, the internal switching dynamics are studied and supported by material characterization.

## 7.1 DC Characterization

### 7.1.1 Comparison of IV characteristics

The three different stacks Pt/HfO$_2$/W, Pt/HfO$_2$/Al$_2$O$_3$/W and Pt/HfO$_2$/Ti/W (Figure 7.1a) are fabricated following the lithography process (Section 2.1) and tested in DC voltage sweep with the W TE biased and the Pt BE grounded. In the chapter, to facilitate the reader, we will refert to the three devices as *H5* for Pt/HfO$_2$/W, *H5A3* for Pt/HfO$_2$/Al$_2$O$_3$/W and *H5T3* for Pt/HfO$_2$/Ti/W. An initial forming procedure in positive polarity is required to create the conductive filament inside the oxide layers. The forming consists in a sweep from 0 V to 7 V with a $I_{cc}$ of 1 mA. In order to compare the device performances, the same voltage amplitude and $I_{cc}$ value are used for all the three stacks. However, one can notice that the forming conditions could be improved for H5 and H5T3 devices, reducing the power consumption. Figure 7.1 reports the forming cycles for the H5, H5A3 and H5T3 ReRAMs; the $V_{forming}$ values are 3.25 V, 5.65 V and 2.57 V, respectively.

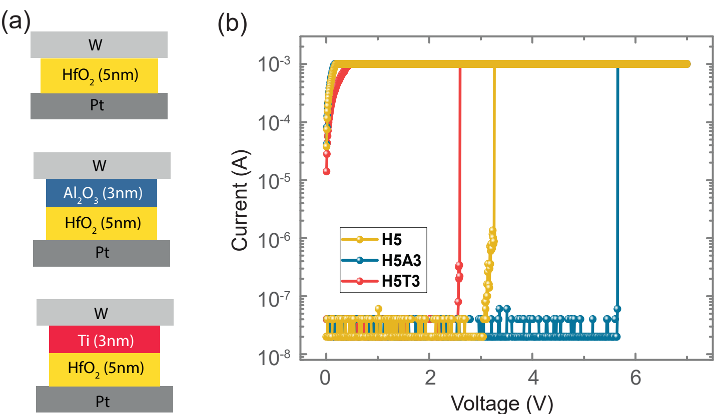


Figure 7.1: (a)Schematic representation of the three studied stack; the thickness of HfO$_2$ oxide layer is 5 nm, while Al$_2$O$_3$ barrier and Ti buffer layers are 3 nm thick. (b) Forming cycle for the three stacks: H5 forming is reported in yellow, H5A3 is reported in blue and H5T3 in red. Adapted from [160].

The H5 stack presents a gradual forming current increase with a higher transient current of $3{\cdot}10^{-7}$ A, which is the effect of consecutive W oxidation stages. As expected, the insertion of the barrier layer determines an increase in the energy required for the initial CF formation compared to the H5. The two factors responsible for this increase are the $Al_2O_3$ high band-gap and the large Al-O bonding energy, which reduce the defect density and prevent the W electrode remote scavenging [31]. The opposite effect is obtained introducing the buffer layer, which acts as oxygen reservoir, increasing the Vö density. W and Ti are active metal with a strong oxygen affinity. However, the energies required to create $WO_x$ and $TiO_x$ are quite different: 7 eV and 1 eV, respectively, with an oxygen atomic percentage of 25% [145]. This demonstrates that Ti has much stronger thermodynamic ability to draw oxygen out of $HfO_2$ with respect to W, and creates more Vö at the interface with the oxide [87]. The metal scavenging ability has been proved to influence the $V_{forming}$ value by the ab-initio calculation reported by Chen et al. [145], based on the following equation:

$$Metal(bulk) + HfO_2 \rightarrow MOx + HfO_x + Vox \tag{7.1}$$

The I-V characteristics for 50 consecutive cycles are reported in Figure 7.2, showing a bipolar switching behavior for all the devices. The SET is performed in positive polarity with a 0 V → 3 V → 0 V sweep and 1 mA $I_{cc}$; the RESET with a 0 V → -1.5 V → 0 V sweep and no current limitation. The H5 sample (Figure 7.2a) shows high current fluctuations in the positive polarity before the formation of a stable CF and the abrupt SET, which occurs at 2.8 V. This is the result of the sequential and spontaneous W oxidations, which increase the Vö densities but are not sufficient to trigger the complete SET. During the RESET operation, a first current change is visible at -0.9 V, corresponding to $V_{reset}$, then the current decreases gradually until -1.5 V. The RESET is marked by a high current overshoot, which is correlated with the large value of the $V_{set}$ and the high current reached before the $I_{cc}$ limitation feedback is activated (few $\mu$s) [164]. The RESET current overshoot and the fluctuations in SET operations decrease the device reliability and cause a fast degradation in device performances. The insertion of an additive layer between W and $HfO_2$ modulates the W contribution, defining different switching kinetics to

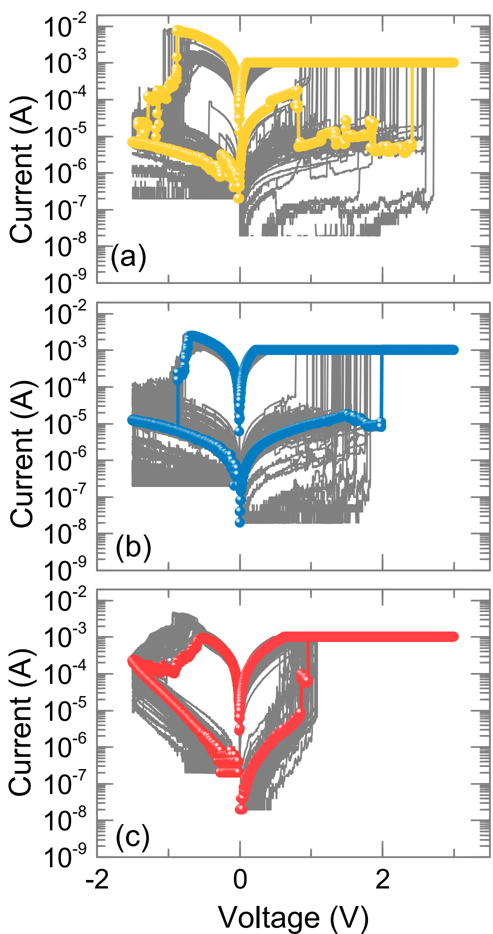


Figure 7.2: DC bipolar resistive switching IV curves for the H5 (yellow), H5A3 (blue) and H5T3 (red) stacks with positive set and negative reset operations. Adapted from [160].

tune the electrical functionality. For the H5A3 (Figure 7.2b), $V_{set}$ and $V_{reset}$ are $\sim$ 2 V and -0.9 V and in both the polarities the resistance switching determines a sharp change in current. The H5T3 device is the most stable in terms of current fluctuations during SET and current overshoot during RESET (Figure 7.2c). This device switches to LRS at $\sim$ 1 V and it maintains the LRS till the $V_{reset}$ at -0.4 V is reached. The current is uniform and stable over cycling and the maximum RESET current is equal to $I_{cc}$.

The HRS and LRS data retention of both H5A3 and H5T3 devices at room temperature is presented in Figure 7.3a,b. The switching is not volatile and the two

resistance states do not drift over time.

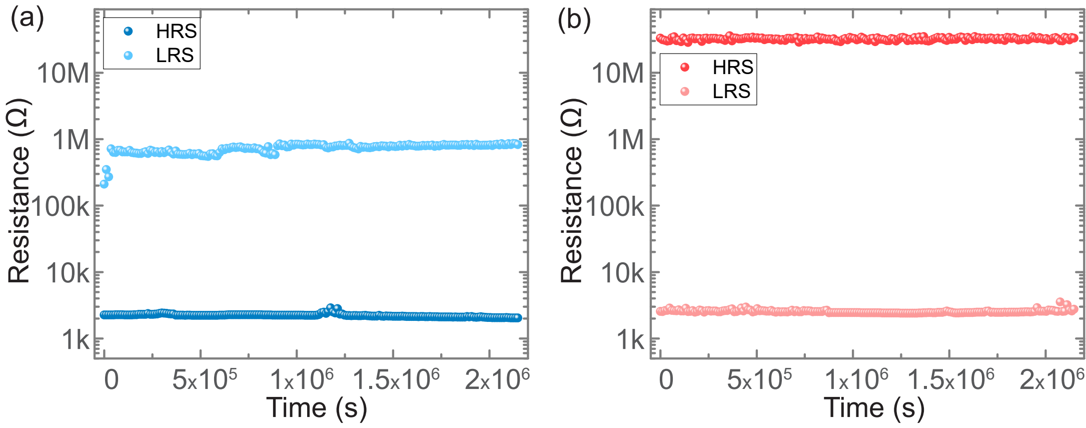


Figure 7.3: HRS and LRS data retention at room temperature for H5A3 (a) and H5T3 (b) devices, reading is performed every 2 min. Adapted from [160].

### 7.1.2 D2D and C2C repeatability

Statistical analyses are conducted in order to compare the effects of $Al_2O_3$ and Ti insertion, with particular attention on the C2C variability and the result repeatability for different samples. Regarding the C2C variability, the mean value ($\mu$) and normal standard deviation ($\sigma$) of $V_{forming}$, $V_{Set}$, $V_{Reset}$, HRS and LRS are evaluated over 100 cycles per each stack. The $\mu$ values are graphically shown in Figure 7.4, while Table 7.1 reports the complete analysis.
Starting with the comparison between H5 and H5A3, some differences are noticeable. Since $Al_2O_3$ film has stronger chemical bonding, compared to the $HfO_2$ [32, 165], a lower vacancy concentration in $Al_2O_3$ rather than in $HfO_2$ is expected, resulting in a confined CF with the rupture point at $HfO_2/Al_2O_3$ interface (extensive explanation in Section 7.3). Therefore, during the RESET, the small number of Vö in the $Al_2O_3$ is efficiently recombined. The result is a lower $V_{reset}$ (-0.54 V) for H5A3 compared to H5 (-0.60 V). The CF confinement determines also that a lower energy is needed to recreate the filaments during the SET process. Recorded $V_{set}$ of 1.43 V is 20% lower than the H5 one (1.75 V). Finally, the CF formation/rupture dynamics determines also a lowering of the HRS from 154 kΩ for H5 to 92 kΩ for

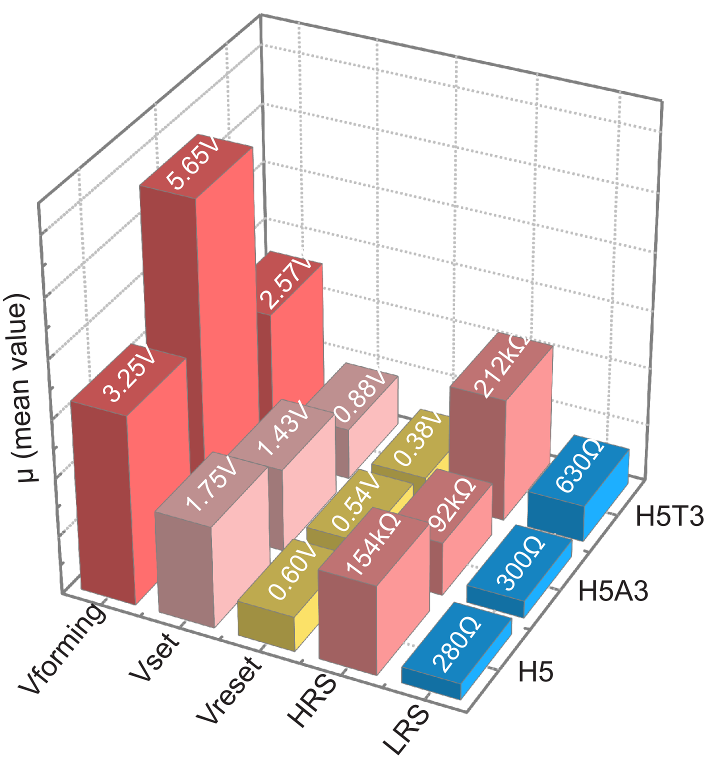


Figure 7.4: Statistical analysis represented as 3D histogram, comparing $V_{forming}$, $V_{Set}$, $V_{Reset}$, HRS and LRS over 100 cycles for H5, H5A3 and H5T3. Adapted from [160].

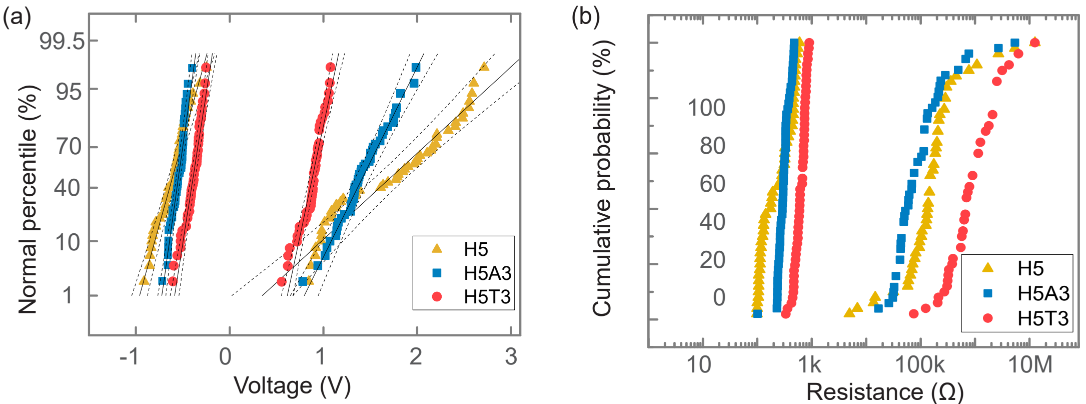


Figure 7.5: (a) Cumulative distribution of $V_{Set}$ and $V_{Reset}$ with standard deviation fit in grey and data dispersion in dash line; (c) Cumulative distribution of HRS and LRS for H5, H5A3 and H5T3 measured at 0.25 V. Adapted from [160].

Table 7.1: Mean values ($\mu$) and standard deviations ($\sigma$) of $V_{forming}$, $V_{set}$ and $V_{reset}$, HRS and LRS values over cycling. The statistic is performed on 100 cycle for each stack. Adapted from [160].

| Stack | | $V_{forming}$ (V) | $V_{set}$ (V) | $V_{reset}$ (V) | HRS kΩ | LRS kΩ |
|---|---|---|---|---|---|---|
| H5 | $\mu$ | 3.25 | 1.8 | -0.60 | 154 | 0.3 |
| | $\sigma$ | - | 0.6 | 0.15 | 90 | 0.2 |
| H5A3 | $\mu$ | 5.65 | 1.4 | -0.54 | 92 | 0.30 |
| | $\sigma$ | - | 0.3 | 0.07 | 70 | 0.07 |
| H5T3 | $\mu$ | 2.57 | 0.88 | -0.38 | 212 | 0.63 |
| | $\sigma$ | - | 0.11 | 0.08 | 160 | 0.13 |

the H5A3, while no significant differences in LRS values are reported. Considering the buffer layer insertion, the more efficient oxygen exchange of Ti during the SET/RESET results in smaller $V_{set}$ and $V_{reset}$ values of 0.88 V and -0.38 V respectively. The HRS value is higher for H5T3 (212 kΩ) compared to the H5 one, due to the fast $TiO_x$ reduction and the high $O^{2-}$ mobility inside the $HfO_2$ layer during the RESET, which result in the formation of a large filament gap. In order to evaluate the variability over cycling, Figure 7.5a,b report the cumulative probability distributions of $V_{set}$/$V_{reset}$ and LRS/HRS for the three samples. It is evident that the insertion of $Al_2O_3$ and Ti layers to modulate the $HfO_2$/W interaction improves the uniformity of both resistance states and switching voltages. Moreover, the variations of the $V_{reset}$ and LRS are smaller compared to $V_{set}$ and HRS, due to intrinsic differences of SET and RESET processes.

The D2D variability is tested by repeated measurements on 4 devices per each stack, on which standard forming procedure and 100 DC consecutive cycles are performed. Descriptive statistic in Figure 7.6 presents the $V_{set}$, $V_{reset}$, LRS and HRS for the different devices. A good device reproducibility is shown.

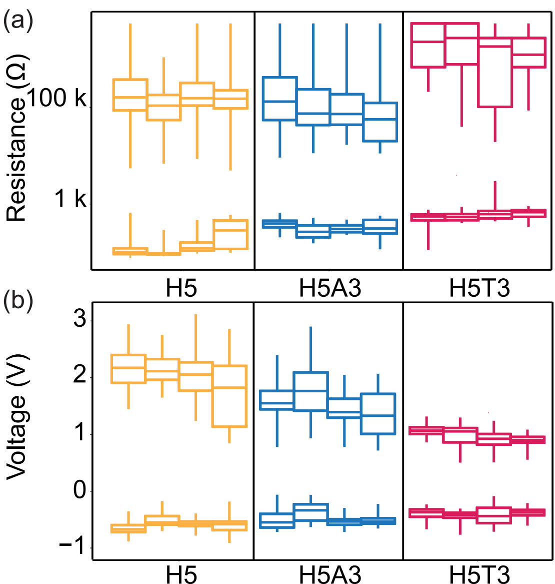


Figure 7.6: D2D distributions of (a) HRS and LRS and (b) V$_{reset}$ and V$_{set}$ for the H5, H5A3 and H5T3 devices. In the box plots, the horizontal line within the box represents the median value and the edge lines correspond to the first and the third quartiles. Figure from [160].

## 7.2 AC Characterization

### 7.2.1 Pulse endurance measurements

Endurance pulse measurements are carried out on the three different stacks, consisting in consecutive positive (SET) and negative (RESET) pulses with programmable voltage amplitude, rise time and width. In order to optimize the ReRAM endurance lifetime, the pulse conditions need to be targeted on the specific stack, choosing the appropriate voltage amplitudes, current limit and timing condition for the pulses. In H5 devices, when W is not modulated by an inter-layer, it is impossible to obtain stable measurements. The endurance degrades fast (∼150 cycles) and a controllable switching is not obtainable using pulses with width $\leq$1ms, underlining the importance of the engineering of HfO$_2$/W interface. For H5A3 and H5T3, V$_{set}$ and V$_{reset}$ are fixed at 2.5 V and -2 V and pulse slope at 20%, while current compliance and pulse width differs, assuming the values of I$_{cc}$ =1 mA; 500 $\mu$A and pulse width=1 ms; 5 $\mu$s, respectively.
Figure 7.7 reports the pulse endurance characteristics of H5A3 and H5T3 for $10^4$

cycles, with a reading periodicity of 50. Although no degradation is observed for both the devices, one can easily notice that H5T3 is capable of switching with higher HRS uniformity and shorter pulse width of 1 $\mu$s, compared to the 1 ms pulses for the H5A3. In the H5A3 endurance, a high HRS variation in the range 100 kΩ ↔10 MΩ is visible, while the LRS is stable at 2 kΩ. The H5T3 device presents a better uniformity in both the resistance states, with HRS around 10 MΩ and LRS at 3 kΩ. The H5T3 has coherent behaviors in DC an AC characterization, maintaining a low C2C variability.

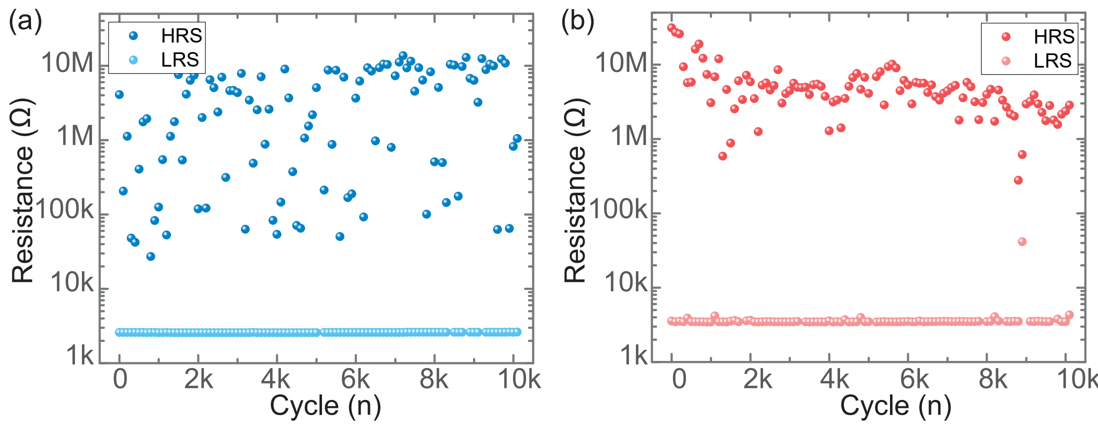


Figure 7.7: Pulse endurance for the H5A3 (a) and the H5T3 (b). For the H5A3 the pulse parameters are: $V_{set}$ =2.5 V, $V_{reset}$ =-2 V, $I_{cc}$ =1 mA, width=1 ms and slope= 20 %; for the H5T3 the same $V_{set}/V_{reset}$ are used, $I_{cc}$ = 500 $\mu$A, width=5 $\mu$s and slope= 20 %). Adapted form [160].

### 7.2.2 Transient time effect

The pulse timing effect on the resistance states of H5A3 and H5T3 is investigated, variyng the width and slope of the input stimuli. For all the utilized pulse widths (5, 10, 50, 100, 500 and 1000 $\mu$s), the slope changes from 10 % to 50 %. Several consecutive endurance tests are performed, changing the pulse width and slope in order to cover all the possible combinations. For each width-slope combination 100 cycles are performed. During the tests, the pulse amplitude and current compliance are fixed to the optimum found through the endurance measurements. The *rise time* ($t_r$) is defined as $t_r = W_p \times S_p$ in order to take into account with a single parameter the impact of both pulse width ($W_p$) and slope ($S_p$). The $t_r$ is

used to compare the resistance trend obtained from the different endurance tests. The HRS and LRS mean values and standard deviations for each set of data (100 cycles) are presented as a function of $t_r$ in Figure 7.8. The choice of represent the data through mean value and standard deviation, derives from the normal distribution of the data-set, which was inspected by Q-Q plots of the resistance values for the 100 cycles (Figure 7.9). From the figure, one can notice that the data are distributed on the diagonal, indicating that the data are correctly represented by normal distribution.

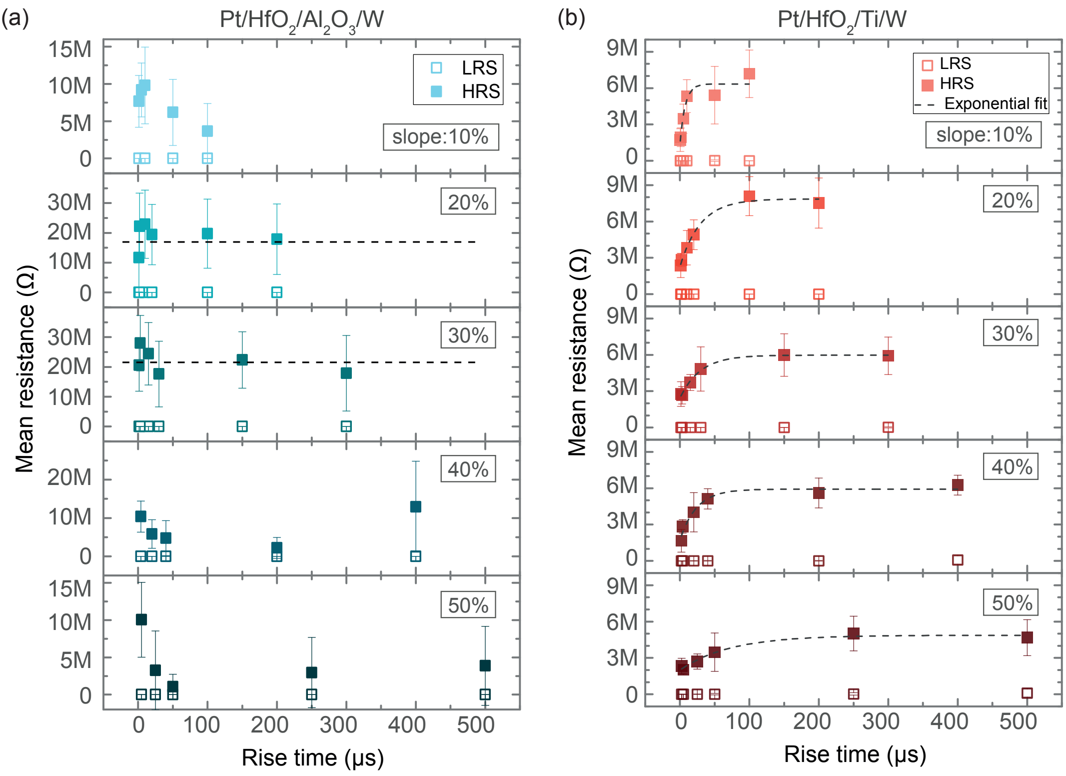


Figure 7.8: Mean values and standard deviations (error bars) on 100 consecutive pulse cycles depending on different timing for the H5A3 (a) and H5T3 (b); $V_{set}$ =2.5 V, $V_{reset}$ =-2 V and $I_{cc}$ =1 mA & 500 $\mu$A. Figure from [160].

The LRS value remains constant at ∼2 kΩ without any significant change for both the stacks, while HRS behavior depends on the kind of inserted layer. Regarding the H5A3 sample (Figure 7.8a), with the pulse slopes of 20% and 30% the device does not show any evident dependence on the rise time. The performance of this stack degrades for steep pulse slopes (< 20 %) and extended ones (≥40 %), due to

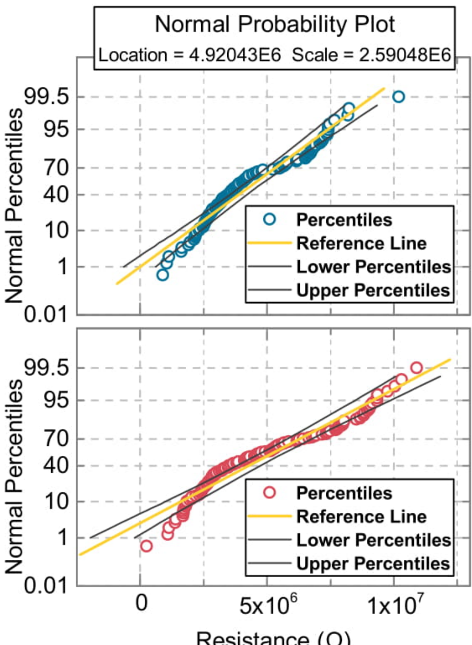


Figure 7.9: Q-Q (quantile - quantile) probability plot for two representative resistance distributions over 100 cycles. The resistances in blue are referred to the H5A3, while the resistances in red to the H5T3.

the resistance failure count, making impossible to establish a relation between HRS and rise time. A different behavior is noticeable for the H5T3 HRS (Figure 7.8b), where a clear logarithmic growth of the resistance value as a function of $t_r$ is visible. To explain the different responses of LRS and HRS with respect to the rise time in H5T3 stacks, it is important to consider the different nature of SET and RESET processes, which are the main responsible of LRS and HRS, respectively. Concerning the SET, the current is inspected using the oscilloscope (inset in Figure 7.10). From the current pulse two parameters are extracted, which are: (i) the $V_{set}$, corresponding to the voltage point before the abrupt current change, and (ii) the switching time, defined as the time interval between the pulse start and $V_{set}$. The correlation of switching time and $V_{set}$ voltage with the rise time are shown in Figure 7.10a,b. The rise time shows a linear dependence on the switching time (Figure 7.10a), while the $V_{set}$ does not present any significant dependence (Figure 7.10b). The trends confirm that SET is a voltage-driven sharp process, which starts when enough energy for ion motion is provided across the $HfO_2$ layer. When the CF is formed, the current suddenly increases and the $I_{cc}$ is reached, limiting

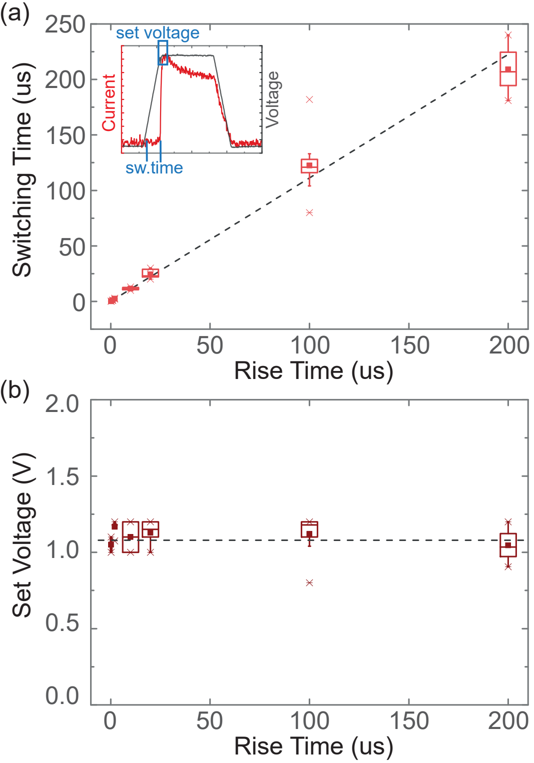


Figure 7.10: Switching time (a) and $V_{set}$ voltage (b) versus rise time during SET for H5T3 stack. Figure from [160].

electric field and temperature. This voltage dependency makes the SET not suitable to be used for gradual resistance control over pulse time. On the other side, the RESET is a gradual process, modulated by temperature and electric field [13]. Distinguishable HRS values are achievable by the precise control of the rise time, adding a degree of freedom in the resistance gradual control for neural network and brain-inspired computing applications [147].

Moreover, it is interesting to observe that the gradual HRS change is a peculiar property of Pt/$HfO_2$/Ti/W devices and has not been observed when TiN is used as TE (Figure 6.7a), underlining the W crucial role in the device electrical response. Figure 7.11 reports the current transient measurements for different pulse timing, measured using the oscilloscope and a series resistance. (Section 2.2.2). The values for the series resistance are selected for each device as a compromise between interference in switching process and noise reduction, resulting in:

- 50 Ω for the H5A3 devices;

- $1\,k\Omega$ for the H5T3 devices.

The pulse voltage amplitude is increased in order to take in account the series resistance effect. In the case of H5A3, the current variation during RESET is abrupt (Figure 7.11a), due to the complete inhibition of W/$HfO_2$ interaction. Whereas, in case of H5T3, a gradual current variation and is notable when the pulse rise time decreases (Figure 7.11b)) and the final HRS value is lower, as a result of the partial W-$HfO_2$ interaction.

To confirm the W interaction with $HfO_2$ through Ti buffer layer, the surface morphology of the samples has been analyzed using atomic force microscopy (AFM), as shown in Figure 7.12. AFM maps for the Pt bottom electrode and for Pt/$HfO_2$(5 nm) /Ti(3 nm) and Pt/$HfO_2$(5 nm)/$Al_2O_3$(3 nm) reveal that the roughness is transferred from the sputtered BE to the deposited thin films. The Pt roughness estimated through peak-to-peak measurements is about 3-4 nm, in the same range of the Ti and $Al_2O_3$ thicknesses. The main difference between these two layers consists in the

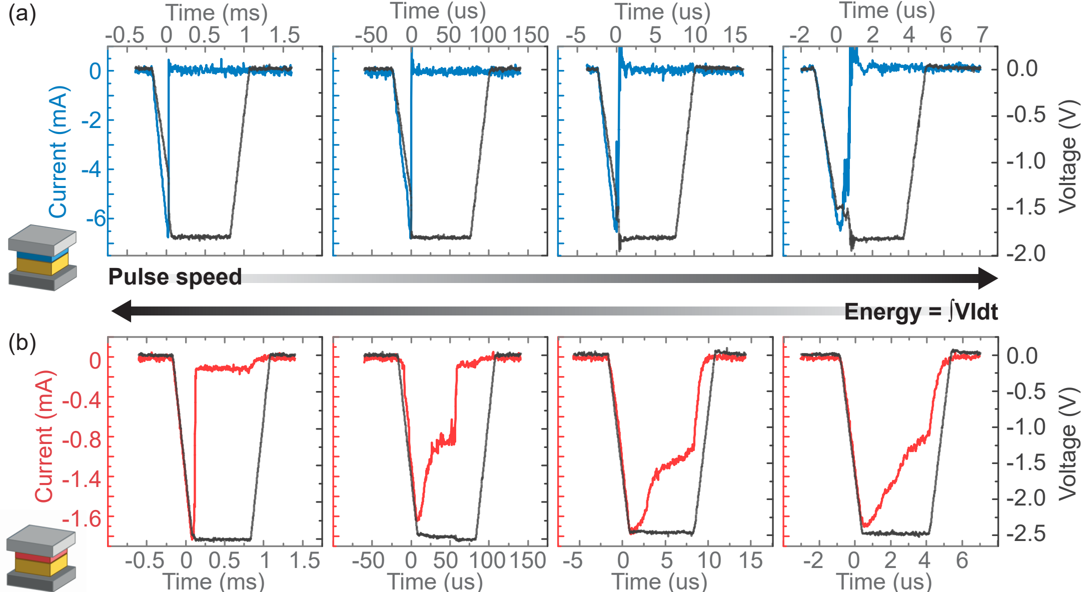


Figure 7.11: Current measurement in pulse RESET, for the different pulse widths of 1 ms, 100 $\mu$s, 10 $\mu$s and 5 $\mu$s. The applied voltages depends on the series resistance value. The H5A3 current measurements are reported in blue, while the H5T3 in red. Figure from [160].

employed deposition techniques, since the dissimilarity between ALD and sputtering are well known [166, 167]. Considering the Ti layer, which is sputtered at room temperature, a roughness 3 nm on a coverage of equivalent thickness makes highly probable the presence of pinholes, which allow the partial contact between W and HfO$_2$. In the case of Al$_2$O$_3$, the oxide acts as a dominant layer to control the switching properties. In fact, the ALD deposition is self-limiting and conformal, defining a uniform and compact Al$_2$O$_3$, when the nominal layer growth is reached (after ∼10 cycles [168]). Therefore, the role of W is completely inhibited by the insertion of the barrier layer, while is just modulated by the presence of the buffer layer. The main consequence is visible in the time-dependent endurance pulse measurement results of Figure 7.8b. A fast RESET pulse induces only the TiO$_x$ reduction, since Ti has lower oxygen affinity than WO$_x$, while the W contribution is visible when the pulse timing is long enough to provide sufficiently high energy. In this second case, due to the increases of oxygen ion density and the O$^{2-}$-Vö recombination, a deeper HRS is achieved. The process reaches its saturation point when W and Ti are both completely reduced.

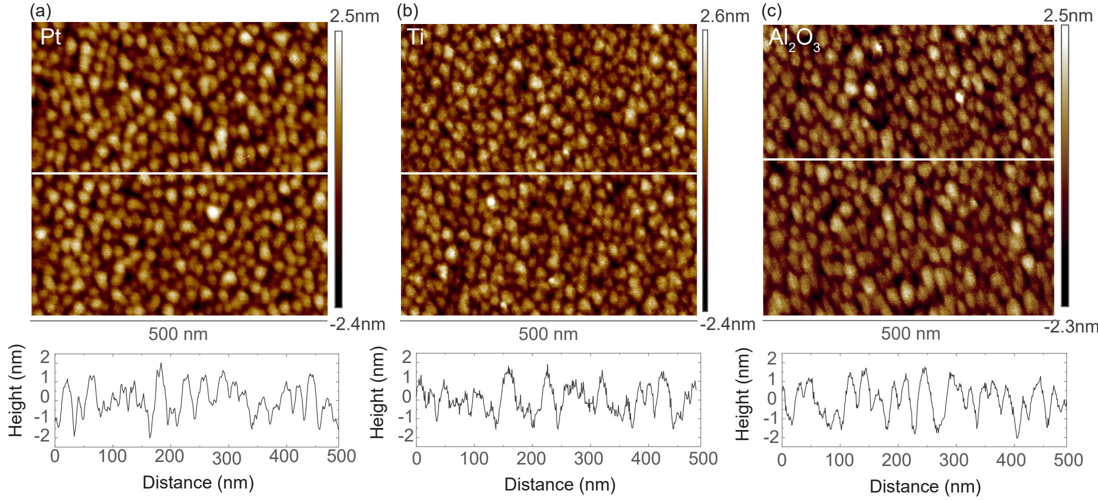


Figure 7.12: AFM maps and surface morphology are reported for the Pt BE (a), Pt/HfO$_2$/Ti (b) and Pt/HfO$_2$/Al$_2$O$_3$ (c). Adapted from [160].

## 7.3 Switching mechanism inspection

The variation in CF dynamic and oxygen exchange phenomenology caused by the insertion of an additive layer are studied in this section. Considering the H5, the direct contact of W and $HfO_2$ determines a $O^{2-}$ ions migration towards the $HfO_2$/W interface when a positive voltage is applied. At the interface a thin $WO_x$ layer and an oxygen-deficient area in the $HfO_2$ side are created. The sub-stoichiometric oxide layer acts as the starting point for the conductive filament formation. However, since W oxidation does not reach its steady state as fast as other active metals, the number of generated Vö in the active layer increases [162, 163]. This abundance can lead to possible multi-filament formation/rupture, defining a higher C2C variability and fast device degradation, as it has been observed in Section 7.1.2. Moreover, when the stable $WO_3$ state is reached, the opposite reduction reaction is not thermodynamically favorable, requiring high energy during RESET. In fact, the creation of a stable $WO_x$ compound traps the oxygen and partially blocks the exchange at the interface. The visible effects are low switching speed and high voltage required during RESET. Therefore, the insertion of a layer between W and $HfO_x$ which can partially or completely inhibits the metal-oxide interaction, strongly influences the filament dynamics and the conduction mechanism.
$Al_2O_3$ has been selected as barrier layer because of its properties, especially the high potential barrier of 8 eV, the high reduction energy and the low oxygen diffusion coefficient [23, 33]. Comparing the $\Delta$G of $HfO_2$ and $Al_2O_3$, whose values are -1010 kJ/mol and -1582 kJ/mol respectively [169], it is clear that $HfO_2$ has higher number of weak oxo-ligand bounds. If we assume that both oxides are stoichiometric and amorphous (as proved by the TEM analyses in Figure 7.13), in $HfO_2$ the formation of Vö is facilitated. Moreover, the $O^{2-}$ ion movement is highly hindered in the $Al_2O_3$, due to the lower oxygen diffusion coefficient [58, 170]. Low Vö density and reduced $O^{2-}$ ion movement in $Al_2O_3$ determine the formation of an asymmetric filament with the thicker part placed in the $HfO_2$ side, where the higher $V_{\ddot{O}}$ density is concentrated. The $HfO_2$/$Al_2O_3$ interface acts as constriction point for the filament rupture and creation, as depicted in Figure 7.14a. In order to investigate the RESET filament dynamics, the negative emi-cycles for the I-V characteristics are fitted in $ln(|I|)$ - $1/|V|$ scales. The fit is repeated on 50 consecutive cycles following the procedure reported in Appendix C. A good accordance with the Trap-Assisted

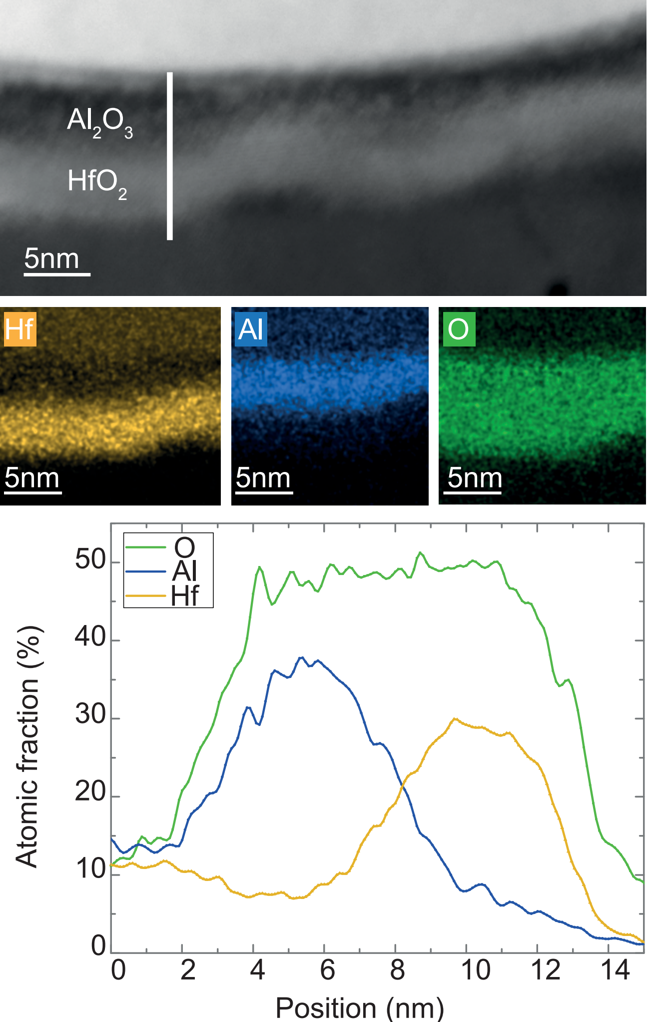


Figure 7.13: HRTEM-EDX in cross-section for the ALD deposited $HfO_2$(5nm)/$Al_2O_3$(3nm) bilayer. The aluminum (Al), hafnium(HF) and oxygen (O) are evidenced in the image and their relative quantities are plotted. Figure from [160].

Tunneling (TAT) transport mechanism is determined by the linear fit. The current density follows the equation:

$$J_{TAT} = A\ exp\left[\frac{-8\pi\sqrt{2qm^*}}{3hE}\ \phi_T^{3/2}\right] \tag{7.2}$$

where $A$ is a constant, $m^*$ is the effective mass, $q$ is the elementary charge, $h$ is the Plank constant, $E$ is the electric field and $\phi_T$ is the energy value of the traps

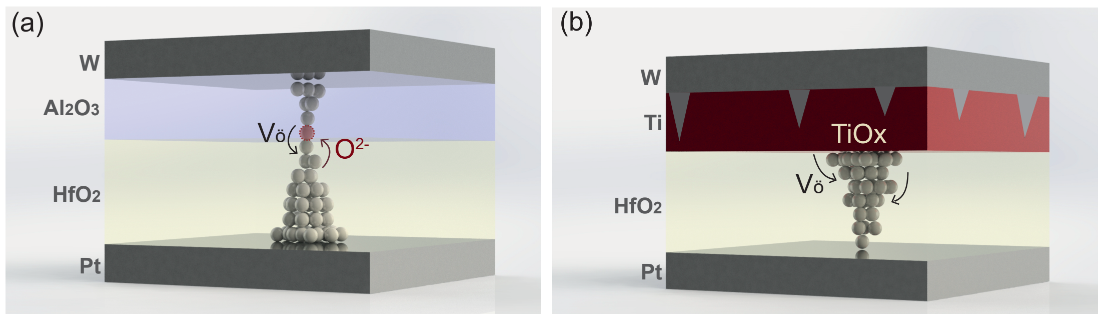


Figure 7.14: Conduction mechanism schematic representation for H5A3 (a) and H5T3 (b) devices. Adapted from [160]

with respect to the conduction band of $Al_2O_3$. When a negative voltage is applied, the carrier drift is assisted by defects-generated trap states near the $HfO_2/Al_2O_3$ interface. Considering the highly confined narrow CF in the $Al_2O_3$, the migration of a small number of ions determine the rupture of the filament resulting in the observed sharp RESET. The $Al_2O_3$ constriction in the CF shape affects also the resistance state values, leading to a higher LRS and a lower HRS, due to the filament reduced dimension and the decrease of insulating gap respectively.
Ti is selected as buffer layer because of the low energy required for oxygen extraction ($\Delta$ =-883.3 kJ/mol [152]). Ti oxidation during forming defines the formation of a thin layer of $TiO_x$ at the interface and an increase in Vö concentration in the $HfO_2$ region close to the buffer layer, which is the CF formation starter.
The presence of the Ti layer determines the formation of a conic shape filament, in which the thick part is placed at the $HfO_2$/Ti interface (Figure 7.14b). The narrow part of the filament at the BE interface is the point in which the CF rupture/rebuilt takes place. The efficient oxygen exchange by consecutive oxidation/reduction reactions at the $HfO_2$/Ti interface enhances the resistance operating window and the C2C stability. Due to the inert nature of the BE, the Pt/$HfO_2$ junction can be modeled as Schottky-like contact. Therefore the conduction mechanism is in this case related to the Schottky model, which follows the Equation 6.1. During RESET, the negative applied voltage increases the gap dimension at the Pt/$HfO_2$ interface, resulting in a gradual change of the current through the device [13]. The RESET kinetic study of H5T3 underline the importance of the engineering of the

oxide/electrode interface through the insertion of a Ti thin layer, which partially allows the $HfO_2$/W interaction. Taking advantage from W peculiar properties and Ti role and structure, we are able to achieve HRS multi-states by pulse timing control. These findings make $Pt/HfO_2/Ti/W$ memristors attractive for neural network applications and spike-inspired circuits, which requires gradual control of the resistance. In fact, in these samples the HRS value can be modulated by both pulse voltage amplitude and rise time.

# Chapter 8

# Conclusion and future prospective

In this thesis an extensive study on the impact of different parameters on the switching performances of oxide based ReRAMs was reported, including the impact on: the oxide structure, the device fabrication, the involved switching mechanisms and the programming stimuli. The general purpose, that acted as a common thread through the dissertation, was the achievement of a deeper awareness in ReRAM fabrication development and testing, which are fundamental requests for the future commercialization and the device reliability.

In the first chapters of the dissertation, the active layer composition, morphology and structure had the major role, dealing with materials not conventionally used for the microelectronic component fabrication. The definition of new ALD processes and the material characterizations were accomplished, in order to optimize the growth parameters and define morphology, structure and composition of the oxide thin films. In particular, regarding pure ZnO, a complete study of the material and its memristive properties have been reported, with a specific focus on the connection between the chemical/physical properties of the active layer and the internal dynamics responsible of the switching. The effects on the device electrical characteristics of oxide thickness and structure, top electrode material, device geometry and DC input stimuli were inspected and compared. In addition, the advantages of different switching mechanisms (VCM and ECM and a mix of the two) were explored on the ZnO. The devices with the optimum in performances

were used for the AC characterization, proving that the resistance of ZnO-based memristors can be gradually modulated by pulse train stimuli. In this sense the ReRAM cells act as biological synapses, changing their conductance proportionally to the input.
Then, exploiting the extreme control of atomic layer deposition technique, the ALD doping procedure was introduced, consisting in the deposition of partial single atomic $Al_2O_3$ layers in the $TiO_2$ and ZnO structures. The presence of localized $Al_2O_3$ single layers induced the creation of confined barriers, able to modify the matrix structure, the ion mobility and carrier density inside the oxide, playing different roles in $TiO_x$:$Al_2O_y$ and $ZnO_x$:$Al_2O_y$ devices. The changes in electrical response were shown and compared with the one of the pure oxides, in terms of resistance states, switching voltages and device stability over cycles. This demonstrates that memristive properties can be tuned through the ALD doping of the active layer, opening the way to a fine regulation of switching voltages and resistance state values by oxide interface engineering. Moreover the presence of barriers determines a higher CF confinement, resulting in a better C2C homogeneity and slower degradation.

In the second part of the dissertation, standard $HfO_2$ devices were introduced, with a major attention on the electrical response of the devices and on the impact of programming parameters. $HfO_2$ was selected because of the proved good C2C and D2D repaeatibility, allowing systematic electrical testing. The last two chapters presented the effects on the switching parameters of the current compliance and the $V_{stop}$ modulation for the DC sweep measures, while the influence of pulse timing, positive and negative voltage amplitudes and pulse train dimensioning were analyzed for AC characterization. A switching kinetics based on the formation/rupture of a Vö filament, characterized by a conic shape with narrower part at the Pt/$HfO_2$ interface was reported, studying its evolution over time for DC cycles and pulse parameters. The modulation of a wide number of resistance multi-states which are repeatable and retainable over time for Pt/$HfO_2$/Ti/TiN devices was achieved by ramping train pulses, taking advantage from the gradual nature of reset behavior. The study was then extended to pulse train for memristor-based neural network applications, suggesting a future development toward crossbar structures. Finally, the impact of the insertion of a buffer Ti or barrier $Al_2O_3$ layers was inspected for Pt/$HfO_2$/W, in order to modulate tungsten interaction with the oxide layer. By

the modulation of W oxidation through Ti insertion, gradual resistance states were achievable through pulse transient timing control.

Future work still need to be addressed to obtain a complete understanding of the internal switching dynamics, in order to fully dominate and control the electrical response of these new-generation devices. Concerning the synaptic-like behavior, in the last five years, the ReRAM technology has rapidly grown, even further than the expectation, becoming nowadays a promising candidate for large-integrated neural networks and for complex multi-logic architectures. The development of reliable synapses-emulator devices, which is the relevant topic from a forward-looking perspective in this work, steel need to face several issues. Among them, the inverse proportionality between operating window and number of distinguishable resistance states, the proper study of the influence of each programming parameter (voltage-time effect in particular), the retention of the intermediate states, the measurement repeatability and the D2D variation, are the focus for future development in our work. Moreover, the development of the selector-free crossbar geometry and of an in-situ current compliance limitation represent the fabrication challenges for device performance improvement.

# Appendix A

# Process Flow for lithography fabrication process

In this appendix, the detailed run card followed in the lithographic process for sample fabrication is reported. The BE deposition (steps 01-05) , the device passivation (step 06) and the VIA opening (steps 07-09) are performed on a 4-inches $< 100 >$ Si wafer covered by a $500\,\mu$m $SiO_2$ layer. Then the wafer is covered by a protective resist and is diced in 1x1 cm die.
The active layer deposition (steps 13-14) and the TE deposition and patterning (steps 15-17) are performed on the single die. This configuration allows more flexibility in different stack testing, giving the possibility to modify the active layer composition and the oxyde-TE interfaces using the same BE process.

The process was developed and optimized in a previous study [90] in the *Center of Micronanotecnology* (CMi) at the École Polytechnique Fédérale de Lausanne (EPFL). The CMi complex is made of different clean rooms, equipped for the fabrication and testing of micro-technologies (**https://cmi.epfl.ch/**). During my period at EPFL, I fabricated the devices, whose electrical measurement are reported in the thesis, with particular focusing on the active layer and TE deposition (steps 13-17).

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☐ Semestral Project ☐ Master Project ☐ Thesis ☑ Other

# Single cell ReRAM

## Description

The following process flow describes the realization of a vertically stacked single crosspoint ReRAM. **I will follow the process starting from step 13** on partially fabricated and diced chips. Therfore, my work is focused on : deposition and patterning of oxide layer and top electrode. This process is on chip (after dicing at step 10-12)

Key features: $HfO_x$ resistive switching layer, TiN tope electrode, Optical lithograpy.

| Technologies used |
|---|
| ALD deposition, Sputtering, $O_2$ plasma, Positive resist, Dry etching, Profilometer, Ellipsometer, SEM |

| Photolith masks | | | |
|---|---|---|---|
| **Mask #** | **Critical Dimension** | **Critical Alignment** | **Remarks** |
| 2 | **20um** | First mask | BE structuration (Ti/Pt) |
| 3 | **1um** | 5um | LTO structuration for VIA Definition |
| 5 | **20um** | 5um | Oxyde and TE structuration (HfOx/Ti/TiN) |

| Substrate Type |
|---|
| Silicon <100>, Ø100mm, 525um thick, Single Side polished, Prime, p type, 0.1-0.5 Ohm.cm |

### *Process outline*

| Step | Process description | Cross-section after process |
|---|---|---|
| **01** | **Substrate**: ***Si/SiO2 test***<br>*Wafer cleaning (SRD rinse + $O_2$ plasma)*<br>Machine: *Oxford PRS900* | View 1 |

| | | |
|---|---|---|
| **02** | ***Adhesion layer +*** <br> ***BE DC sputtering*** <br> Machine: *SPIDER600* <br> Material : Ti-Pt <br> Thickness : 5nm-125nm | View 1 |
| **03** | ***Photolitography*** <br> Machine: *ACS200 coater/develop + SuessMA6* <br> PR : AZECI3007 – 1.2$\mu m$ <br> Mask : #2 *CD = 20$\mu m$* | 20 um <br> View 1 |
| **04/05** | ***Dry Etch*** <br> Material : *Ti [$Cl_2/BCl_3$]- Pt[$Cl_2/Ar$]* <br> Machine: *STS Multiplex ICP* <br> Depth : 130nm <br> + Resist strip | View 1 |
| **06** | ***LPCVD Passivation*** <br> Machine: *Centrotherm Furn.* <br> Material : LTO <br> Thickness : 100nm | View 1 |
| **07** | ***Photolithography*** <br> Machine: *ACS200 coater/develop + SuessMA6* <br> PR : AZECI3007 – 0.63$\mu m$ <br> Mask : #3 *CD = 1um* | View 1 |

| | | |
|---|---|---|
| **08/09** | ***Wet Etch***<br>Material : *LTO [BHF]*<br>Machine: *Plade Wetbench*<br>Depth : 100nm<br>+ Resist strip | View 1 |
| **10/11/12** | ***Resist Coating***<br>Machine: *ACS200 coater*<br>PR : AZECI3027 –4$\mu m$<br>***+ Dicing***<br>Machine: *BM0229*<br>***+Resist Strip*** | |
| **13** | ***Resistive layer ALD***<br>Machine: *BENEQ TFS200*<br>Material : $HfO_2$<br>Thickness : 5nm | View 1 |
| **14** | ***Buffer layer DC sputtering***<br>Machine: *DP650*<br>Material : Ti<br>Thickness : 3nm<br>+<br>***TE RF sputtering***<br>Machine: DP650<br>Material : TiN<br>Thickness : 56nm | View 1<br>View 1 |

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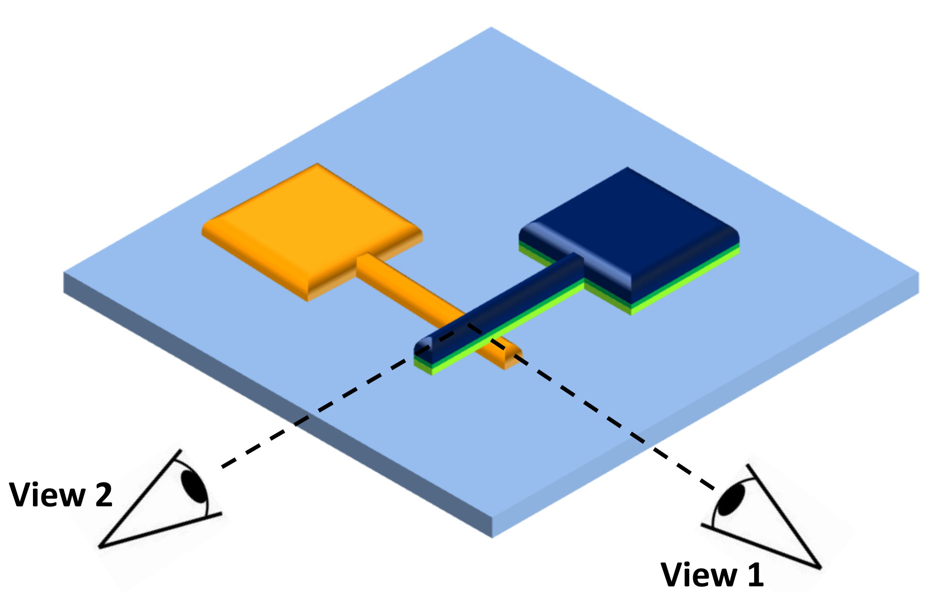
| | | |
|---|---|---|
| **15** | ***Photolithography***<br>Machine: *Manual coater + MJB4*<br>PR : AZECI3007 – 1$\mu m$<br>Mask : #5 *CD = 20um* | 20 um<br>View 2 |
| **16/17** | ***Dry Etch***<br>Material : *TiN [$Cl_2$/$BCl_3$] - Hf[$Cl_2$/$BCl_3$] - $HfO_2$ [Ar/$Cl_2$/ $BCl_3$]*<br>Machine: *STS Multiplex ICP*<br>Depth : 64nm<br>**+ Resist strip** | View 2 |



# Appendix B

# ALD recipe for Beneq TFS 200 reactor

In order to define the ALD process, is important to control the Beneq TFS 200 reactor, controlling the precursor doses, the inert gas fluxes and the chamber temperature and pressure. The dedicated software allows to control all this parameters by writing specific recipe with a customized code.

A case-study for the recipe developed for 50 nm ZnO at a reactor temperature of 200°C is reported.

In the first steps of the recipe, the chamber is purged and the gas fluxes are modulated to reach the 250 and 600 sccm. Then, if temperature and pressure are in the range defined for the deposition, the recipe core start and the two half reactions of the ALD cycle are defined. A code loop allows to repeat the cycle a set number of time to reach the desired thickness, depending on the GPC.

```
*Recipe ZnO test 50nm
*Recipe for ZnO 0.22 nm/cycles
*Precursors DEZ and Water by own vapor pressures
*DEZ at liquid source 2
*Water at liquid source 4
*Source needle valves (NV-PL2 open 1 turn, NV-PL4 open 1 turn)
*reactor temperature 200

*Program start
SPROG

*Open the N2 main valve and chamber flow valve and make sure filling valve is closed
OPEN DV-SN1,DV-NV2
CLOSE DV-NV1

*Open main vacuum valve
OPEN DV-VP1

*Set flows for preparation step
    FLOW MFC-NOVS=20
    FLOW MFC-NOPS=20

*Close pulse valves
CLOSE DV-PL1,DV-BL1
CLOSE DV-PL2,DV-BL2
CLOSE DV-PH1,DV-BH1,DV-BHA1
CLOSE DV-AF

*Close process gas valves
CLOSE DV-PG1

*Check the vacuum level
    WUNTIL PT-P1<10 10s

*Set temperatures 200C
    TEMP TE-R1S=200

*Wait until temperature is ok
    WUNTIL TE-R1>195 5h

*Set flows for process
    FLOW MFC-NOVS=250
    FLOW MFC-NOPS=600

*Are temperatures ok to start the process ?
WRITE M5
WUSER YES

*open precursor hand valves
WRITE M6
```

```
WUSER YES

*Pulsing DEZ and Water 227 cycles -------------------------------------------

REPEAT 227

    Pulse DV-PL2 200ms
    Purge 2s

    Pulse DV-PL4 500ms
    Purge 2s

REND

*-------------------------------------------------------------------------------

*Set temperatures
    TEMP TE-R1S=20

*Close pulse valves
CLOSE DV-PL1,DV-BL1
CLOSE DV-PL2,DV-BL2
CLOSE DV-PH1,DV-BH1,DV-BHA1
CLOSE DV-AF

*Close process gas valves
CLOSE DV-PG1

*Close precursor hand valves
WRITE M7
WUSER YES

*Confirm that all precursor hand valves are closed
WRITE M22
WUSER YES

*Start DEZ line purge
WRITE M25
WUSER YES

PULSE DV-PL2 2min

*Set flows
    FLOW MFC-NOVS=20
    FLOW MFC-NOPS=20

*End program
EPROG
```

# Appendix C

# Process for the fit of the I-V curves

In this appendix, the process followed for the linear fit of I-V cycles in order to define the switching mechanism is presented. The same procedure has been followed for the results reported in Chapter 6 and Chapter 7, with the main purpose of the repeating of the same fit on a wide number of consecutive cycles, to obtain a systematic and reliable study.

Table C.1: In the Table the parameters extracted from 10 linear fits for the 0 V→-1.5 V→0 V DC sweep in Pt/$HfO_2$/Ti/TiN samples are reported.

| **Cycles n** | **Resistance kΩ** | **Slope** | **Intercept** | **Energy Gap eV** | **$D_{sw}$ nm** |
|---|---|---|---|---|---|
| 1 | 498 | 5,3 | -17,2 | 1,11 | 0.5 |
| 2 | 551 | 4,2 | -15,9 | 1,03 | 0.8 |
| 3 | 249 | 4,8 | -16,4 | 1,06 | 0.6 |
| 4 | 286 | 4,6 | -16,0 | 1,03 | 0.6 |
| 5 | 326 | 4,4 | -15,9 | 1,03 | 0.7 |
| 6 | 245 | 4,5 | -16,0 | 1,03 | 0.6 |
| 7 | 102 | 4,9 | -16,5 | 1,07 | 0.5 |
| 8 | 295 | 4,3 | -16,1 | 1,04 | 0.7 |
| 9 | 183 | 4,3 | -15,4 | 0,99 | 0.7 |
| 10 | 391 | 4,6 | -16,2 | 1,05 | 0.6 |

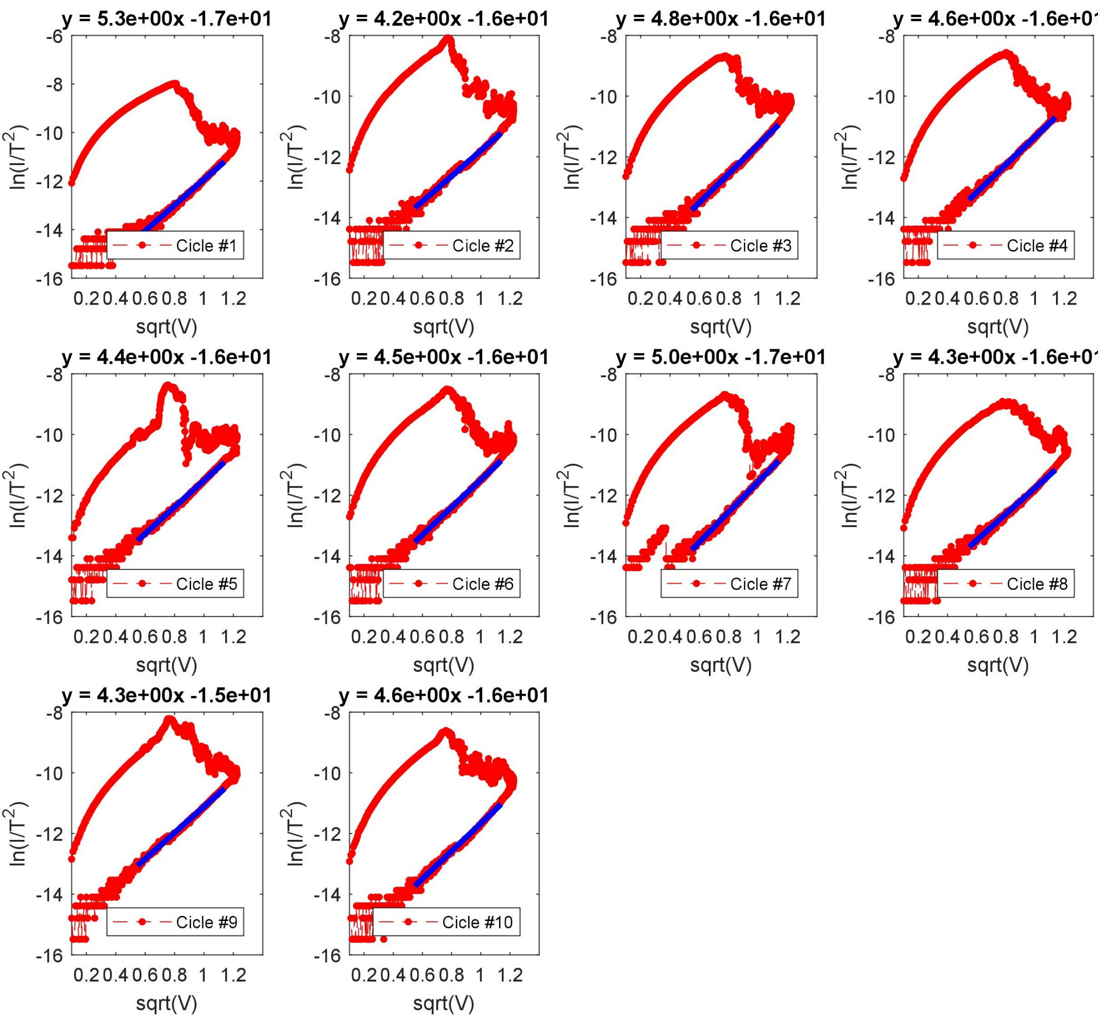



Figure C.1: The I-V negative emi-cycles, presented in $ln(J/A^{*}T^{2})$ - $\sqrt{V}$ scale. For each of the ten cycles, the HRS is interpolated by linear fit, in the same interval.[91]

To display the procedure a case study is selected, consisting in the RESET DC sweep of 0 V→-1.5 V→0 V for the Pt/$HfO_2$/Ti/TiN sample. In the chosen case, 10 consecutive cycles for each $V_{stop}$ value are analyzed. The linear fit for each cycle is performed on the same interval of values on the I-V negative emi-cycles, and the coefficient of determination ($R^2$), the intercept and the slope are extracted. The first parameter is used to define the goodness of the fit-data concordance, to understand which is the conduction mechanism that best describes the transport during the RESET. While from the slope and intercept the barrier height and gap

dimension at the inert electrode/ active layer interface are extracted.
Figure C.1 reports the I-V curves in $ln(J/A^{*}T^{2})$ - $\sqrt{V}$ scale for the 10 cycles and the linear fit of the HRS. In this case, the Schottky transport mechanism correctly describes the data. The extracted parameters are summarized in the Table C.1.

# Bibliography

1. Chua, L. Memristor-the missing circuit element. *IEEE Transactions on circuit theory* **18,** 507–519 (1971).
2. Corinto, F. & Forti, M. Memristor Circuits: Flux-Charge Analysis Method. *IEEE Trans. on Circuits and Systems* **63,** 1997–2009 (2016).
3. Chua, L. O. & Kang, S. M. Memristive devices and systems. *Proceedings of the IEEE* **64,** 209–223 (1976).
4. Strukov, D. B., Snider, G. S., Stewart, D. R. & Williams, R. S. The missing memristor found. *nature* **453,** 80 (2008).
5. Wong, H.-S. P. *et al.* Metal–oxide RRAM. *Proceedings of the IEEE* **100,** 1951–1970 (2012).
6. Kumar, D., Aluguri, R., Chand, U. & Tseng, T. Metal oxide resistive switching memory: materials, properties and switching mechanisms. *Ceramics International* **43,** S547–S556 (2017).
7. Yang, J. J., Strukov, D. B. & Stewart, D. R. Memristive devices for computing. *Nature nanotechnology* **8,** 13 (2013).
8. Ielmini, D. Resistive switching memories based on metal oxides: mechanisms, reliability and scaling. *Semiconductor Science and Technology* **31,** 063002 (2016).
9. Sawa, A. Resistive switching in transition metal oxides. *Materials today* **11,** 28–36 (2008).
10. *Functional Metal Oxide Nanostructures* 1st ed. ISBN: 978-1-4419-9930-6,978-1-4419-9931-3 (Springer-Verlag New York, 2012).

11. Larentis, S., Nardi, F., Balatti, S., Gilmer, D. C. & Ielmini, D. Resistive switching by voltage-driven ion migration in bipolar RRAM—Part II: Modeling. *IEEE Transactions on Electron Devices* **59,** 2468–2475 (2012).

12. Ielmini, D., Nardi, F. & Balatti, S. Evidence for voltage-driven set/reset processes in bipolar switching RRAM. *IEEE Transactions on Electron Devices* **59,** 2049–2056 (2012).

13. Marchewka, A. *et al.* Nanoionic resistive switching memories: On the physical nature of the dynamic reset process. *Advanced Electronic Materials* **2,** 1500233 (2016).

14. Kim, S., Choi, S. & Lu, W. Comprehensive physical model of dynamic resistive switching in an oxide memristor. *ACS nano* **8,** 2369–2376 (2014).

15. Nardi, F., Larentis, S., Balatti, S., Gilmer, D. C. & Ielmini, D. Resistive switching by voltage-driven ion migration in bipolar RRAM—Part I: Experimental study. *IEEE Transactions on Electron Devices* **59,** 2461–2467 (2012).

16. Menzel, S., Böttger, U., Wimmer, M. & Salinga, M. Physics of the switching kinetics in resistive memories. *Advanced functional materials* **25,** 6306–6325 (2015).

17. Yu, S. & Wong, H.-S. P. A phenomenological model for the reset mechanism of metal oxide RRAM. *IEEE Electron Device Letters* **31,** 1455–1457 (2010).

18. Son, J. & Shin, Y.-H. Direct observation of conducting filaments on resistive switching of NiO thin films. *Applied Physics Letters* **92,** 222106 (2008).

19. Celano, U. *et al.* Imaging the three-dimensional conductive channel in filamentary-based oxide resistive switching memory. *Nano letters* **15,** 7970–7975 (2015).

20. Liu, Q. *et al.* Real-time observation on dynamic growth/dissolution of conductive filaments in oxide-electrolyte-based ReRAM. *Advanced Materials* **24,** 1844–1849 (2012).

21. Yang, Y. *et al.* Observation of conducting filament growth in nanoscale resistive memories. *Nature communications* **3,** 732 (2012).

22. Tian, X. *et al.* Filament growth dynamics in solid electrolyte-based resistive memories revealed by in situ TEM. *Nano Research* **7,** 1065–1072 (2014).

23. Yang, Y. *et al.* Probing nanoscale oxygen ion motion in memristive systems. *Nature Communications* **8,** 15173 (2017).

24. Kamarozaman, N. S. *et al.* Effect of film thickness on the memristive behavior of spin coated titanium dioxide thin films. *Proceedings - RSM 2013: 2013 IEEE Regional Symposium on Micro and Nano Electronics,* 155–158 (2013).

25. Chanthbouala, A. *et al.* Solid-state memories based on ferroelectric tunnel junctions. *Nature nanotechnology* **7,** 101 (2012).

26. Raoux, S., Wełnic, W. & Ielmini, D. Phase change materials and their application to nonvolatile memories. *Chemical reviews* **110,** 240–267 (2009).

27. Jiang, A. Q. *et al.* A Resistive Memory in Semiconducting BiFeO3 Thin-Film Capacitors. *Advanced materials* **23,** 1277–1281 (2011).

28. Schindler, C., Thermadam, S. C. P., Waser, R. & Kozicki, M. N. Bipolar and Unipolar Resistive Switching in Cu-Doped $SiO_2$. *IEEE Transactions on Electron Devices* **54,** 2762–2768 (2007).

29. Jeong, D. S., Schroeder, H. & Waser, R. Coexistence of bipolar and unipolar resistive switching behaviors in a Pt/ TiO2/ Pt stack. *Electrochemical and solid-state letters* **10,** G51–G53 (2007).

30. Robertson, J. & Clark, S. Limits to doping in oxides. *Physical Review B* **83,** 075205 (2011).

31. Govoreanu, B. *et al. Vacancy-modulated conductive oxide resistive RAM (VMCO-RRAM): An area-scalable switching current, self-compliant, highly nonlinear and wide on/off-window resistive switching cell* in *Electron Devices Meeting (IEDM), 2013 IEEE International* (2013), 10–2.

32. Goux, L. *et al.* On the Bipolar Resistive-switching Characteristics of Al2O3- and HfO2-based Memory Cells Operated in the Soft-breakdown Regime. *Journal of Applied Physics* **116,** 134502 (2014).

33. Banerjee, W. *et al.* Variability Improvement of TiO x/Al2O3 Bilayer Nonvolatile Resistive Switching Devices by Interfacial Band Engineering with an Ultrathin Al2O3 Dielectric Material. *ACS Omega* **2,** 6888–6895 (2017).

34. Guo, Y. & Robertson, J. Materials selection for oxide-based resistive random access memories. *Applied Physics Letters* **105,** 223516 (2014).

35. Rahaman, S. Z. *et al.* Excellent resistive memory characteristics and switching mechanism using a Ti nanolayer at the Cu/TaO x interface. *Nanoscale research letters* **7,** 345 (2012).

36. Lim, E. W. & Ismail, R. Conduction Mechanism of Valence Change Resistive Switching Memory: A Survey, 586–613 (2015).

37. Waser, R. & Matthias, W. *Memristive Phenomena – From Fundamental Physics to Neuromorphic Computing. Lecture Notes of the 47th IFF Spring School 2016* (Forschungszentrum Jülich GmbH, 2016).

38. Li, Y. *et al.* Investigation on the conductive filament growth dynamics in resistive switching memory via a universal Monte Carlo simulator. *Scientific Reports* **7,** 11204 (2017).

39. Lian, X. *et al.* Multi-scale quantum point contact model for filamentary conduction in resistive random access memories devices. *Journal of Applied Physics* **115,** 244507 (2014).

40. Zhang, Z. *et al.* Electrochemical metallization cell with anion supplying active electrode. *Scientific reports* **8,** 12617 (2018).

41. Yang, Y. *et al.* Electrochemical dynamics of nanoscale metallic inclusions in dielectrics. *Nature communications* **5,** 4232 (2014).

42. Valov, I. *et al.* Nanobatteries in redox-based resistive switches require extension of memristor theory. *Nature communications* **4,** 1771 (2013).

43. Pan, F., Gao, S., Chen, C., Song, C. & Zeng, F. Recent progress in resistive random access memories: materials, switching mechanisms, and performance. *Materials Science and Engineering: R: Reports* **83,** 1–59 (2014).

44. Pi, S. *et al.* Memristor crossbars with 4.5 terabits-per-inch-square density and two nanometer dimension. *arXiv preprint arXiv:1804.09848* (2018).

45. Jiang, H. *et al.* Sub-10 nm Ta Channel Responsible for Superior Performance of a HfO 2 Memristor. *Scientific reports* **6,** 28525 (2016).

46. Zangeneh, M. & Joshi, A. Design and optimization of nonvolatile multibit 1T1R resistive RAM. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* **22,** 1815–1828 (2014).

47. Merced-Grafals, E. J., Dávila, N., Ge, N., Williams, R. S. & Strachan, J. P. Repeatable, accurate, and high speed multi-level programming of memristor 1T1R arrays for power efficient analog computing applications. *Nanotechnology* **27,** 365202 (2016).

48. Hong, X. *et al.* Oxide-based RRAM materials for neuromorphic computing. *Journal of Materials Science,* 1–27 (2018).

49. Jo, S. H. *et al.* Nanoscale memristor device as synapse in neuromorphic systems. *Nano letters* **10,** 1297–1301 (2010).

50. Choi, S., Shin, J. H., Lee, J., Sheridan, P. & Lu, W. D. Experimental demonstration of feature extraction and dimensionality reduction using memristor networks. *Nano letters* **17,** 3113–3118 (2017).

51. Li, C. *et al.* Analogue signal and image processing with large memristor crossbars. *Nature Electronics* **1,** 52 (2018).

52. Yao, P. *et al.* Face classification using electronic synapses. *Nature communications* **8,** 15199 (2017).

53. Al-Mamun, M., King, S. W., Meda, S. & Orlowski, M. K. Impact of the Heat Conductivity of the Inert Electrode on ReRAM Performance and Endurance. *ECS Transactions* **85,** 207–212 (2018).

54. Lee, M.-J. *et al.* A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta 2 O 5- x/TaO 2- x bilayer structures. *Nature materials* **10,** 625 (2011).

55. Chand, U. *et al.* Suppression of endurance degradation by utilizing oxygen plasma treatment in HfO2 resistive switching memory. *Applied Physics Letters* **106,** 153502 (2015).

56. Su, Y.-T. *et al.* Suppression of endurance degradation by applying constant voltage stress in one-transistor and one-resistor resistive random access memory. *Japanese Journal of Applied Physics* **56,** 010303 (2016).

57. Lee, H. *et al. Evidence and solution of over-RESET problem for HfO x based resistive memory with sub-ns switching speed and high endurance* in *Electron Devices Meeting (IEDM), 2010 IEEE International* (2010), 19–7.

58. Lin, Y.-D. *et al.* Retention Model of TaO/HfO x and TaO/AlO x RRAM with Self-Rectifying Switch Characteristics. *Nanoscale research letters* **12,** 407 (2017).

59. Yu, S., Guan, X. & Wong, H.-S. P. *On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, Monte Carlo simulation, and experimental characterization* in *Electron Devices Meeting (IEDM), 2011 IEEE International* (2011), 17–3.

60. Park, J. *et al.* Improved switching uniformity of a carbon-based conductive-bridge type ReRAM by controlling the size of conducting filament. *Microelectronic Engineering* **88,** 935–938 (2011).

61. Calderoni, A., Sills, S., Cardon, C., Faraoni, E. & Ramaswamy, N. Engineering ReRAM for high-density applications. *Microelectronic Engineering* **147,** 145–150 (2015).

62. Kim, W., Menzel, S., Wouters, D., Waser, R. & Rana, V. 3-bit multilevel switching by deep reset phenomenon in Pt/W/TaO X/Pt-ReRAM devices. *IEEE Electron Device Letters* **37,** 564–567 (2016).

63. Zhao, L. *et al.* Multi-level control of conductive nano-filament evolution in HfO 2 ReRAM by pulse-train operations. *Nanoscale* **6,** 5698–5702 (2014).

64. Samanta, S. *et al.* Understanding of multi-level resistive switching mechanism in GeO x through redox reaction in H 2 O 2/sarcosine prostate cancer biomarker detection. *Scientific Reports* **7,** 11240 (2017).

65. Zhang, W. *et al.* An electronic synapse device based on solid electrolyte resistive random access memory. *IEEE Electron Device Letters* **36,** 772–774 (2015).

66. Yu, S., Wu, Y., Jeyasingh, R., Kuzum, D. & Wong, H.-S. P. An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation. *IEEE Transactions on Electron Devices* **58,** 2729–2737 (2011).

67. Kim, S. *et al.* Analog synaptic behavior of a silicon nitride memristor. *ACS applied materials & interfaces* **9,** 40420–40427 (2017).

68. Hsieh, C.-C., Roy, A., Chang, Y.-F., Shahrjerdi, D. & Banerjee, S. K. A sub-1-volt analog metal oxide memristive-based synaptic device with large conductance change for energy-efficient spike-based computing systems. *Applied Physics Letters* **109,** 223501 (2016).

69. Wang, Z. *et al.* Engineering incremental resistive switching in TaO x based memristors for brain-inspired computing. *Nanoscale* **8,** 14015–14022 (2016).

70. Yang, C.-S. *et al.* Electrochemical-reaction-induced synaptic plasticity in MoO x-based solid state electrochemical cells. *Physical Chemistry Chemical Physics* **19,** 4190–4198 (2017).

71. Fang, R., Chen, W., Gao, L., Yu, W. & Yu, S. Low-temperature characteristics of HfO x-based resistive random access memory. *IEEE Electron Device Letters* **36,** 567–569 (2015).

72. Gilmer, D. *et al.* *Superior filament formation control in HfO2 based RRAM for high-performance low-power operation of 1 μA to 20 μA at+/- 1V* in *VLSI Technology, Systems, and Applications (VLSI-TSA), 2012 International Symposium on* (2012), 1–2.

73. Kim, W. *et al.* *Forming-free Nitrogen-doped AlO X RRAM with Sub-μA Programming Current* in *VLSI Technology (VLSIT), 2011 Symposium on* (2011), 22–23.

74. Kim, W. *et al.* Impact of Oxygen Exchange Reaction at the Ohmic Interface in Ta 2 O 5-based ReRAM Devices. *Nanoscale* **8,** 17774–17781 (2016).

75. Yang, J. J. *et al.* Dopant control by atomic layer deposition in oxide films for memristive switches. *Chemistry of Materials* **23,** 123–125 (2010).

76. Siles, P. F. *et al.* Tuning resistive switching on single-pulse doped multilayer memristors. *Nanotechnology* **24,** 035702 (2012).

77. Simanjuntak, F. M. *et al.* Impacts of Co doping on ZnO transparent switching memory device characteristics. *Applied Physics Letters* **108,** 183506 (2016).

78. Wang, H. *et al.* Resistance switching properties of Ag/ZnMn 2 O 4/p-Si fabricated by magnetron sputtering for resistance random access memory. *Journal of Wuhan University of Technology-Mater. Sci. Ed.* **30,** 1159–1162 (2015).

79. Li, H. *et al.* Improvement of resistive switching in ZnO film by Ti doping. *Thin Solid Films* **537,** 279–284 (2013).

80. George, S. M. Atomic layer deposition: an overview. *Chemical reviews* **110,** 111–131 (2009).

81. Ponraj, J. S., Attolini, G. & Bosi, M. Review on atomic layer deposition and applications of oxide thin films. *Critical Reviews in Solid State and Materials Sciences* **38,** 203–233 (2013).

82. Kuech, T. *Handbook of Crystal Growth: Thin Films and Epitaxy* (Elsevier, 2014).

83. Miikkulainen, V., Leskelä, M., Ritala, M. & Puurunen, R. L. Crystallinity of inorganic films grown by atomic layer deposition: Overview and general trends. *Journal of Applied Physics* **113,** 2 (2013).

84. Knauth, P. & Tuller, H. Electrical and defect thermodynamic properties of nanocrystalline titanium dioxide. *Journal of applied physics* **85,** 897–902 (1999).

85. Elam, J., Routkevitch, D. & George, S. Properties of ZnO/Al2 O 3 Alloy Films Grown Using Atomic Layer Deposition Techniques. *Journal of the Electrochemical Society* **150,** G339–G347 (2003).

86. Banerjee, P., Lee, W.-J., Bae, K.-R., Lee, S. B. & Rubloff, G. W. Structural, electrical, and optical properties of atomic layer deposition Al-doped ZnO films. *Journal of Applied Physics* **108,** 043504 (2010).

87. Bersuker, G. *et al.* Metal oxide resistive memory switching mechanism based on conductive filament properties. *Journal of Applied Physics* **110,** 124518 (2011).

88. Baek, G. H., Lee, A. R., Kim, T. Y., Im, H. S. & Hong, J. P. Oxide stoichiometry-controlled TaOx-based resistive switching behaviors. *Applied Physics Letters* **109,** 143502 (2016).

89. Ke, J.-J. *et al.* Surface-controlled metal oxide resistive memory. *IEEE Electron Device Letters* **36,** 1307–1309 (2015).

90. Sandrini, J. *Fabrication, Characterization and Integration of Resistive Random Access Memories* tech. rep. (EPFL, 2017).

91. Giovinazzo, C., Ricciardi, C., Pirri, C., Chiolerio, A. & Porro, S. Effects of single-pulse Al2O3 insertion in TiO2 oxide memristors by low temperature ALD. *Applied Physics A* **124,** 686 (2018).

92. Porro, S. *et al.* Low-temperature atomic layer deposition of TiO2 thin layers for the processing of memristive devices. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **34,** 01A147 (2016).
93. Groner, M., Fabreguette, F., Elam, J. & George, S. Low-temperature Al2O3 atomic layer deposition. *Chemistry of Materials* **16,** 639–645 (2004).
94. Sánchez-Agudo, M., Soriano, L., Quirós, C., Avila, J. & Sanz, J. Electronic interaction at the TiO2–Al2O3 interface as observed by X-ray absorption spectroscopy. *Surface science* **482,** 470–475 (2001).
95. Omari, M., Sorbello, R. & Aita, C. Crystallization and (Al, Ti)-oxide growth in annealed Ti O 2–Al 2 O 3 multilayers. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **24,** 317–323 (2006).
96. Wohlfromm, H., Pena, P., Moya, J. S. & Requena, J. Al2TiO5 formation in alumina/titania multilayer composites. *Journal of the American Ceramic Society* **75,** 3473–3476 (1992).
97. Kwon, D.-H. *et al.* Atomic structure of conducting nanofilaments in TiO 2 resistive switching memory. *Nature nanotechnology* **5,** 148 (2010).
98. Horowitz, G., Fichou, D., Peng, X. & Delannoy, P. Evidence for a linear low-voltage space-charge-limited current in organic thin films. Film thickness and temperature dependence in alpha-conjugated sexithienyl. *Journal de Physique* **51,** 1489–1499 (1990).
99. Degraeve, R. *et al.* New insights in the relation between electron trap generation and the statistical properties of oxide breakdown. *IEEE Transactions on Electron Devices* **45,** 904–911 (1998).
100. Lee, G., Lai, B.-K., Phatak, C., Katiyar, R. S. & Auciello, O. Interface-controlled high dielectric constant Al2O3/TiOx nanolaminates with low loss and low leakage current density for new generation nanodevices. *Journal of Applied Physics* **114,** 027001 (2013).
101. Simanjuntak, F. M., Panda, D., Wei, K.-H. & Tseng, T.-Y. Status and prospects of ZnO-based resistive switching memory devices. *Nanoscale research letters* **11,** 368 (2016).

102. Laurenti, M., Porro, S., Pirri, C. F., Ricciardi, C. & Chiolerio, A. Zinc oxide thin films for memristive devices: a review. *Critical Reviews in Solid State and Materials Sciences* **42,** 153–172 (2017).

103. Porro, S. *et al.* Multiple resistive switching in core–shell ZnO nanowires exhibiting tunable surface states. *Journal of Materials Chemistry C* **5,** 10517–10523 (2017).

104. Conti, D. *et al.* Resistive switching in sub-micrometric ZnO polycrystalline films. *Nanotechnology* **30,** 065707 (2018).

105. Kääriäinen, T., Cameron, D., Kääriäinen, M.-L. & Sherman, A. *Atomic layer deposition: principles, characteristics, and nanotechnology applications* (John Wiley & Sons, 2013).

106. Yuan, N. *et al.* The influence of deposition temperature on growth mode, optical and mechanical properties of ZnO films prepared by the ALD method. *Journal of Crystal Growth* **366,** 43–46 (2013).

107. Tapily, K., Gu, D., Baumgart, H., Rigo, M. & Seo, J. Raman spectroscopy of ZnO thin films by atomic layer deposition. *ECS Transactions* **33,** 117–123 (2010).

108. Cuscó, R. *et al.* Temperature dependence of Raman scattering in ZnO. *Physical Review B* **75,** 165202 (2007).

109. Tynell, T. & Karppinen, M. Atomic layer deposition of ZnO: a review. *Semiconductor Science and Technology* **29,** 043001 (2014).

110. Jeon, S. *et al.* Structural and electrical properties of ZnO thin films deposited by atomic layer deposition at low temperatures. *Journal of the Electrochemical Society* **155,** H738–H743 (2008).

111. Pung, S.-Y., Choy, K.-L., Hou, X. & Shan, C. Preferential growth of ZnO thin films by the atomic layer deposition technique. *Nanotechnology* **19,** 435609 (2008).

112. Huby, N., Ferrari, S., Guziewicz, E., Godlewski, M. & Osinniy, V. Electrical behavior of zinc oxide layers grown by low temperature atomic layer deposition. *Applied Physics Letters* **92,** 023502 (2008).

113. Miller, D., Biesinger, M. & McIntyre, N. Interactions of CO2 and CO at fractional atmosphere pressures with iron and iron oxide surfaces: one possible mechanism for surface contamination? *Surface and Interface Analysis: An International Journal devoted to the development and application of techniques for the analysis of surfaces, interfaces and thin films* **33,** 299–305 (2002).

114. Murali, S. *et al.* Resistive switching in zinc tin oxide. *Solid-State Electronics* **79,** 248–252 (2013).

115. Kukreja, L., Das, A. & Misra, P. Studies on nonvolatile resistance memory switching in ZnO thin films. *Bulletin of Materials Science* **32,** 247–252 (2009).

116. Huang, R., Sun, K., Kiang, K. S., Morgan, K. A. & De Groot, C. Forming-free resistive switching of tunable ZnO films grown by atomic layer deposition. *Microelectronic Engineering* **161,** 7–12 (2016).

117. Kim, K. M., Han, S. & Hwang, C. S. Electronic bipolar resistance switching in an anti-serially connected Pt/TiO2/Pt structure for improved reliability. *Nanotechnology* **23,** 035201 (2011).

118. Valov, I., Waser, R., Jameson, J. R. & Kozicki, M. N. Electrochemical metallization memories—fundamentals, applications, prospects. *Nanotechnology* **22,** 254003 (2011).

119. Wedig, A. *et al.* Nanoscale cation motion in TaOx, HfOx and TiOx memristive systems. *Nature nanotechnology* **11,** 67 (2016).

120. Kang, Y. H., Choi, J.-H., Lee, T. I., Lee, W. & Myoung, J.-M. Thickness dependence of the resistive switching behavior of nonvolatile memory device structures based on undoped ZnO films. *Solid State Communications* **151,** 1739–1742 (2011).

121. Huang, Y. *et al.* Amorphous ZnO based resistive random access memory. *Rsc Advances* **6,** 17867–17872 (2016).

122. Wu, H. *et al.* Resistive Switching Performance Improvement of $Ta_2O_{5-x}/TaO_y$ Bilayer ReRAM Devices by Inserting $AlO_\delta$ Barrier Layer. *IEEE Electron Device Letters* **35,** 39–41 (2014).

123. Chen, C. *et al.* Stack optimization of oxide-based RRAM for fast write speed ($< 1\mu s$) at low operating current ($< 10\mu A$). *Solid-State Electronics* **125,** 198–203 (2016).

124. Shahrabi, E., Giovinazzo, C., Sandrini, J. & Leblebici, Y. *Multi-ReRAM synapses for artificial neural network training* in *2018 14th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME)* (2018), 69–72.

125. Zhuge, F. *et al.* Improvement of resistive switching in Cu/ZnO/Pt sandwiches by weakening the randomicity of the formation/rupture of Cu filaments. *Nanotechnology* **22,** 275204 (2011).

126. Milano, G. *et al.* Unravelling Resistive Switching Mechanism in ZnO NW Arrays: The Role of the Polycrystalline Base Layer. *The Journal of Physical Chemistry C* **122,** 866–874 (2017).

127. Frascaroli, J., Brivio, S., Covi, E. & Spiga, S. Evidence of soft bound behaviour in analogue memristive devices for neuromorphic computing. *Scientific reports* **8,** 7178 (2018).

128. Wang, C., He, W., Tong, Y. & Zhao, R. Investigation and manipulation of different analog behaviors of memristor as electronic synapse for neuromorphic applications. *Scientific reports* **6,** 22970 (2016).

129. Hardtdegen, A. *et al. Internal cell resistance as the origin of abrupt reset behavior in HfO2-based devices determined from current compliance series* in *Memory Workshop (IMW), 2016 IEEE 8th International* (2016), 1–4.

130. Fantini, A. *et al. Intrinsic switching behavior in HfO2 RRAM by fast electrical measurements on novel 2R test structures* in *Memory Workshop (IMW), 2012 4th IEEE International* (2012), 1–4.

131. Čičo, K. *et al.* Resistive switching in nonplanar HfO2-based structures with variable series resistance. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **33,** 01A108 (2015).

132. Thangavel, R. *et al.* Cesium doped and undoped ZnO nanocrystalline thin films: a comparative study of structural and micro-Raman investigation of optical phonons. *Journal of Raman Spectroscopy* **41,** 1594–1600 (2010).

133. Elam, J. & George, S. Growth of ZnO/Al2O3 alloy films using atomic layer deposition techniques. *Chemistry of Materials* **15,** 1020–1028 (2003).

134. Lu, J. *et al.* Structural, optical, and electrical properties of (Zn, Al) O films over a wide range of compositions. *Journal of Applied Physics* **100,** 073714 (2006).

135. Jia, C., Dong, Q. & Zhang, W. Effect of incorporating copper on resistive switching properties of ZnO films. *Journal of Alloys and Compounds* **520,** 250–254 (2012).

136. Lee, W.-H., Kim, E.-J. & Yoon, S.-M. Effect of Al incorporation amount upon the resistive-switching characteristics for nonvolatile memory devices using Al-doped ZnO semiconductors. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **33,** 051216 (2015).

137. Yoshioka, S. *et al.* Atomic structures of supersaturated Zn O–Al 2 O 3 solid solutions. *Journal of Applied Physics* **103,** 014309 (2008).

138. Bundesmann, C. *et al.* Raman scattering in ZnO thin films doped with Fe, Sb, Al, Ga, and Li. *Applied Physics Letters* **83,** 1974–1976 (2003).

139. Manjón, F., Mari, B., Serrano, J. & Romero, A. Silent Raman modes in zinc oxide and related nitrides. *Journal of Applied Physics* **97,** 053516 (2005).

140. Russo, V., Ghidelli, M., Gondoni, P., Casari, C. & Li Bassi, A. Multi-wavelength Raman scattering of nanostructured Al-doped zinc oxide. *Journal of Applied Physics* **115,** 073508 (2014).

141. Maeng, W., Lee, J.-w., Lee, J. H., Chung, K.-B. & Park, J.-S. Studies on optical, structural and electrical properties of atomic layer deposited Al-doped ZnO thin films with various Al concentrations and deposition temperatures. *Journal of Physics D: Applied Physics* **44,** 445305 (2011).

142. Ghosh, S., Sarkar, A., Chaudhuri, S. & Pal, A. Grain boundary scattering in aluminium-doped ZnO films. *Thin Solid Films* **205,** 64–68 (1991).

143. Giovinazzo, C. *et al.* *Analog control of retainable resistance multi-states in* $HfO_2$ *ReRAM* Submitted paper.

144. Moon, K. *et al.* Analog synapse device with 5-b MLC and improved data retention for neuromorphic system. *IEEE Electron Device Letters* **37,** 1067–1070 (2016).

145. Chen, Y. Y. *et al.* Endurance/retention trade-off on HfO2/metal cap 1T1R bipolar RRAM. *IEEE Trans Electron Devices* **60,** 1114 (2013).

146. Lee, H. *et al.* Low-power and nanosecond switching in robust hafnium oxide resistive memory with a thin Ti cap. *IEEE Electron Device Letters* **31,** 44–46 (2010).

147. Stathopoulos, S. *et al.* Multibit memory operation of metal-oxide bi-layer memristors. *Scientific reports* **7,** 17532 (2017).

148. Chen, A. Area and thickness scaling of forming voltage of resistive switching memories. *IEEE Electron Device Letters* **35,** 57–59 (2014).

149. Gao, S. *et al.* Improving Unipolar Resistive Switching Uniformity with Cone-Shaped Conducting Filaments and Its Logic-In-Memory Application. *ACS applied materials & interfaces* **10,** 6453–6462 (2018).

150. Prakash, A. *et al.* Demonstration of low power 3-bit multilevel cell characteristics in a TaOx-based RRAM by stack engineering. *IEEE Electron Device Lett* **36,** 32–34 (2015).

151. Bai, Y. *et al.* Study of multi-level characteristics for 3D vertical resistive switching memory. *Scientific reports* **4,** 5780 (2014).

152. Kinoshita, K., Koh, S.-G., Moriyama, T. & Kishida, S. Finding Oxygen Reservoir by Using Extremely Small Test Cell Structure for Resistive Random Access Memory with Replaceable Bottom Electrode. *Scientific reports* **5,** 18442 (2015).

153. Traore, B. *et al.* HfO 2/Ti Interface Mediated Conductive Filament Formation in RRAM: An Ab Initio Study. *IEEE Transactions on Electron Devices* **65,** 507–513 (2018).

154. Rana, A. M. *et al.* Endurance and cycle-to-cycle uniformity improvement in tri-layered CeO 2/Ti/CeO 2 resistive switching devices by changing top electrode material. *Scientific reports* **7,** 39539 (2017).

155. Syu, Y.-E. *et al.* Atomic-level quantized reaction of HfOx memristor. *Applied Physics Letters* **102,** 172903 (2013).

156. Volos, C. K., Kyprianidis, I., Stouboulos, I., Tlelo-Cuautle, E. & Vaidyanathan, S. Memristor: A new concept in synchronization of coupled neuromorphic circuits. *Journal of Engineering Science and Technology Review* **8,** 157–173 (2015).

157. Woo, J. *et al.* Improved synaptic behavior under identical pulses using AlO x/HfO 2 bilayer RRAM array for neuromorphic systems. *IEEE Electron Device Letters* **37,** 994–997 (2016).

158. Serb, A. *et al.* Unsupervised learning in probabilistic neural networks with multi-state metal-oxide memristive synapses. *Nature communications* **7,** 12611 (2016).

159. Boybat, I. *et al. The key impact of incorporated Al2O3 barrier layer on W-based ReRAM switching performance* Paper accepted. 2019.

160. Shahrabi, E., Giovinazzo, C., Hadad, M., Ricciardi, C. & Leblebici, Y. *Switching kinetics control of W-based ReRAM cells in transient operation by interface engineering* Submitted paper.

161. Shao, X. L. *et al.* Electronic resistance switching in the Al/TiO x/Al structure for forming-free and area-scalable memory. *Nanoscale* **7,** 11063–11074 (2015).

162. Gemelli, E. & Camargo, N. Oxidation kinetics of commercially pure titanium. *Matéria (Rio de Janeiro)* **12,** 525–531 (2007).

163. Cifuentes, S. C., Monge, M. & Pérez, P. On the oxidation mechanism of pure tungsten in the temperature range 600–800 C. *Corrosion Science* **57,** 114–121 (2012).

164. Bricalli, A. *et al.* Resistive Switching Device Technology Based on Silicon Oxide for Improved ON–OFF Ratio—Part II: Select Devices. *IEEE Transactions on Electron Devices* **65,** 122–128 (2018).

165. Sokolov, A. S. *et al.* Comparative Study of Al2O3, HfO2, and HfAlOx for Improved Self-Compliance Bipolar Resistive Switching. *Journal of the American Ceramic Society* (2017).

166. Hirvikorpi, T., Vähä-Nissi, M., Harlin, A. & Karppinen, M. Comparison of some coating techniques to fabricate barrier layers on packaging materials. *Thin Solid Films* **518,** 5463–5466 (2010).

167. Aznilinda, Z., Herman, S. & Rusop, M. *Physical characteristic of room-temperature deposited TiO 2 thin films by RF magnetron sputtering at different RF power* in *Humanities, Science and Engineering Research (SHUSER), 2012 IEEE Symposium on* (2012), 685–689.

168. Naumann, V., Otto, M., Wehrspohn, R., Werner, M. & Hagendorf, C. Interface and material characterization of thin ALD-Al2O3 layers on crystalline silicon. *Energy Procedia* **27,** 312–318 (2012).

169. Hsu, C.-C., Sun, J.-K., Tsao, C.-C. & Chuang, P.-Y. Effects of Gibbs Free Energy of Iinterfacial Metal Oxide on Resistive Switching Characteristics of Solution-processed HfOx Films. *Physica B: Condensed Matter* **519,** 21–25 (2017).

170. Wang, L.-G. *et al.* Excellent Resistive Switching Properties of Atomic Layer-deposited Al 2O 3/HfO 2/Al 2 O 3 Trilayer Structures for Non-volatile Memory Applications. *Nanoscale research letters* **10,** 135 (2015).

171. Kim, K. M., Jeong, D. S. & Hwang, C. S. Nanofilamentary resistive switching in binary oxide system; a review on the present status and outlook. *Nanotechnology* **22,** 254002 (2011).

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