

Frequency- and time-domain analysis of high-frequency on-chip interconnects with nonuniform conductor edges

*Original*

Frequency- and time-domain analysis of high-frequency on-chip interconnects with nonuniform conductor edges / Manfredi, P., Vande Ginste, D., De Zutter, D.. - ELETTRONICO. - (2015), pp. 1-4. (IEEE 19th Workshop on Signal and Power Integrity (SPI 2015) Berlin (Germany) May 10-13) [10.1109/SaPIW.2015.7237392].

*Availability:*

This version is available at: 11583/2715103 since: 2018-10-15T19:28:00Z

*Publisher:*

Piscataway, N.J. : IEEE

*Published*

DOI:10.1109/SaPIW.2015.7237392

*Terms of use:*

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

*Publisher copyright*

(Article begins on next page)

# Frequency- and Time-Domain Analysis of High-Frequency On-Chip Interconnects with Nonuniform Conductor Edges

Paolo Manfredi, Dries Vande Ginste, and Daniël De Zutter

Electromagnetics Group, Department of Information Technology, Ghent University/iMinds  
Sint-Pietersnieuwstraat 41, 9000 Gent, Belgium

E-mail: paolo.manfredi@ugent.be

**Abstract**—In this paper we illustrate a modeling framework to analyze on-chip transmission lines affected by longitudinal nonuniformities in their conductor edges. The method consists of two steps. First, a macromodel for the frequency-dependent per-unit-length parameters is constructed based on an accurate field solver and it is used to conveniently obtain the pertinent place-dependent line parameters. Second, a fast and accurate perturbation technique is used to analyze the nonuniform transmission line problem. As shown by the application example, the proposed technique makes the statistical assessment for a large number of edge profiles feasible. Numerical results and discussions are provided for the case of an on-chip inverted embedded microstrip line.

**Index Terms**—Edge roughness, nonuniform transmission lines, on-chip interconnects, perturbation methods, statistical analysis.

## I. INTRODUCTION

The increase of operating frequencies and the simultaneous scaling of device dimensions are amplifying the impact of size effects in on-chip interconnects, like skin effect and conductor roughness, which require accurate modeling [1]. Specifically, as the cross-sectional interconnect dimensions are reduced, a non-negligible impact of conductor edge roughness is found on the electrical performance of on-chip and nanoscale interconnects [2]–[4]. Line-edge roughness (LER) is the longitudinal variation of the conductor edges and has many sources, including mask roughness and statistical phenomena like resist diffusion and chemical etching [5].

The effect of LER is inherently statistical and several stochastic models are available for its description. They mainly consist of either sinusoidal profiles [6]–[8] or correlated Gaussian processes [9]–[11]. The aforementioned works assess the impact of LER on the resistance and/or capacitance variations, and show a decreasing effect on longer interconnects due to averaging. However, a comprehensive modeling framework, accounting also for inductive effects and dielectric losses, and enabling an efficient statistical analysis of the overall signal integrity, seems yet to be missing.

The goal of this contribution is to cover this gap by putting forward a robust simulation framework to account for random longitudinal conductor edge variations in the interconnect simulation. The methodology is based on the construction of a macromodel for the resulting frequency- and place-dependent

per-unit-length (p.u.l.) parameters and on the application of a perturbation technique for the analysis of the pertinent nonuniform transmission line (NUTL) [12]. For the sake of simplicity, in this contribution the discussion is limited to a single signal line with a symmetric LER for its two edges. The approach is validated via the analysis of an inverted embedded microstrip (IEM) line in both the frequency and time domain.

## II. EDGE ROUGHNESS MODELING

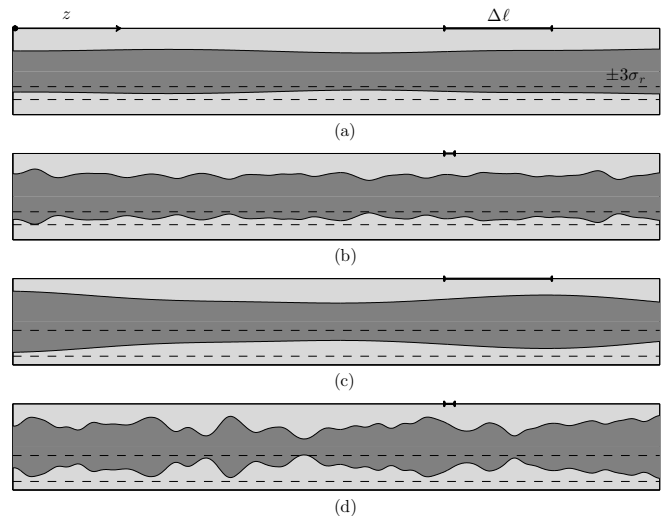


Fig. 1. Top view of conductor profiles for different LER parameters: (a) low  $\sigma_r$  and long  $\Delta\ell$ ; (b) low  $\sigma_r$  and short  $\Delta\ell$ ; (c) high  $\sigma_r$  and long  $\Delta\ell$ ; (d) high  $\sigma_r$  and short  $\Delta\ell$ . These parameters are illustrated on each plot.

The statistical properties of LER are usually described by at least two relevant parameters [5]: the absolute standard deviation  $\sigma_r$  of the conductor edge from its nominal cross-sectional position, and the correlation length  $\Delta\ell$  along the direction of propagation  $z$ . Fig. 1 visualizes four edge profiles obtained with different combinations of the aforementioned parameters. As shown by the figure, reducing the correlation length results in the edge to be longitudinally rougher, whereas the standard deviation affects the transverse variations. It is possible to extract these parameters from real profiles, measured with a scanning electron microscope [5].

As the geometry of the conductor is nonuniform along the longitudinal coordinate  $z$ , an interconnect affected by LER is in fact a NUTL and it is described by the following Telegrapher's equations [13]:

$$\frac{d}{dz}\hat{V}(\omega, z) = -\hat{Z}(\omega, z)\hat{I}(\omega, z) \quad (1a)$$

$$\frac{d}{dz}\hat{I}(\omega, z) = -\hat{Y}(\omega, z)\hat{V}(\omega, z) \quad (1b)$$

where  $\hat{V}$  and  $\hat{I}$  denote the phasors of the voltage and current along the line, whereas  $\hat{Z} = R(\omega, z) + j\omega L(\omega, z)$  and  $\hat{Y} = G(\omega, z) + j\omega C(\omega, z)$  are the frequency- and place-dependent p.u.l. parameters, which are function of the conductor cross-sectional geometry at a given point along  $z$ . In the sequel, the argument  $\omega$  that explicitly expresses the frequency dependency, will be dropped for notational brevity.

Two issues arise for the modeling of a transmission line with LER via (1). First, no closed-form solution exists for (1). The typical strategy for the determination of the voltage and current is to subdivide the line into short and locally uniform sections and to concatenate the respective chain-parameter matrices (CPMs) [13]. This is here referred to as the ‘‘CPM approach’’, which turns out to be computationally inefficient as the number of discretizations needed is usually high, especially for rapid variations as those occurring in rougher edge profiles. Second, the direct evaluation of the p.u.l. parameters in each section is even more computationally demanding, as it requires accurate field calculations [14].

These two problems are overcome by constructing a macromodel for the p.u.l. parameters and by solving the NUTL equation via a perturbation technique, as shown in the following sections.

#### A. Macromodel of the Per-Unit-Length Parameters

We define the LER profile as the longitudinal variation  $\delta(z)$  of the conductor edge from its nominal position. This is modeled as a Gaussian random process with zero mean and squared exponential autocorrelation function:

$$K(z, z') = \sigma_r^2 \exp\left(-\frac{|z - z'|^2}{2\Delta\ell^2}\right) \quad (2)$$

Moreover, we introduce the deviation normalized w.r.t. the roughness standard deviation  $\sigma_r$ , i.e.

$$\xi = \xi(z) = \frac{\delta(z)}{\sigma_r} \quad (3)$$

It should be noted that with the introduced assumptions and the above definitions, the actual conductor width at a given position  $z$  is

$$w(z) = \bar{w} + 2\delta(z) = \bar{w} + 2\sigma_r\xi(z), \quad (4)$$

where  $\bar{w}$  denotes the nominal width.

A macromodel is constructed for the p.u.l. parameters  $\hat{Z}$  and  $\hat{Y}$  as a function of the normalized deviation  $\xi$  by means

of a Lagrange interpolation [15]:

$$\hat{Z} \approx \sum_{k=1}^K \hat{Z}(\xi_k) \Phi_k(\xi) \quad (5a)$$

$$\hat{Y} \approx \sum_{k=1}^K \hat{Y}(\xi_k) \Phi_k(\xi) \quad (5b)$$

where the coefficients  $\hat{Z}(\xi_k)$  and  $\hat{Y}(\xi_k)$  are the p.u.l. parameters calculated at the interpolation nodes  $\{\xi_k\}_{k=1}^K$  based on the actual conductor width (4), whilst the functions  $\Phi_k$  are the corresponding Lagrange polynomials, i.e.

$$\Phi_k(\xi) = \prod_{\substack{1 \leq j \leq K \\ j \neq k}} \frac{\xi - \xi_j}{\xi_k - \xi_j}, \quad k = 1, \dots, K \quad (6)$$

Owing to the Gaussian distribution of the edge variations, we use as interpolation nodes the zeros of Hermite polynomials [15]. A macromodel based on  $K = 6$  interpolated samples is constructed, resulting in an error less than 0.2% over the interval  $[-3\sigma_r, +3\sigma_r]$  and 1.7% over the interval  $[-4\sigma_r, +4\sigma_r]$ , up to a frequency of 100 GHz. It is important to point out that a single calculation of  $\hat{Z}$  and  $\hat{Y}$  requires about 5 min. Therefore, it is virtually impossible to directly calculate many place-dependent p.u.l. parameters along the entire line length, as would be needed in a brute-force analysis. Yet, once the macromodel is available, it suffices to generate a suitable LER profile  $\delta(z)$  and sample (5) to inexpensively obtain them.

#### B. Perturbation Technique for the Nonuniform Transmission Line

The problem of solving a NUTL like (1) is converted into the solution of a uniform transmission line with distributed sources by means of the perturbation technique described in [12]. The place-dependent  $\hat{Z}$  and  $\hat{Y}$  are interpreted as a perturbation w.r.t. a reference value, corresponding to their average along  $z$ :

$$\hat{Z}(z) = \hat{Z}_0 + \Delta\hat{Z}(z) = \frac{1}{\ell} \int_0^\ell \hat{Z}(z) dz + \Delta\hat{Z}(z) \quad (7a)$$

$$\hat{Y}(z) = \hat{Y}_0 + \Delta\hat{Y}(z) = \frac{1}{\ell} \int_0^\ell \hat{Y}(z) dz + \Delta\hat{Y}(z) \quad (7b)$$

A second-order perturbation is introduced for the voltage and current along the line, i.e.

$$\hat{V}(z) \approx \hat{V}_0(z) + \hat{V}_1(z) + \hat{V}_2(z) \quad (8a)$$

$$\hat{I}(z) \approx \hat{I}_0(z) + \hat{I}_1(z) + \hat{I}_2(z) \quad (8b)$$

where  $\hat{V}_0$  and  $\hat{I}_0$  are the solution of the uniform ‘‘unperturbed’’ line

$$\frac{d}{dz}\hat{V}_0(z) = -\hat{Z}_0\hat{I}_0(z) \quad (9a)$$

$$\frac{d}{dz}\hat{I}_0(z) = -\hat{Y}_0\hat{V}_0(z) \quad (9b)$$

whilst  $\hat{V}_i$  and  $\hat{I}_i$ ,  $i = 1, 2$ , are the solutions of

$$\frac{d}{dz}\hat{V}_i(z) = -\hat{Z}_0\hat{I}_i(z) - \Delta\hat{Z}(z)\hat{I}_{i-1}(z) \quad (10a)$$

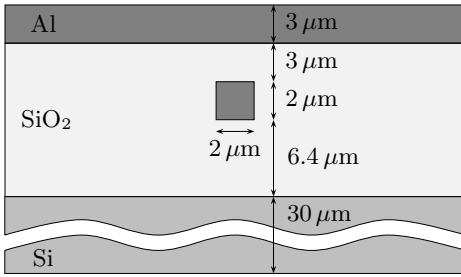
$$\frac{d}{dz}\hat{I}_i(z) = -\hat{Y}_0\hat{V}_i(z) - \Delta\hat{Y}(z)\hat{V}_{i-1}(z) \quad (10b)$$

where the additional terms on the right-hand side play the role of distributed sources [13]. Closed-form expressions are available for  $\hat{V}_i$  and  $\hat{I}_i$  [12].

### III. APPLICATION EXAMPLE

The proposed application example refers to the IEM line shown in Fig. 2, where all the relevant geometrical and material parameters are indicated. It consists of an aluminum signal conductor embedded in a silicon dioxide layer on a silicon substrate, and with an aluminum ground plane on top. The displayed width of  $2\ \mu\text{m}$  is the desired nominal width  $\bar{w}$ . The line is 1-mm long.

For the sake of simplicity, a solid ground plane is considered, although mesh-type grounds are often adopted for on-chip lines [16]–[18]. By assuming a periodic structure for the mesh, this case can be treated in a similar fashion as fiber weave structures in [19].



Al:  $\sigma = 3.77 \cdot 10^7\ \text{S/m}$   
SiO<sub>2</sub>:  $\epsilon_r = 3.9$ ,  $\tan \delta = 0.001$   
Si:  $\epsilon_r = 11.7$ ,  $\sigma = 10\ \text{S/m}$

Fig. 2. Cross-section of the IEM line for the considered application example.

#### A. Frequency-Domain Analysis

A frequency-domain analysis is carried out first. To statistically assess the impact of LER, 1000 random profiles are generated by considering  $\sigma_r = 0.1\ \mu\text{m}$  and  $\Delta\ell = 5\ \mu\text{m}$ . Fig. 3 shows the magnitude and phase of the corresponding  $S_{11}$  (solid gray lines), thus illustrating the spread of the response due to LER. The S-parameters are obtained from the total voltage and current (8) at the line ends ( $z = 0$  and  $z = \ell$ ), calculated for  $50\text{-}\Omega$  terminations [20]. The components  $V_{0,1,2}$  and  $I_{0,1,2}$  are determined using the formulas in [12].

Furthermore, the 99% bounds, obtained from the cumulative distribution function of the samples, are also indicated in Fig. 3 (solid black lines). For comparison, the bounds computed by solving the NUTL (1) with the CPM approach are also shown (dashed gray lines). The two results are indistinguishable. Nonetheless, the repeated solution with the CPM method takes

6515 s on an ASUS U30S laptop with an Intel(R) Core(TM) i3-2330M, CPU running at 2.20 GHz and 4 GB of RAM, as opposed to the 409 s required by the perturbation technique. Therefore, a relevant speed-up of  $16\times$  is achieved by adopting the latter.

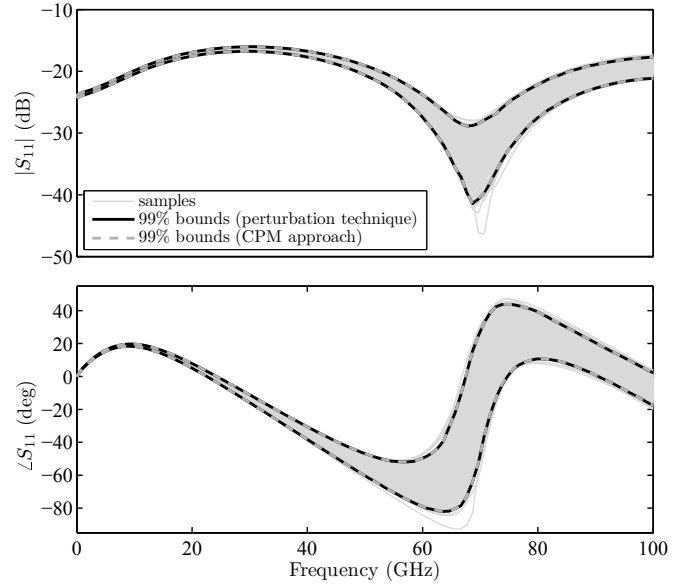


Fig. 3. Magnitude and phase of  $S_{11}$  for the 1-mm long IEM line of Fig. 2. The solid gray lines show the spread of the response due to LER; the solid black and the dashed gray lines highlight the  $\pm 3\sigma$  bounds obtained by using the perturbation technique and the CPM approach, respectively.

#### B. Time-Domain Analysis

Next, the time-domain response to a step voltage source of 1 V, with an internal resistance of  $1\ \Omega$  and a risetime of 50 ps, is simulated. The load is a 1-pF capacitor. The results are obtained via a Fourier analysis with 100 harmonics.

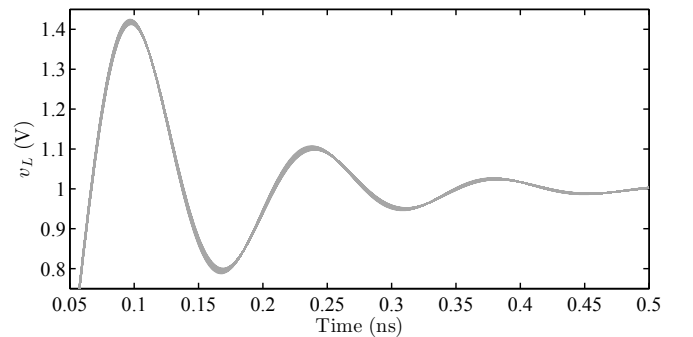


Fig. 4. Step response of the IEM line subject to LER.

Fig. 4 shows the voltage  $v_L$  transmitted to the far end of the line. The LER parameters are in this case the same as for the frequency-domain analysis and cause an appreciable variation of the voltage waveform, although the dominant effect is here the ringing, caused by the combination of the inductances of the line and the capacitive load. Therefore, to

better highlight the impact of the roughness parameters, the probability density function (PDF) of the voltage maximum overshoot, occurring at around 0.1 ns, is simulated for different correlation lengths  $\Delta\ell$ . The results in Fig. 5 show that for shorter correlation lengths (i.e., rougher profiles) the range of the voltage variation is narrower. This is because the effect of LER tends to be averaged out. Such a behavior is in agreement with literature results [6]–[11].

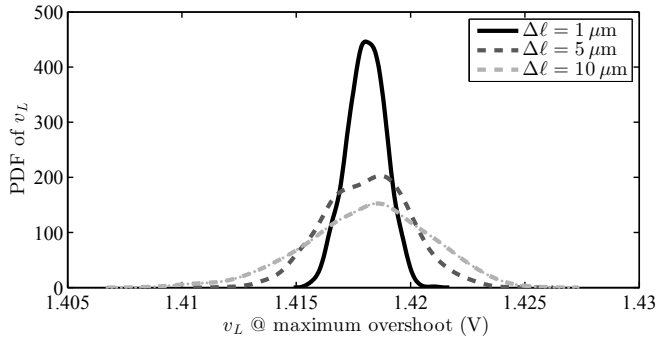


Fig. 5. PDF of the voltage maximum overshoot obtained for various roughness correlation lengths.

#### IV. CONCLUSIONS

This contribution introduces a comprehensive modeling framework for on-chip interconnects affected by LER. Being based on Telegrapher’s equation with dispersive RLGC parameters, it also allows to capture all the relevant electrical (e.g. skin and slow-wave) effects, resulting in an accurate statistical signal integrity analysis.

The method is based on the creation of a macromodel of the p.u.l. parameters as a function of the edge variation from its nominal position. This allows to inexpensively obtain the longitudinally varying line parameters, whereas the direct calculation would be virtually impossible. Furthermore, a perturbation technique is adopted to solve the equations for the resulting NUTL. This second step introduces an additional, significant computational advantage. The combination of these two elements makes a repeated-run statistical analysis for several LER profiles feasible and tractable.

The effectiveness of the proposed approach is demonstrated by analyzing an IEM on-chip line. The frequency-domain behavior in presence of LER is assessed and the impact of LER’s correlation length on the time-domain response variability is discussed.

In future work, the method will be extended to multiconductor lines, where a non-negligible effect of LER on crosstalk is also expected.

#### ACKNOWLEDGMENT

This work was supported by the Research Foundation Flanders (FWO-Vlaanderen). Paolo Manfredi is a Post-Doctoral Research Fellow of FWO-Vlaanderen.

#### REFERENCES

- [1] B. Curran, I. Ndip, S. Guttowski, and H. Reichl, “A methodology for combined modeling of skin, proximity, edge, and surface roughness effects,” *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 9, pp. 2448–2455, Sep. 2010.
- [2] W. Steinhögl, G. Schindler, G. Steinlesberger, M. Traving, and M. Engelhardt, “Impact of line edge roughness on the resistivity of nanometer-scale interconnects,” *Microelectronic Eng.*, vol. 76, no. 1–4, pp. 126–130, Aug. 2004.
- [3] M. Stucchi, M. Bamal, and K. Maex, “Impact of line-edge roughness on resistance and capacitance of scaled interconnects,” *Microelectronic Eng.*, vol. 84, no. 11, pp. 2733–2737, Nov. 2007.
- [4] G. G. Lopez, “The impact of interconnect process variations and size effects for gigascale integration,” Ph. D. dissertation, Georgia Institute of Technology, Atlanta, GA, USA, Dec. 2009.
- [5] K. Patel, S. N. Lahiri, and C. J. Spanos, “Robust estimation of line width roughness parameters,” *J. Vacuum Sci. Technology B*, vol. 28, no. 6, pp. 18–33, Nov. 2010.
- [6] G. Lopez, R. Murali, R. Sarvari, K. Bowman, J. Davis, and J. Meindl, “The impact of size effects and copper interconnect process variations on the maximum critical path delay of single and multi-core microprocessors,” in *Proc. IEEE Int. Interconnect Technology Conference*, Burlingame, CA, USA, Jun. 2007, pp. 40–42.
- [7] G. Lopez, J. Davis, and J. Meindl, “A new physical model and experimental measurements of copper interconnect resistivity considering size effects and line-edge roughness (LER),” in *Proc. IEEE Int. Interconnect Technology Conference*, Sapporo, Japan, Jun. 2009, pp. 231–234.
- [8] T. Kurusu, H. Tanimoto, M. Wada, A. Isobayashi, A. Kajita, N. Aoki, and Y. Toyoshima, “Impact of line-edge roughness on electrical resistivity in decananoscale copper wires: a Monte Carlo study,” in *Proc. Int. Conference on Simulation of Semiconductor Processes and Devices*, Denver, CO, USA, Sep. 2012, pp. 304–307.
- [9] F. J. Twaddle, D. R. S. Cumming, S. Roy, A. Asenov, and T. D. Drysdale, “RC variability of short-range interconnects,” in *Proc. Int. Workshop on Computational Electron.*, Beijing, China, May 2009, pp. 1–3.
- [10] Y. Bi, P. Harpe, and N. P. van der Meijs, “Efficient sensitivity-based capacitance modeling for systematic and random geometric variations,” in *Proc. 16th Asian and South Pacific Design Automation Conference*, Yokohama, Japan, Jan. 2011, pp. 61–66.
- [11] W. Yu, Q. Zhang, Z. Ye, and Z. Luo, “Efficient statistical capacitance extraction of nanometer interconnects considering the on-chip line edge roughness,” *Microelectronics Rel.*, vol. 52, no. 4, pp. 704–710, Apr. 2012.
- [12] M. Chernobryvko, D. De Zutter, and D. Vande Ginste, “Nonuniform multiconductor transmission line analysis by a two-step perturbation technique,” *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 4, no. 11, pp. 1838–1846, Nov. 2014.
- [13] C. R. Paul, *Analysis of Multiconductor Transmission Lines*, 2nd ed. Hoboken, NJ: Wiley, 2008.
- [14] T. Demeester and D. De Zutter, “Quasi-TM transmission line parameters of coupled lossy lines based on the Dirichlet to Neumann boundary operator,” *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 7, pp. 1649–1660, Jul. 2008.
- [15] P. Manfredi, I. S. Stievano, and F. G. Canavero, “Prediction of stochastic eye diagrams via IC equivalents and Lagrange polynomials”, in *Proc. IEEE 17th Workshop on Signal and Power Integrity*, Paris, France, May 2013, pp. 1–4.
- [16] C.-H. Chan and R. Mittra, “The propagation characteristics of signal lines embedded in a multilayered structure in the presence of a periodically perforated ground plane,” *IEEE Trans. Microw. Theory Techn.*, vol. 36, no. 6, pp. 968–975, Jun. 1988.
- [17] A. C. Cangellaris, M. Gribbons, and J. Prince, “Electrical characteristics of multichip module interconnects with perforated reference planes,” *IEEE Trans. Compon. Hybrids, Manuf. Technol.*, vol. 16, no. 1, pp. 113–118, Feb. 1993.
- [18] S. Luo, J.-M. Jang, and V. K. Tripathi, “Crosstalk in coupled interconnects with meshed ground planes,” in *Proc. IEEE Multi-Chip Module Conf.*, Santa Cruz, CA, USA, Mar. 1994, pp. 132–137.
- [19] M. Chernobryvko, D. Vande Ginste, and D. De Zutter, “A perturbation technique to analyze the influence of fiber weave effects on differential signaling,” in *Proc. IEEE 22nd Conf. Elect. Perform. Electron. Packag. Syst.*, San Jose, CA, Oct. 2013, pp. 15–18.
- [20] D. M. Pozar, *Microwave Engineering*, 4th ed. Hoboken, NJ: Wiley, 2012.