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Design and testing of CMOS radiation detectors for High Energy Physics Experiments

By

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Declaration

I hereby declare that, the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

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Said the straight man
to the late man
"Where have you been?"
"I've been here and
I've been there and
I've been in between"

Abstract

In recent years, the study and the development of novel architectures and technologies to improve performance of silicon pixel detectors became a pivotal node for High Energy Physics (HEP) experiments. Their extremely tight constraints of spatial resolution, low power dissipation, speed, granularity, signal-to-noise ratio and radiation hardness, led the scientific community to continuously research new solutions to satisfy newer and more stringent requirements. In this context, the two main categories of detectors technologies have been represented by Hybrid Pixel Detectors (HPDs) and Monolithic Active Pixel Sensors (MAPS).

Traditionally, HPDs constitute the more widespread technology for particle pixel detectors: due to their excellent characteristics, they are adopted for the inner layers of the most of current main HEP experiments. However, on the other side, the relatively novel monolithic sensors technology became recently more and more interesting as leading replacing technology due to its improved radiation hardness and the lower material budget and cost with respect to HPDs.

In this thesis an introduction to these technologies will be carried out and some related research results will be shown.

In Chapter 1 Hybrid Pixel Detectors technology will be described, with an additional part dedicated to some literature examples about HEP experiments which adopted this kind of sensors for their inner layers. This chapter acts as an introduction to the CHIPIX65 (***CHI****p for* ***PIX****el detector in a* ***65*** *nm process*) prototype shown in Chapter 3 and to the Phase-Locked Loop described in Chapter 5.

In Chapter 2 MAPS (Monolithic Active Pixel Sensors) technology will be introduced, from the early prototypes based on 3-T and 4-T architecture until the last examples of monolithic sensors implemented inside more recent particle detectors upgrades. This part is preparatory to Chapter 5, where the MATISSE prototype is described both to the development and to the testing point of view.

Chapter 3 is dedicated to CHIPIX65 project and the development of a novel prototype of an 65 nm CMOS HPD: realized in collaboration of some INFN Italian groups, this is the first example of HPD fully developed in a sub-micron CMOS technology. Starting with a short introduction to architecture and readout modes, this chapter shows some important testing results presented in Strasbourg during an IEEE MIC-NSS Conference talk in 2016.

Chapter 4 is fully dedicated to a low-noise and compact Phase-Locked Loop (PLL) built in the same 65 nm CMOS technology. After some theoretical and introductory sections, the prototype will be described and test results provided.

Chapter 5 is fully dedicated to the development and test of a prototype of MAPS, called MATISSE (***M****onolithic* ***A****c****TI****ve pixel* ***S****en****S****or* ***E****lectronics*). Developed by INFN groups of Turin and Padua, University of Trento and TIFPA, it is an example of a fully-depleted monolithic active sensor. Here, some sensor and readout electronics will be described, followed by some tests. These results have been presented during a poster session in Atlanta during the IEEE MIC-NSS Conference in 2017.

Appendices will cover some follow-up topics related to the previous sections.

Appendix A summarizes radiation effects on silicon devices, both total dose and heavy-ions effect: this section is useful to referring to all the parts related to radiation hardness tests of described prototypes.

Appendix B outlines some practical guidelines about Process Design Kit (PDK) of a given technology process. Indeed, before starting the design of any ASIC device, a PDK needs to be provided by the foundry, installed and configured in order to allow to work with.

Appendix C is dedicated to some theoretical issues on oscillator phase noise, which represent a huge subject in Phase-Lock Loop theory; however, since it is not covered by the analysis and tests on the PLL prototype, it has been chosen to put this part separately to Chapter 4.

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Chapter 1

Hybrid pixel detectors

1.1 Introduction to hybrid pixel detectors

The development of LHC detectors, where remarkable speed and radiation hardness constraints are required, has promoted an astound growth of the Hybrid Pixel Detectors (HPDs)[9]. From the point of view of fabrication, even though very similar to microstrip detectors' ones, HPDs show an higher segmentation by splitting the original strip structure into small parts called, indeed, *pixels*.
Detecting sensors and their front-end electronics chip belong to two different pieces and they are processed and optimized separately [10]. Usually, the read-out electronics is developed in some commercial CMOS process, which facilitates huge and low-cost production. In order to extract the signal from the front-end, some ancillary logic is needed with organizing and off-chip transmission purposes. These logic parts generally are not distributed along the pixel matrices but they are concentrated all together and put close to the chip. On the other hand, detecting sensor is generally developed with high-resistivity silicon but also other materials are considered, such as diamond [11]. The solding with these two parts is achieved by means of the flip-chip bonding technique [12] where the mechanical and electrical connection between the two is established by some small solder balls (gold, indium or other metals are utilized). The connectivity between sensor and front-end electronics must be vertical in order to allow them to stay very close (10-20 μm). Furthermore, the pixel size must match with the size of its corresponding electronics. This proximity

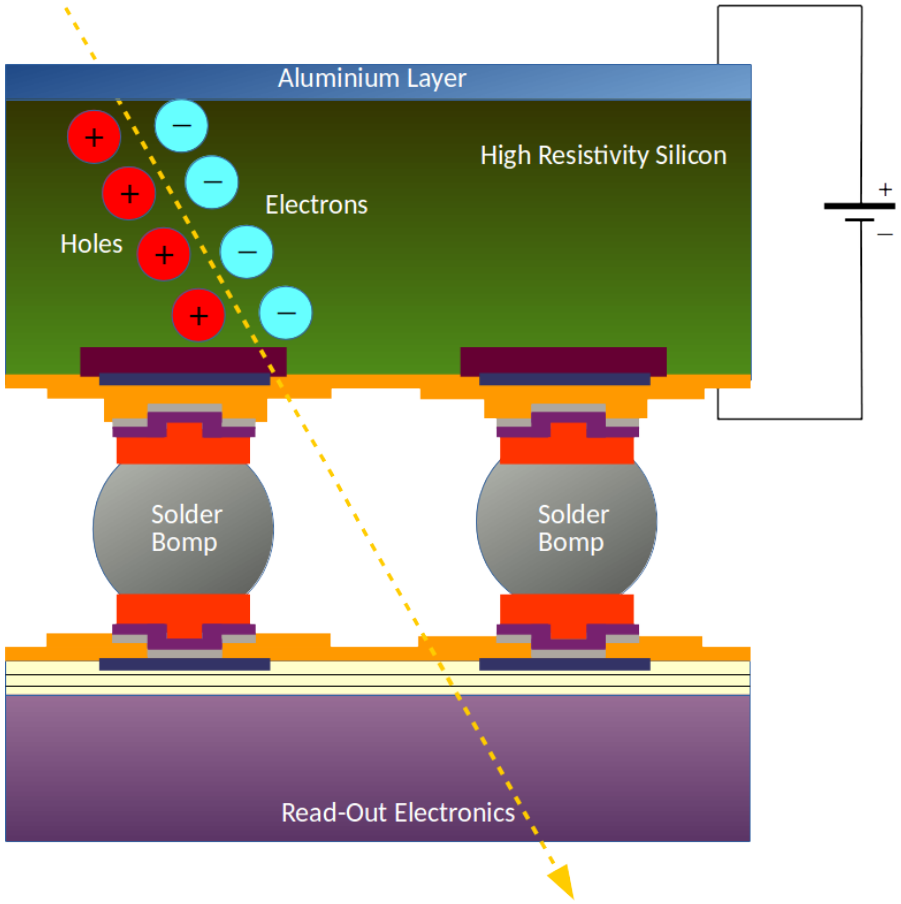


Figure 1.1: Section of a generic hybrid pixel detector.

may cause some issues which need some special attention during the design phase:

- spurious signals due to high-frequency signals on the electronics detected on the metalization of the pixel. This phenomenon may be contained by reducing the coupling capacitance between digital lines and sensor and by utilizing low-swing logic (such as LVDS);

- destructive sparks due to static voltage (e.g. bias voltages) on the edges or front-side of the sensor may damage the front-end electronics. For this reason, some specific structures (*guardrings*) are utilized with the aim to confine the high voltage parts on the sensor's backside.

The small dimension of the sensing unity - the pixel - represents the main characteristic of HPDs. Actually, each pixel is fabricated with a thin silicon layer ($\approx$300 μm) and occupies a small area ($\approx 10^{-4}$ cm^2). Thanks to the low capacitance ($\approx$0.2-

0.4 pF), HPDs stand out for low noise and fast signal shaping.
Common noise values are around 200 e^- for 40 MHz operating frequencies; a good choice of detection threshold (i.e. 10 σ noise) may ensure that noise fluctuations do not cross the threshold, maintaining a full efficiency at the same time with an extremely low probability to incur in spurious hits [13].
Additionally, a good Signal-To-Noise Ratio (SNR) implies for the detector the needed robustness for remarkable loss of signal. Even though the huge complexity

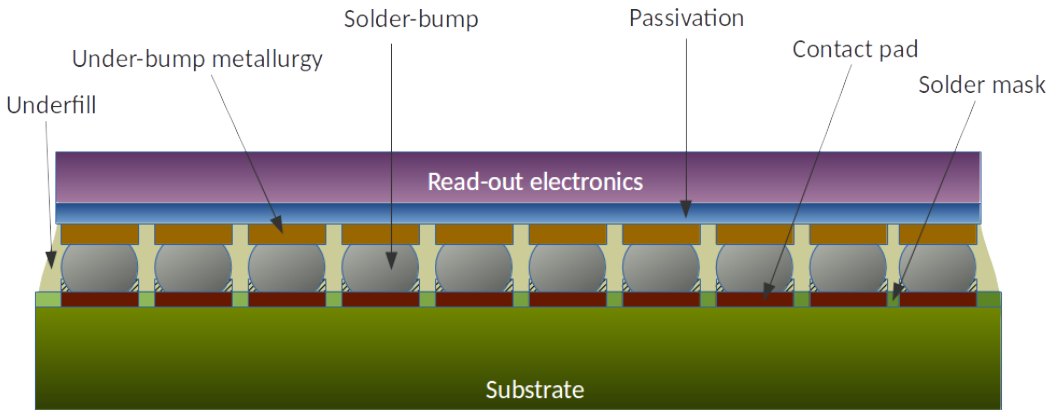


Figure 1.2: Flip-chip technique.

of interconnections and functionalities, HPDs allows an excellent resolution of the acquired signals, this entails an high power dissipation (by approximately few hundreds mW/cm^2), more material for the active areas and larger pixels' size since more space for readout circuitry is needed.
A solution can be found into taking advantages by material sensors with thin active depth, such as GaAs, CdZnTe or diamond, which are, however, characterized by meager collection of the charge; alternatively, silicon sensors which may be degraded by radiation and thus reduce the charge collection due to carriers' trapping phenomena. Furthermore, the small dimension of the pixel leads to small reverse depletion current (in the order of 0.1 μA/cm^2): this allows operation after irradiation due to reduced noise. This makes HPDs the appropriate detector for harsh radiation environment.
HPDs have demonstrated their worth in the field of huge HEP detector, where the need to cover square meters of sensitive area with millions of channels for extremely intense particle fluxes occurs. Their characteristics and the freedom to choose the sensitive material makes them a preferred technology also in other fields, such as

medical diagnostics [14].

Advantages	Disadvantages
high space and time resolution	extra material (due to the flip-chip)
speed	high power dissipation
radiation hardness	high costs (solding)
non-ambiguous 3D measurements	two different foundry processes (sensor and FEE)

Table 1.1: Advantages and disadvantages of HPDs.

1.1.1 Some examples

As said before, HPDs represent the main detector tipology for High Energy Physics experiments. Following, a round-up of some readout chips based on HPDs.

1.1.1.1 FPix2

FPix2 [15] is the rad-hard chip developed for the BTeV experiment at Fermilab [16]. BTeV was proposed for the CZero interaction region of the Tevatron [17] and it was intended to collect data from a pixel vertex detector by reconstructing vertices and tracks for each beam crossing. The detector requirements pertain in particular to the extreme radiation hardness ($\approx$ 3Mrad/year), to be SEE tolerant and to the capability to sustain very high leakage currents. Radiation hardness techniques has been implemented in order to accomplish to this crucial requirement [18]. Furthermore, given the Tevatron time between proton-antiproton interactions (132 ns), the FPix2 needed to be designed to guarantee no data losses due to the readout deadtime. In addition to that, enough bandwidth is needed in order to collect all the data (since the trigger needs all pixel data each crossing) and a high-speed zero suppression system to manage the high data quantity. The vertex detector was intended to be made of sensors arrays perpendicular to the direction of the beam.
Built in a commercial CMOS 250 nm, the pixel matrix is composed by 22$\times$128 pixels; the pixel size is 50$\times$400 μm^2. The chip needs just 2.5 V supply and ground signal, since all the other ones (current and voltages bias, thresholds) are on-chip generated by some DACs. For the I/O interface, FPix2 is equipped with standard

Parameter	**Value**
CMOS technology process	250 nm
Pixel size	50×400 μm^2
Matrix array	22×128 pixels
I/O interface	LVDS
Voltage Supply	2.5 V

Table 1.2: FPix2 parameters summary.

LVDS protocol.
As said before, all the pixels are read and their data readout each beam crossing. All the pixel hits are sent, every readout period, to a Pixel Data Combiner Board on a FPGA located far off the collision ($\approx$10 meters). A 140 Mbps serial link is used to send off-chip all the data using a point-to-point serial way. In order to modulate the required bandwidth by the section of the detector (from the closest to the further from the collision), the output serial link can be programmed in four different modes.

The pixel unit cell consists in a continuous-time-filter amplifier with a 3-bit flash ADC, composed by eight comparators and some digital circuitry to encode the output of the ADC and store the data related to the hits. This last information is preserved until a signal coming from the EoC allows to transmit them to the output interface. The data word sent on a core output-bus is 23-bit long and it is made of the 7-bit row number, the 3-bit ADC value plus thirteen bits added by the EoC (a 5-bit column number and an 8-bit time-stamp, also called the BCO number); data from 1^{st} to 13^{th} bit cannot be zero: for this reason the numbers of 22 columns are encoded on five bits by using binary code without zeroes in lowest positions. The data are then serialized and sent off-chip [18].
A synchronization/status word is used to synchronize the chip with the data combiner board which checks its correctness as well: the readout is performed column by column in a round-robin way. The output of the chip is managed using Low Voltage Differential Signaling (LVDS) and consists in a clock signal and in a programming number corresponding to the position of the chip with respect to the collision point: it can be 1, 2, 4 or 6 respectively from the further to the closest to collision position; thus, each number corresponds to a different internal readout clock frequency (1 to 5.8 MHz, 2 to 11.7 MHz, 4 to 23.3 MHz, 6 to 35 MHz); this frequency derives by the

transfer bit rate divided by the word size (24 bit) and the number of active data links. Data output clock and readout clock are originated from a 70 MHz internal clock. The equality between the time required to send data off chip and time required to readout is guaranteed by the relationship between the number of data links used and internal readout clock: one clock period is needed to send off chip one word.

1.1.1.2 Topix v4

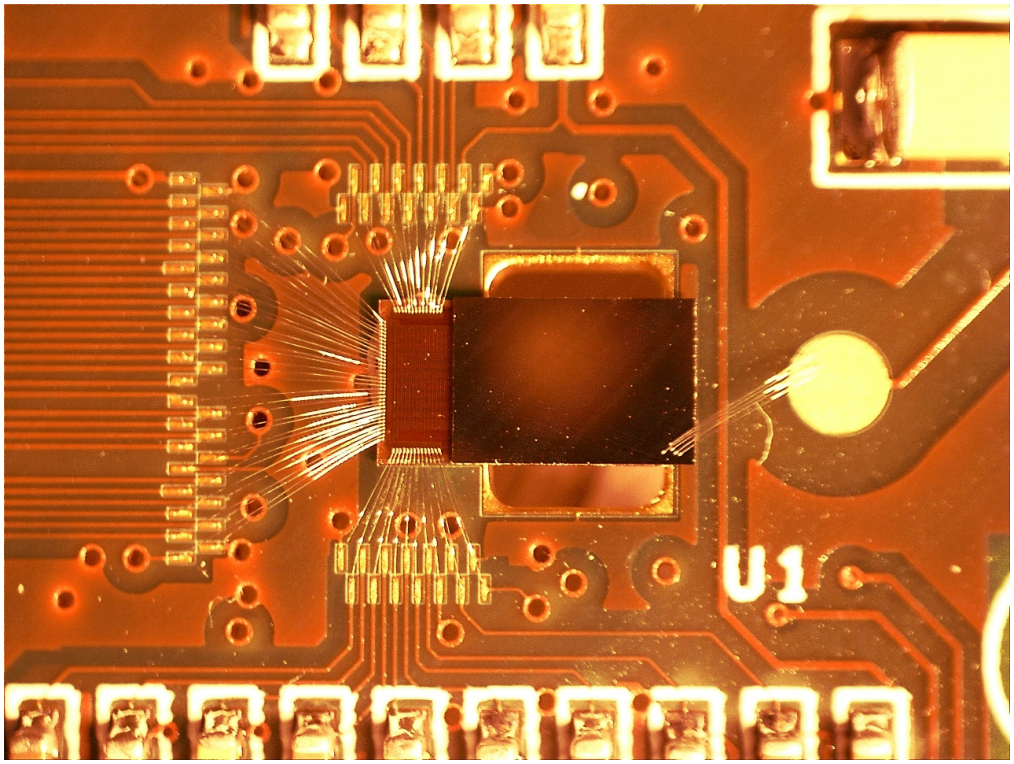


Figure 1.3: ToPix v4 close-up.

In the framework of the Micro Vertex Detector of PANDA [19] experiment, ToPix v4 ASIC [20] has been developed for the readout of the silicon hybrid pixel detectors. Designed in a commercial 130 nm CMOS process, the prototype shows a 640 pixel matrix organized in 8 columns; the die size is 6 mm $\times$3 mm.
While the full chip should be consisted into a 116$\times$110 pixel matrix arranged in 55 double columns, with four full column controllers and a Chip Control Unit (CCU), whose purpose is to multiplex data from the column controllers to the GBT chip by mean of a 320 Mb/s serial link, the prototype consists into a smaller matrix of

just 640 pixels organized in four double columns with different size arrangements (the two central ones are 2×128 pixels, while the other ones are 2×32 pixels; this allows to analyze issues of the data transmission in very long on-chip lines) with a simplified CCU and with a dedicated time stamp circuitry with a 160 MHz frequency for time arrival measurements. In order to measure released energy, a ToT technique is implemented: in such a way, Topix v4 is able to return information about time, position and energy of the incoming particle. The readout chain is based on a 4.9 fF

Parameter	**Value**
CMOS technology process	130 nm
Pixel size	100×100 μm^2
Active area	11.4×11.6 mm^2
Maximum input charge	50 fC
Power consumption	< 800 mW/cm^2
Preamplifier noise	< 32 aC (200 e$^-$)
Time resolution	6.25 ns (1.8 ns rms)
Input clock frequency	160 MHz
Maximum hit rate	6.1×10^6/cm^2
dE/dx measurement	ToT, 12 bits dynamic range
Total ionizing dose	< 100 kGy

Table 1.3: ToPix v4 parameters summary.

feedback preamplifier with a constant current discharge circuit and a comparator. Detection of the comparator output falling and rising edges and their storing of time-stamps into two 12 bit registers is managed by a digital control unit. Then, a dedicated bus distributes the time reference to all columns. A time-over-threshold technique is used for the measure of the charge released in the detector by the particle: since a capacitor discharges linearly, the difference between the two edges of this pulse of the comparator is related to the integrated charge released into the detector by the incident particle. Once this information is stored, a busy signal by mean of a fast-OR chain is propagated along the columns; the column controller enables the writing of the address and the data of the hit pixel. Since the logic is asynchronous, the 160 MHz clock is not propagated to all the pixel of the array. For a better calibration of the threshold of the comparator and for pixel masking purposes, a configuration register is provided: its configuration values are uploaded during the time preceding the phase dedicated to pixel data collecting by using the time

stamp bus. The time stamp propagation is improved by mean of some techniques, such as pre-emphasis, Gray encoding and differential transmission on the bus, which can be demanding in terms of RC delay even though the low values of capacitance and resistance. A 32 word FIFO is connected to each double column readout buses; the CCU performs the readout of those FIFOs and sends out the data with a 320 Mb/s SLVS serial link. For what concerns the I/O, on the top and bottom of the die some test pads and analog bias are located; all the pads of the digital interface are differential and put on the right side. In order to test the radiation tolerance of the chip ToPix v4 prototype has been irradiated up to 100 kGy of TID and under several ions type in order to check SEE hardness. Detailed report could be found in [20].

1.1.1.3 TimePix3

Timepix3 is the enhanced version of Timepix [21][22]. Designed by CERN, NIKHEF (Netherlands) and University of Bonn (Germany), it is based on a CMOS 130 nm process. Similarly to Timepix [23] (which indeed is based on a CMOS 250 nm process), it consists in a 256×256 matrix with a 55 μm pitch in both directions. It is capable to provide time to arrival (ToA), Time-Over-threshold (ToT) or event/photon counting measurement (called PC). Differently to Timepix, it is able to perform ToA and ToT or PC or iToT (integral ToT) at the same time.
Timepix3 can operate in two main modes: ToT with ToA or PC with iToT.
In the first mode, each pixel is able to record 10 bits for the ToT and 18 bits for the ToA. A 40 MHz reference clock is used to sample the most significant 14 bits, while the last 4 bits are measured by mean of a VCO (Voltage Controlled Oscillator) inside the pixel matrix. In the second mode, a 14 bit register is used to store the integrated values of the ToT during a period determined by an external shutter signal; another 10 bits register is implemented to store the number of hits. A different requirement between Timepix and Timepix3 is the monotonicity of the input charge vs ToT up to 300k holes (positive charge).
The readout can be performed in two ways as well. The first is a classical sequential shutter period readout. The last one is a data-driven mode readout: when a pixel is hit, the chip sends off chip a 48 bits string. Pixel are then gathered together in 2×4 pixels groups which may be called ”superpixel”. Each superpixel group has a dedicated VCO which generates a 640 MHz local clock, used for ToA measurements

Parameter	Value
CMOS technology process	130 nm
Matrix	256×256 pixels
Pitch	55μm
Analog FEE Area	55×13.5 μm^2
Detector Capacitance	min 25 fF typ 50 fF max 100 fF
Polarity of the signal	positive and negative
Monotonicity of the ToT	up to 300 kh$^+$
Leakage current	from -5 nA to 20 nA
Jitter and mismatch of ToA	1.56 ns resolution compatibility
Amplitude linearity	not required
Time to peak	25 ns target
Noise and threshold mismatch	90 electrons
Power consumption	12 μW/pixel
On pixel equalization DACs	4 bit

Table 1.4: Timepix3 parameters summary.

up to 1.56 ns. This architecture is able to optimize the bandwidth since the expected maximum hit rate is of 40 Mhits/s·cm^{-2}. Furthermore, the front-end electronics is based on a single threshold discriminator and charge preamplifier with a Krummenacher feedback. Other features which enable Timepix3 to be optimized for power pulsing tests (dynamic wake-up/shut-down) needed for large systems and essential for LINAC requirements.

1.1.1.4 VELOpix

VELOPix[24] ASIC is the chosen chip for VErtex LOcator (VELO)[25] at LHCb. Based on the Timepix3 [22] architecture, the 256×256 pixel array is organized in 128 double columns; each column contains 64 super pixel (2×16 pixels each) and each super pixel connects to 8 digital front-end connected to the analog front-end by mean of the output of the discriminator. Each double column has a data buffer and a finite state machine with communication purposes placed which consist into EoCs. Each super pixel is equipped with the same digital and full-custom analog circuitry integrated in a digital-on-top fashion.

Parameter	Value
CMOS technology process	130 nm
Layout size	14×55 μm^2
C det	50 fF
Minimum threshold	500 e^-, 5-bit threshold DAC
Dead time	400 ns for 16 ke^- input charge
Maximum leakage current	12 nA
Noise (simulation)	60 e^-

Table 1.5: VELOPix parameters summary.

The motivation of the choice of a 2×4 size superpixel is related to the opportunity of packing an sharing data in order to reduce the data rate of 30%. A preamplifier with a Krummenacher feedback and a discriminator give rise to the analog front end, specifically developed for electrons collection; a global threshold is utilized for all pixels. On the other hand, the digital parts show some synchronization circuitry and a linear feedback shift register (LFSR) with a 62 counts range: this pseudo random counter could be programmed for event counting purposes, in a ToT configuration or as a smaller binary counter (with pseudo-randomized values, easily readable with a lookup table); 8 digital front ends arrange a super pixel logic. A ToT threshold logic is dedicated to accept or reject hit values based on a comparison between ToT and a digital programmable threshold. ToT technique is utilized internally into the pixel and the same programmable digital value is shared in the same superpixel. Thus, differetly to Timepix3, VELOPix does not provide charge information. Time resolution is 16 times less accurate with respect to Timepix3 (25 ns) and the on pixel memory for time measurement is smaller (9 bits instead 14). The periphery is node-based [26] and a second memory is dedicated in order to increase the throughput packet from one packet every three clock cycle to just only one clock cycle. Four 160 MHz clocked parallel data channels characterize each half periphery: this leads to a 1.28 Gpackets/s ($2\times4\times160$ MHz).

At the end of the data path, four serializer and drivers with a data rate of 5.12 Gbps are implemented. From a 320 MHz clock, with a DLL (Delay-Locked Loop), sixteen different clock are derived and generated on-chip. This generates 128-bit frame each 40 MHz/output link with a data stream of 5.12 Gbps (320 MHz $\times16$); each frame is composed by 30 bit: 4 bits for the header and a parity bit every packet.

Radiation tolerance is implemented both for total ionizing dose effects and against

single event effects. NMOS transistors inside the preamplifier are equipped with enclosed layout. All state or configuration registers, clock muxes, clock gates, FSMs show a triple modular redundancy protection. Event data coming from pixel does not have protection due to missing area for additional flip-flops. Clearly, radiation protection increases considerably the total chip area.

Chapter 2

Monolithic pixel detectors

2.1 Introduction to monolithic pixel detectors

2.1.1 Generalia

Monolithic Active Pixel Detectors (MAPS) [27][28] were conceived in early 90s as a leading technology for camera sensors development. At that time requirements on noise, speed and leakage were somehow less stringent and the main aim was the detection of visible light (i.e. for consumer devices such as commercial cameras). Due to the initial limitations and poor performance of their original architecture, several improvement and different implementations were considered during the next years in order to richly enhance their performance.
However, until the beginning, some key strengths of MAPS were clear [29][30]:

- they are developed in a standard commercial CMOS technology: this leads simplification of the process for wide cheap production of sensors;
- no bonding necessary (or other types of connections): sensor and front end electronics are in the same piece of silicon and thus produced in the same process;
- possibility to develop smaller pixels with several functionalities integrated in the front end electronics together with the sensor;
- they have low power dissipation;

- radiation robustness can be obtained with deep submicron processes;
- random accessibility to the pixel array;
- massively parallel and high speed analog to digital readout;
- limited readout I/O requirements.

Nowadays they are extensively utilized into everyday technological devices (cams, mobile phones, computers, web-cams, toys, security tools) and they are considered as working technology for particle detectors in HEP.

2.1.1.1 Early architectures: 3T and 4T

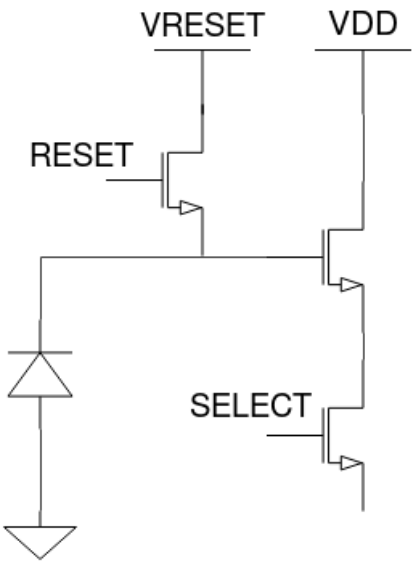


Figure 2.1: The 3T MAPS architecture.

The simplest structure of a MAPS consist in just three transtors (Figure 2.1): one is implemented as reset for the FD node on the photodiode; a second is utilized as switch for readout line selection and the third is the input for a source follower outside the pixel, used as current source and common to all the column. For efficiency reasons the preferred type of transistor are nMOS with p-substrate.
The diode allows a quite good radiation hardness [31][32] and a rather fast time for collecting charge.

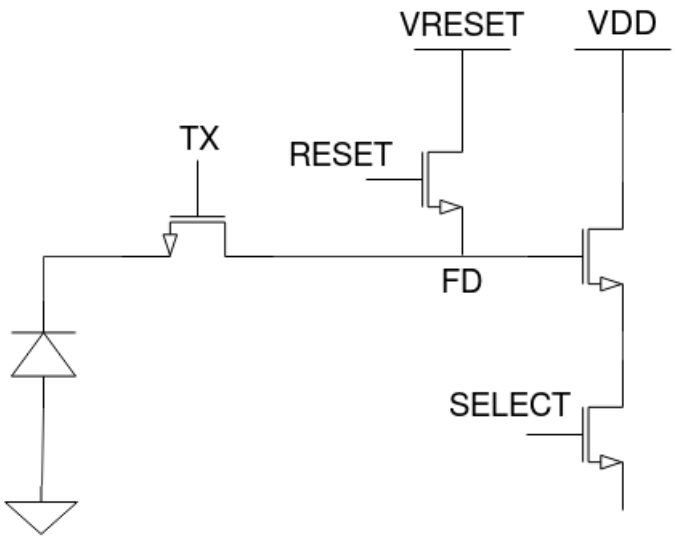


Figure 2.2: The 4T MAPS architecture.

The working mode for this kind of sensors is the so-called *rolling-shutter* mode: pixel array is readout in parallel one line at once by activating the SELECT transistor an then resetting the floating node FD node to a VRESET voltage. In the majority of structures, the charge collection is performed by diffusion and this makes these structures limited in speed. Furthermore, radiation hardness is fairly reduced by the minority carriers lifetime. Nevertheless, deep n-well structures [33][34][35] may guarantee better speed performance. The 3T architecture was used for some projects of particle detecting sensors [32][36][37][38] and it was well known and tested. The 4T MAPS pixel structure with pinned diode and stitching is shown in Fig. 2.2. The two major differences with respect to the 3T structure are:

- a forth transistor in series between FD and the pinned photodiode; with the appropriate timing this transistor is able to transfer the charge from the photodiode to the FD, in this way establishing a in-pixel Correlated Double Sampling (CDS)[39], thus easing reset noise removal (which usually represents the main cause of noise).

- the pinned photodiode represents the key element of the imaging instruments: its structure is fairly close to the base bipolar transistor, with an additional p+ implants on the top of the structure n-well/p-sub; some recent studies [40][41] analyzes its performance during irradiation.

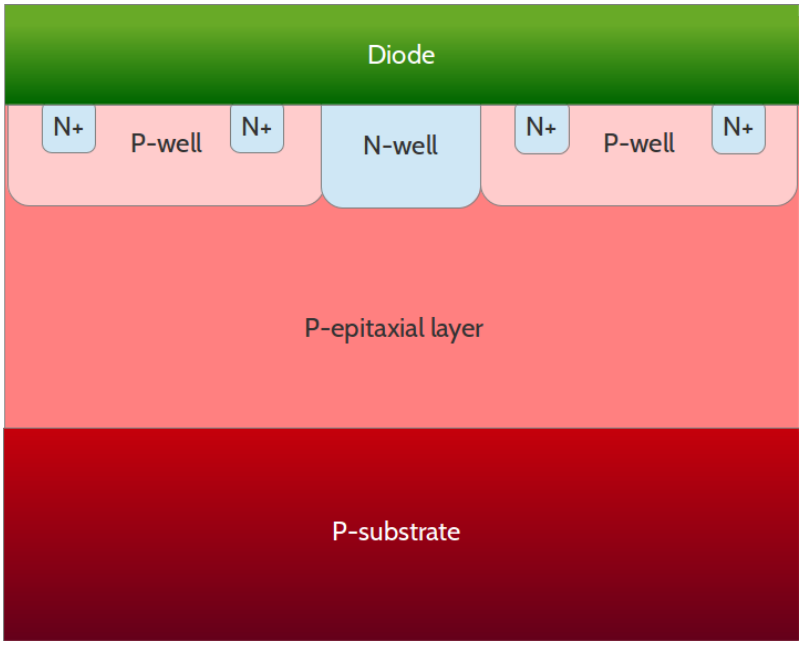


Figure 2.3: A general scheme for a Monolithic Active Pixel Sensor.

In recent years, the development of new silicon detectors in HEP became crucial due to the stringent requirements such as speed, radiation tolerance, time and space resolution, high rate capability and cost lead scientists to put more effort on study and investigation of new adequate solutions. As mentioned before, with the aim to overcome the original structure issues, several improvements [42] of the 3T/4T architecture made MAPS attractive and suitable for High Energy Physics experiments. With respect to HPDs, MAPS fulfill excellently all the requirements pertinent to the quality of the data collection and also an extremely low material budget (since sensor and front end electronics are integrated on the same piece of silicon and no bonding or soldering is needed), easy assembly and low production cost (since they can be produced in a commercial CMOS process). In addition to that, since the connection between the detector and the collection node usually introduces some parasitic capacitance, MAPS exhibit low detector capacitances (on the order of fFs), which means the possibility to working in a low power mode.

2.1.2 Some examples

2.1.2.1 LePix

LePix [43] has been developed in a CMOS process 90 nm with a mid-resistive substrate. Besides traditional charge collection by diffusion, depletion by drift is here possible and it is eased by high values of resistivity: the process on which LePix is based provides an above 500 Ω·cm resistivity substrate, which makes possible to deplete the substrate by using low voltages (≈100 V).
The importance of this opportunity lies in some reasons: the possibility to use very low voltages for drift depletion, thanks to doping level much higher than the traditional MAPS, allows lower power dissipation of the detector system. In addition to that, advanced processes (such as 90 nm or smaller) facilitate reduction of dead area and ease high speed transmission, which represent two main constraints of new generation of particle detectors.
In LePix architecture the collection electrode is built by means of a 2D array of n-well diffusion inserted in a p-substrate. The n-well diffusion also contains the readout circuit, where the nMOS transistors are arranged into a p-well inside the initial n-well, thus originating a triple well configuration.
The detector matrix is composed by 32×32 pixel with a 50 μm pitch. Four sectors of 8×32 pixels implement different input devices:

- sector 1: thin oxide pMOS transistors
- sector 2: thin oxide pMOS transistors (bigger than sector 1)
- sector 3: thick oxide pMOS transistors
- sector 4: nMOS transistors

As expected, transistors in sectors 1 and 2 show higher values of gate leakage while neither transistors in sector 3 nor the nMOS transistors experience this issue. On the other hand, nMOS input transistor exhibits a large parasitic capacitance.
In addition to that, two matrices have been designed in order to implement different sizes of collection nodes (but identical in the other parts): very small, in order to minimize the intrinsic capacitance and fairly larger; tests show that in the first case a smaller size of the electrode leads to an increase of the electric field.
Another difference is the way to reset the pixels: the first 16 rows are reset by

Parameter	Value
Process	90 nm
Pixel array	32×32 pixels
Dimensions	50×50 μm^2
Integration time	programmable
Readout	double-sampling serial

Table 2.1: LePix parameters summary.

applying a reset signal to the reset transistor in each pixel, leading this way an active reset mode. The lower 16 rows, instead, are reset with a diode which absorbs the pixel leakage, generating a sort of continuous reset mode. An embedded capacitor allows test pulse to rows 1 and 17. Power supply is set at 1.2 V for both analog and digital parts, even if their power are separated; CMOS 1.2 V logic is implemented for all the signals. To allow reverse bias of the substrate, a guard ring is inserted. The analog readout is double-sampling serial: at the begin and at the end of the programmable integration time, each pixel's analog voltage level is sampled and the difference between the two is then stored: this value corresponds to the signal plus the integrated leakage current. Even though this readout mode is very similar to the traditional rolling shutter, it differs in the outer and simultaneous storing of the pixel information. For this reason, a peripheral line connects all the pixel and manages the pixels' signal collection. Electrical and irradiation tests have been extensively done [44] [45] [46] [47].

2.1.2.2 ALPIDE

ALICE experiment at CERN is currently through an upgrade which involves the development of a new Inner Tracking System [48] [49] [50] [51]. Based on seven concentric cylindric layers of MAPS, it will cover an area of 10 m^2 and it will be installed during the second long shutdown (2019-2020).
Monolithic Active Pixel Sensor will be produced in a TowerJazz 180 nm process with six metal layers available and the additional small deep p-well structure, which allows the implementation of full CMOS structures inside the pixel circuitry [52]. High resistive epitaxial layers (more than 1 kΩ·cm) represent a crucial node for a better charge collection [53] [54]. During the years several prototypes have been

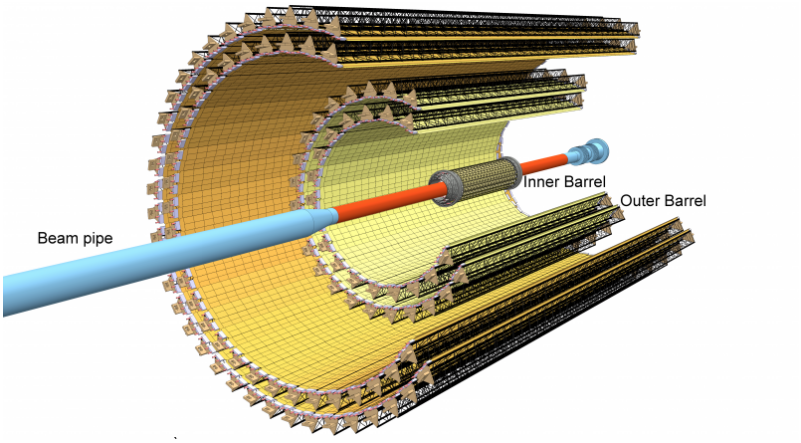


Figure 2.4: Inner Tracking System section; inner and outer barrel are highlighted (image via [1]).

developed to fulfill geometry, power consumption and radiation hardness constraints until the full-scale submission of the final ALPIDE chip in 2014.
ALPIDE chip [55] [55] is arranged by 512×1024 pixel array and its dimension is 1.5×3 cm^2, with a pixel area of 28×28 μm^2.
The readout [56] is binary with an in-pixel hit discrimination and the low-power front-end is continuously active: hit data information can thus be discriminated and sent to a multiple event memory continuously with a trigger latency of some microseconds. However, memory strobing may also be done within long and steady periods in order to perform non-stop data recording. Hit pixel information is thus sent from matrix to the periphery by mean of an in-matrix sparsification circuit with an asynchronous and hit-driven combinatorial circuitry constituted by a priority encoder every double column. From periphery, data are serialized and then delivered off the detector by mean of a high-speed link. Irradiation tests show a detection efficiency of the sensor above 99%, a space resolution of $\approx 5\mu$m and a fake hit rate lower han 10^{-5}. Other details on test may be found in [3].

Parameter	**Value**
Process	180 nm
Sensor thinckness	[inner barrel] 50 μm
	[outer barrel] 100 μm
Dimensions	1.5$\times$3 cm^2
Pixel array	512$\times$1024 pixels
Pixel area	28$\times$28 μm^2
Spatial resolution	[inner barrel] 5 μm^2
	[outer barrel] 10 μm^2
Event-time resolution	$\approx$2 μs
Power density	[inner barrel] 300 mW/cm^2
	[outer barrel] 100 mW/cm^2
Detection efficiency	$>$99%
TID radiation hardness	[inner barrel] 2700 krad
	[outer barrel] 100 krad
NIEL radiation hardness	[inner barrel] 1.7$\cdot$10^{-13} MeV$\cdot$n$_{eq}$cm^2
	[outer barrel] 10^{-12} MeV$\cdot$n$_{eq}$cm^2
Fake hit rate per pixel and readout	$\ll$10^{-6}

Table 2.2: ALPIDE parameters summary.

Chapter 3

The CHIPIX65 project

3.1 Background and motivation

A new frontier of particle physics is represented by the High-Luminosity Large Hadron Collider (LHC) at CERN which should be operational by 2025.

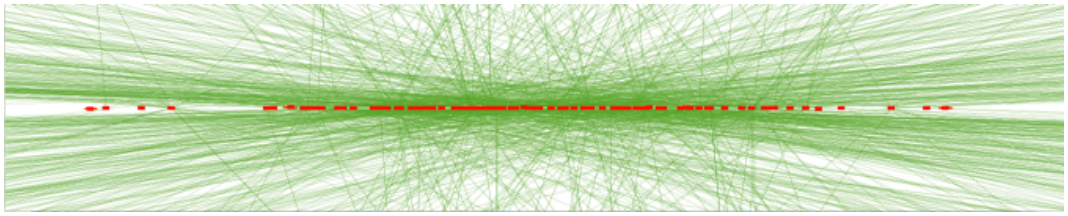


Figure 3.1: HL-LHC pileup graphic simulation.

The aim of this huge project is to increase the LHC performances in order to extend the possibility of discoveries in high energies physics field. The main target is to obtain a $\times 10$ higher luminosity with respect to the current one. Luminosity can characterize the collider because it is proportional to the number of particle collisions happened in a given time. The more elevated is the luminosity, the more particle collision data are collected, the more the accelerator is performing. A higher luminosity collider will allow more accurate studies of new particles and rare processes: HL-LHC will be able to generate 15 million of Higgs processed in a year with respect to the 1.2 million (2011-2012)[57].
For this reason, unprecedented levels of radiation and track density force many technological innovations: in this context, design and the installation of a new kind

of silicon pixel detectors inside the innermost part of the current collider becomes crucial.

The Hilumi LHC [58] of 2011 represented the first part of this project which was

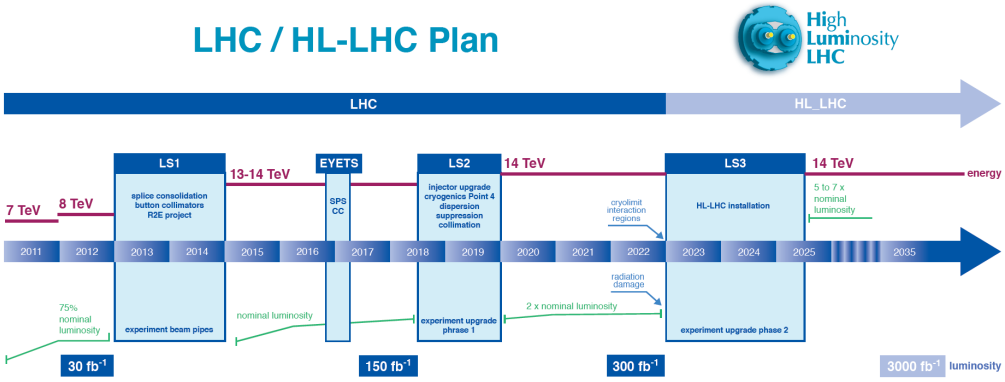


Figure 3.2: Roadmap of HL-LHC Project.

able to pick together some CERN's Member States research centers and it received a public funding from the FP7 European program [58] [59].

A budget of about 950 million CHF is devoted by CERN over a period of ten years to develop HL-LHC.

Parameter	**1st generation LHC Phase 0**	**2nd generation LHC Phase 1**	**3rd generation LHC Phase 2**
CMOS technology	250 nm	250 nm / 130 nm	65 nm
Pixel Dimensions	100×150 μm^2	100×150 μm^2	25×100 μm^2
	50×400 μm^2	50×250 μm^2	50×50 μm^2
ASIC area	≈1 cm^2	≈ 4 cm^2	≈1-4 cm^2
Hit Memory/Chip	0.1 Mb	1 Mb	≈ 16 Mb
Chip Output BW	≈40 Mb/s	≈320 Mb/s	≈3 Gb/s
Max Particle Flux	≈50 MHz/cm^2	≈200 MHz/cm^2	≈500 MHz/cm^2
Max Flux	200 MHz/cm^2	≈600 MHz/cm^2	2 GHz/cm^2
Radiation Hardness	1.5 MGy	3.5 MGy	10 MGy
Signal Threshold	2500-3000 e$^-$	1500-2000 e$^-$	≈1000 e$^-$
L1 Trigger Latency	2-3 μs	4-6 μs	10-20 μs
L1 Trigger Rates	100 kHz	≈100 kHz	200-1000 kHz
Power Budget	≈0.3 W/cm^2	≈0.3 W/cm^2	<0.6 W/cm^2

Table 3.1: Main requirements for the detectors among LHC Phases.

3.1.1 RD53 collaboration

In November 2012 during a workshop [60][61] organized at CERN between some experts of CMS and ATLAS experiments and some VLSI designers the RD53 Collaboration was formed [62]. The aim of this collaboration was based on a program of developing a novel pixel readout for extreme radiation environment based on CMOS 65 nm hybrid technology. The proposal [63] was presented on June 2013 and approved in August of the same year. At the moment, RD53 Collaboration gets involved twenty institutes from Italy, France, Netherlands, Spain, Switzerland, UK, Czech Republic, USA and more than one hundred physicists and electronic designers. The collaboration is organized into six working groups: analog design, I/O developing, top-level design, simulation and testing, radiation qualification, IP-block design [64][65][66].

3.1.2 CHIPIX65 project

The purpose of the CHIPIX65 project [67] is to investigate the potentiality of the 65 nm CMOS technology for its use in high-energy physics experiments. In detail, the main interest is the development of an innovative **CHIP** for a **PIX**el detector in a **65** nm process at extreme rates of radiation for future particle colliders, building analog and digital core elements and analyzing integration and behavioral circuitry issues. Since a CMOS 65 nm technology is used for the first time in HEP community, the radiation hardness technology response needs to be characterized and gathered, especially for what concerns the performances of front end electronics and the behavioral of digital parts with single event upset.
Currently, for several pixel project inside the High Energy Physics field, CMOS 130 nm process is the favorite for various experiments, e.g. VELOpix-LHCb [24], IBL-ATLAS [68]), TimePix [22], ToPix [20], FE-I4 [69]. For the High Luminosity LHC CMS upgrade [70], 130 nm process has been considered but it has been estimated that it cannot fulfill all the stringent area and density requirements [71]. Furthermore, 65 nm technology node represents a stable process already intensively utilized in other industrial applications and thus available for a long time. For these reasons, it has been considered a good choice ready for HEP pixel detector purposes. Beyond this, 65 nm process appears faster ($\times 2$ speed), exhibits a lower power consumption

($\times 4$) and superior compactness of memories and digital parts ($\times 4$). Thanks to the microelectronic department at CERN (PH-ESE-ME), the chosen 65 nm technology has also been tested up to 3MGy of TID with very pledging results.
CHIPIX65 project comprehends seven Italian INFN institutes which are already integral part of RD53 collaboration. Their contribute can be summarized such like this:

- front-end chain (preamplifier, discriminator, signal processing) with different architectures synchronous/asynchronous;
- digital on top architecture for all the developed analog front-end;
- definition of the digital architecture with high-level modeling tools such as SystemVerilog;
- SLVS-to-CMOS and CMOS-to-SLVS transceivers;
- rad-hard by design memories like Dice SRAM[8] and logic;
- Band-gap;
- DAC and ADC;
- providing monitoring data from the chip;
- High Speed Serializer/Deserializer;
- input protocol studies for clock and trigger signals, data protection with error-correcting codes;
- PLL, which is one of the relevant topic of this thesis (see Chapter 3);
- study on Total Ionizing Dose (TID), Total Displacement Damage (TDD), Single Event Upset (SEU), radiation qualification of the technology;

3.2 The CHIPIX65 demonstrator

In the following section the second prototype of a new-generation readout pixel chip [61] [67] is described. As said before, this demonstrator has been designed in a commercial CMOS 65 nm process, identified as a promising technology fulfilling all the High Luminosity LHC Phase 2 Upgrade specifications. The prototype has been designed in order to comply with extremely harsh radiation doses and provide high data rates [72]. Its layout is depicted in Fig. 3.3.
The matrix array is composed by 64×64 pixels with 50×50 μm^2 cells organized in 4×4 groups, integrating two different analog front-end architectures [73][74][75], each occupying half of the pixel matrix and working in parallel. The first synchronous one has been developed by INFN Torino Group; the second one, asynchronous with discriminators, has been designed by Bergamo and Pavia INFN group. Each one occupies an area of 35×35 μm^2.

Parameter	**Value**
Demonstrator Dimensions	3.5×5.1 mm^2
Pixel Array	64×64 pixels
Pixel Size	50×50 μm^2
Analog Front-End	first half: synchronous (35×35 μm^2) second half: asynchronous (35×35 μm^2)
Total Area	17.85 mm^2
Biasing	10-bit DAC
Monitoring	12-bit ADC
Integration Mode	digital-on-top
Trigger Rates	up to 1 MHz
Trigger Latency	12.5 μms
Total Power Consumption	5 μW/pixel
Analog Dead-Time	below 1%
Digital Hit Efficiency	99% at up to 35 GHz/cm^2 pixel rates
Serial Data Transmission Freq.	320 MHz (CMOS-to-SLVS)

Table 3.2: Summary of the characteristics of the prototype.

Charge measurement linearity up to 30 ke^- input charge are performed by using a ToT (Time-over-Threshold encoding technique) for digitization up to 5-bit [76] of

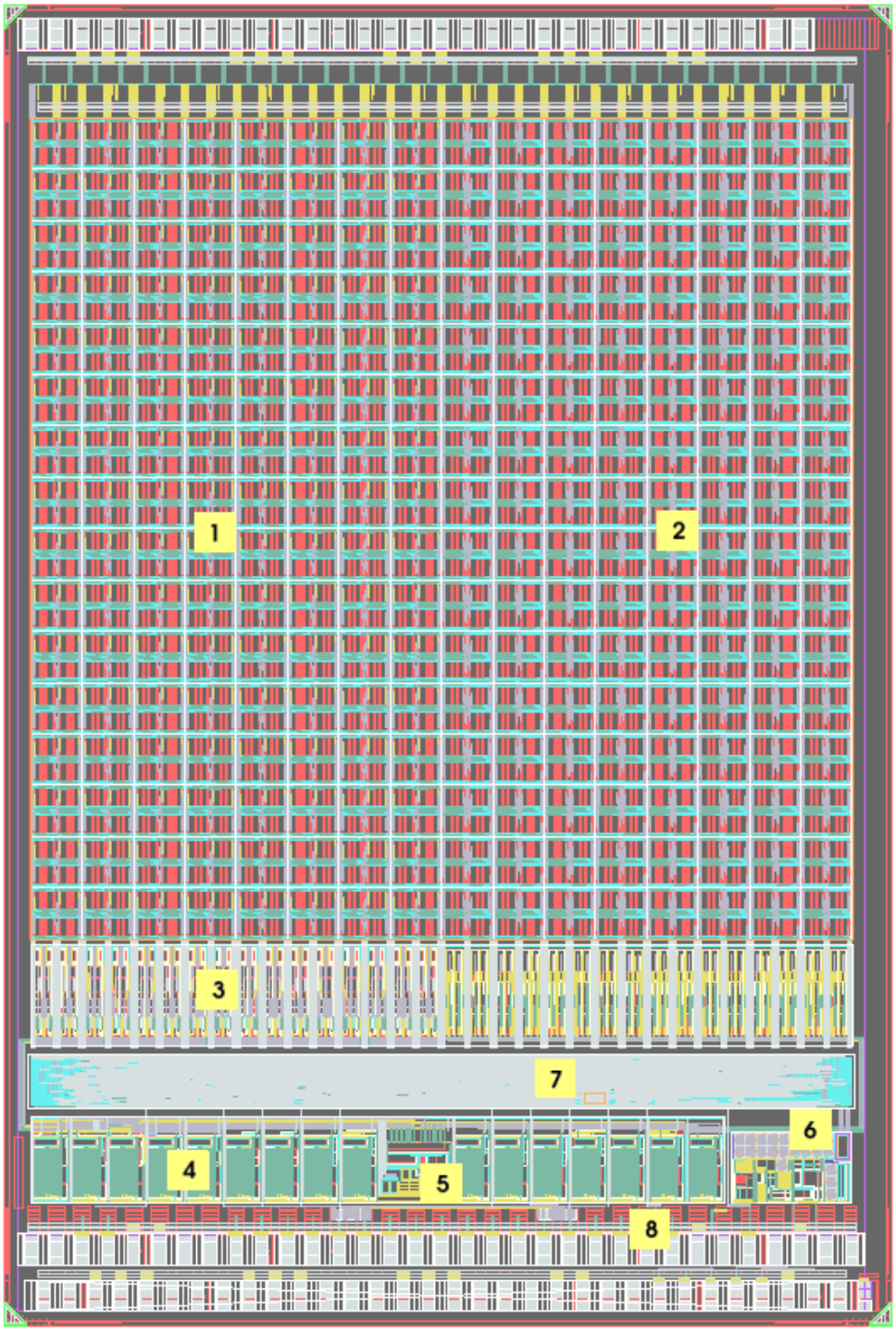


Figure 3.3: CHIPIX65 demonstrator layout. It consists of a 64×64 matrix with dimensions equal to 3.5 mm×5.1 mm. In detail: Synchronous Front-End Architecture (pale yellow label 1), Asynchronous Front-End Architecture (pale yellow label 2), Column Bias Cells with current mirrors (pale yellow label 3), Global DACs (pale yellow label 4), Band Gap Reference (BGR) (pale yellow label 5), monitoring ADC (pale yellow label 6), End of Column and high-speed serializer (pale yellow label 7), SLVS TX/RX and I/O cells (pale yellow label 8).

encoding resolution with a the compensation of the leakage current up to 50 nA/pixel by using a continuous charge reset in the preamplifier achieved through a Krummenacher stage. A fast rise time allows to correct time-stamp allocation with a 40 MHz frequency (which is the nominal LHC bunch crossing frequency). With low noise (ENC<100 e^- RMS for 50 fF of input capacitance) and low power (below 5 μW/pixel, which is the bump bonded chip expected value) performancess, both analog front ends (synchronous and asynchronous) are able to work with low thresholds (below 1000 e^-) and to ensure high efficiency at extreme data rates. Thanks to its compactness, all the analog front-end electronics (both sync and async) is fit inside half pixel area. Analog front-end electronics has been separated by the digital parts in order to avoid noise issues: all the circuitry (ADC and the bias cells with current mirros, DACs, band-gap voltage reference) has been developed into a deep n-well 2×2 pixels large and its routing has been protected by mean of shield barriers near the digital parts.

A common novel region-based digital architecture [76] has been designed in order to guarantee >99% efficiency with HL-LHC (12.5μs trigger latency, 1 MHz trigger rate and 3 GHz/cm^2 hit rate). All the pixels share a common digital synthesized logic whose aim is to provide trigger matching, local configuration and a central memory for latency buffering. Simulations have demonstrated that this digital architecture shows an inefficiency below 0.1% during usual HL-LHC particle runs.

The architecture of the readout for triggered data is based on some replicated FIFOs at the periphery with a column drain protocol. An high-speed serializer [73] is used to sent off-chip all the data previously 8b/10b encoded and then split into 20-bit chunks; serialized data are transmitted off-chip at 320 MHz. Besides this, a debug and a triggerless operating mode is supported for testing and verification purposes. Fully duplex SPI (Serial Peripheral Interface) master/slave protocol allows to perform slow control and chip configuration. A custom-designed JEDEC 400 mV-compliant SLVS transmitters and receivers constitutes the I/O digital interface. An on-chip 10-bit programmable DAC [77] is used to generate voltages and global biases for the analog parts; then again a 12-bit ADC [73] allow bias currents and voltages monitoring. The stable reference value for all these parts is generated by a band-gap voltage reference circuit. All global biases and voltages required by analogue front-ends are generated on-chip using 10-bit programmable DACs. Bias currents and voltages can be monitored by a 12-bit ADC. A band-gap voltage reference circuit [78] provides

a stable reference voltage for all these blocks. All the IP-blocks (band-gap voltage reference, monitoring ADCs, serializer,SLVS drivers) and and front-ends used are silicon-proven and tested after exposure to ionizing radiation (up to 500-800 Mrad TID)[73].

3.2.1 Analog Architecture

The CHIPIX65 demonstrator shows two different analog front-end architectures:

- a synchronous one [74], which occupies the first half of matrix (see Fig. 3.4)
- an asynchronous one [75], which occupies the second half of matrix (see Fig. 3.5).

A common configuration scheme and digital architecture are used among all the pixels.
Both solutions are rad-hard designed and they were validated in silicon by using small 8×8 prototypes and test structures during the very first CHIPIX65 chip submission; in this context, the first small prototypes were tested to an irradiation test up to 800 Mrad and then were fully working after that [73] [74] [75] [79].

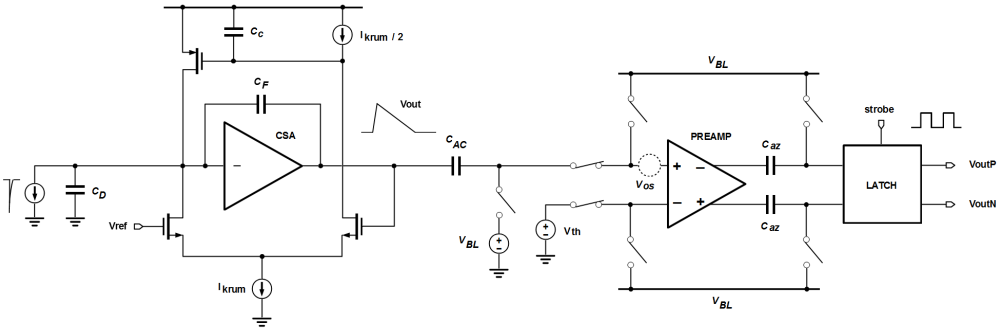


Figure 3.4: Schematic view of the synchronous front-end. From left: Krummenacher feedback charge-sensitive amplifier, AC coupling and track-and-latch voltage comparator with auto-zeroing obtained with the OOS technique.

In Fig. 3.4 the synchronous front-end schematic view is shown. A telescopic-cascode inverting amplifier is implemented with the possibility to choose two feedback capacitors for charge sensitivity selection. For the hit discrimination, track-and-latch

voltage comparator is utilized.
The generation of a CMOS digital pulse is carried out when a signal is above the nominal threshold; this signal is then synchronized with a 40 MHz clock, by strobing the latch. FastTOT charge digitization encoding is provided by an high-frequency clock signal (up to 800 MHz), which is pixel-level designed and internally generated by turning a latch into a Voltage-Controlled Oscillator.
An auto-zeroing circuit based on OOS (Output Offset Storage) between the positive-feedback latch and the differential amplifier furnishes the compensation of the threshold variations pixel-to-pixel. For this reason, no DACs are needed to tune the threshold value in each pixel. On the other hand, in the asynchronous front-end

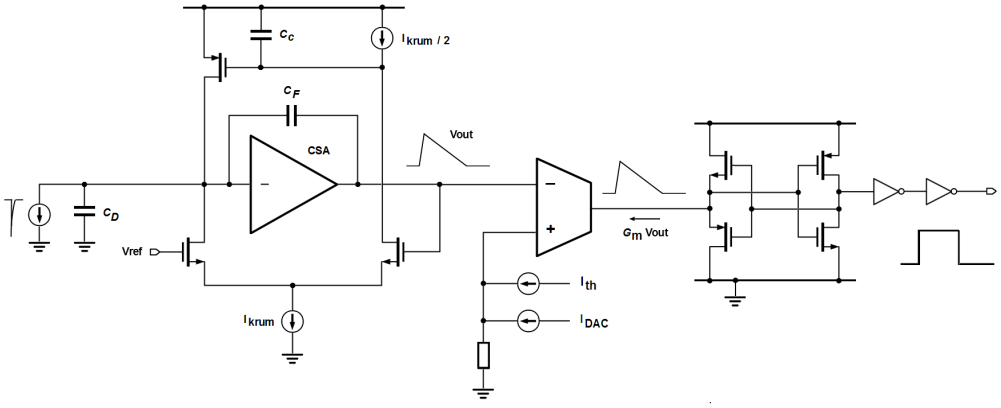


Figure 3.5: Schematic view of synchronous front-end chain. From left: Krummenacher feedback charge-sensitive amplifier, voltage-to-current transconductor and fast current comparator.

version (see Fig. 3.5) some feedback-network optimizations with different CSA have been made, while a common architecture scheme (with the Krummenacher feedback) is shared: as the gain stage a folded-cascode inverting amplifier is implemented, with a selectable charge sensitivity. For the hit discrimination a current-comparator is used with a transconductor stage to convert voltage to current.
Digital pulse CMOS inverters are implemented to get a full-swing rail-to-rail. The threshold value is generated by current flowing into a diode-connected MOS device. A local 4-bit binary-weighted DACs provides the pixel-to-pixel threshold compensation while all the pixels provide the global current reference.

3.2.2 Region digital architecture

All the 64 pixels are divided into 16 small 4×4 matrices which are called Pixel Regions (PR). Each PR includes in itself 16 analog front-ends in four analog islands in the chip layout. In order to gather all the pixels' data, a novel digital architecture shared between analog parts is implemented. Its aim, beyond the configuration managing, is to communicate with the chip periphery (where the readout block is located) and execute the trigger matching.

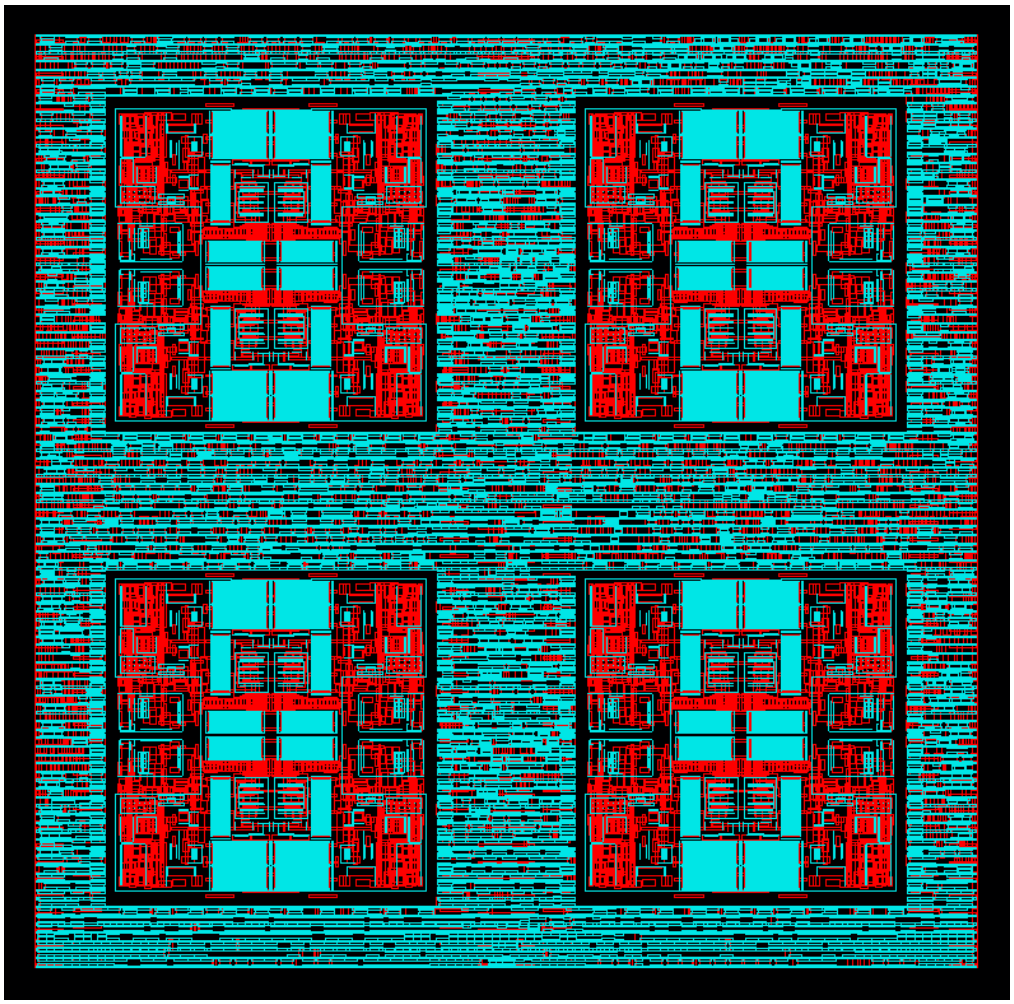


Figure 3.6: Pixel region (4×4 pixel) layout. As it is possible to see, each pixel region contains 2×2 analog islands (sixteen analog front-ends) with a common digital logic architecture.

Based on some theoretical prediction [80], 16 buffer rows are needed in order to

achieve a low event loss ($\approx 0.1\%$) for each Pixel Region. Furthermore, the TOT compression helps to optimize power and area. With the aim to simplify and automate estimations and simulations of the working condition, a dedicated RD53 verification environment has been designed [65][81][82][83].

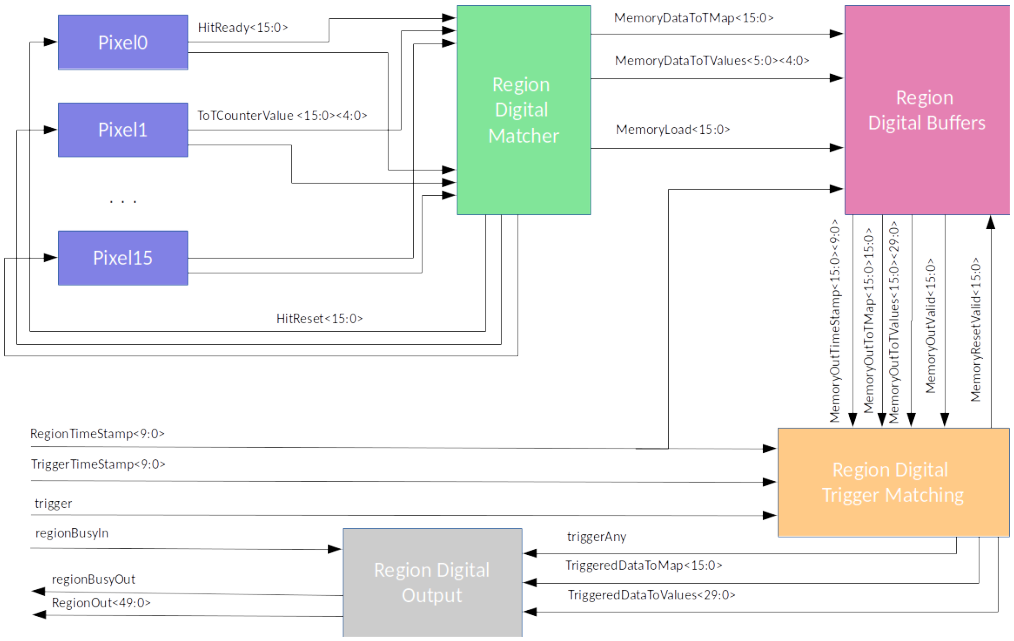


Figure 3.7: Digital architecture functional scheme.

3.2.2.1 Pixel data acquisition and synchronization

When some pixel are hit together, their data processing happens at the same time, independently of their TOT value. For this reason, in order to compress acquired data, all the pixels must be synchronized with the others by using some deadtime counters: their purpose is to force all the pixel to freeze for a common fixed time during which they are unable to catch other hits because they are processing the old ones. This deadtime does not involve a whole PR but one pixel a time. Once this time is completed, the first 6 hit pixel are selected and put into a priority line and the shared buffer is filled with timestamp and hit map collected data. In such a way, each event can be rebuilt with a binary map which allows an off-chip reconstruction. At the end of this procedure, all the pixel are reset and the shared logic enable them to be ready for another acquisition again. This procedure promotes both area saving

and a low information loss ($\approx 0.6\%$ due to the number of saved TOT values). More details on inefficiencies may be found in [80].

3.2.2.2 Operation modes

Readout of the storing buffer can be carried out into different ways: triggered, triggerless mode and debug mode.

- *Triggered mode:* when this mode is selected, the Chip Periphery propagates an activation signal for some dedicated comparators along the Pixel Regions with a trigger timestamp: these comparators stand by waiting for a trigger signal. When it happens, the comparators compare their timestamp with the one previously received. If there is any matching between them, the output line is marked and a busy flag signal is put high and propagated to the End of Column. A OR gates chain allows to carry the busy flag signal from the hit pixel region to another. Furthermore, all the previous pixel regions do not do so. Instead, if the busy flag comes from some previous pixel region, a multiplexer propagates this signal to the following one;
- *Triggerless mode:* in this mode, all the events are carried out as soon as they are collected, recording just the binary data with a negligible deadtime. This mode is useful for laboratory testing (e.g. to acquire data from a bump-bonded sensor during irradiation);
- *Debug mode:* input values are directly put into the digital part keeping out the analog front-end.

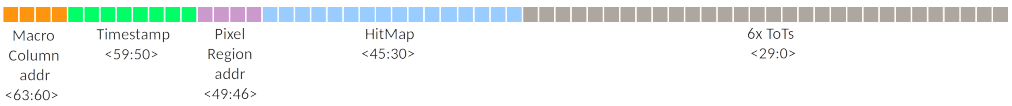


Figure 3.8: Output packet scheme.

3.2.2.3 Readout

Macro Column Drainer (MCD) modules are designed with the aim of communicate between each macro-column, which is a column composed by PRs. Each Macro

Column Drainer is connected to a dispatcher whose purpose is to fill the output serializer with valid data (see Fig. 3.9). Pixel Region readout is immediate: when some valid triggered data appear in any PR, their busy flag is lift after a clock cycle and their signal is transmitted in an asynchronous way to the multi-column drainer. In detail, when the triggered mode is chosen, the MCDs store the trigger signals coming from the Chip Periphery in correspondence with their timestamp. At the same time, a finite state machine (FSM) continuously checks the trigger buffer, makes a selection of the first value and sends it to the PR and lastly checks the PR busy flag. On the other hand, if a triggerless mode is activated, the finite state machine remains listening for all the time.
All the outputs coming from the MCDs buffers are collected and gathered into a buffer inner to the dispatcher; another finite state machine manages this data, dividing them in 16-bit long blocks and sends them to a 8b10b encoder[1], which provides 20-bit words: this data stream represents the final output sent to the serializer. Some special codes are utilized to identify starting/end of a data bunch or an empty data stream.

Parameter	**Value**	**Comments**
Total Area	33083 μm^2	6 6% STD cells TU
		(including CTS and buffers)
Total Power	$\approx$120 μW, 7.5 μW/pixel	(triggered mode, slow clock)
Inefficiencies:		
	event loss	$\approx$0.04% (due to buffer overflow)
	charge information loss	$\approx$0.41% (due to limited ToT values saved)
	ghost hits	$\approx$0.025%
	effects of fixed	deadtime not included

Table 3.3: Digital architecture performances summary.

3.2.2.4 Chip configuration, End of Column readout and I/O

An SPI configuration is used to perform the configuration of the chip. An off-chip master handles the sending of 20-bit serialized data packet and the chip behaves aas an SPI slave. In order to perform the configuration, there are four kinds of registers:

[1] A 8b10b encoding allows code 8bit into 10 bit with the aim to reach a bounded disparity and DC balance of a telecommunication [84].

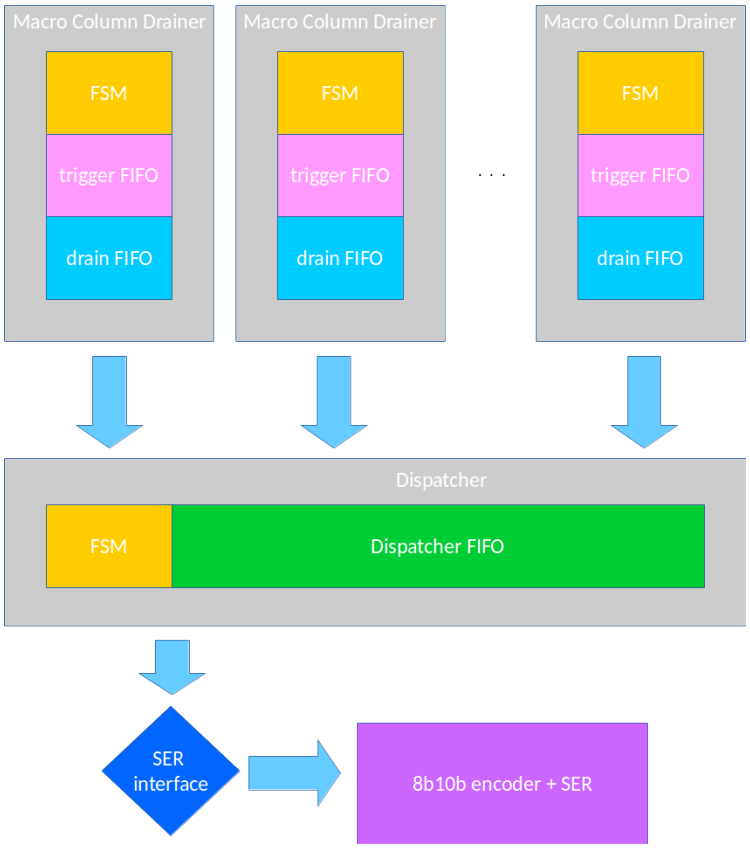


Figure 3.9: Macro Column Drainers readout flow.

- the Pixel Configuration Registers (PCRs)
- the End of Column Configuration Registers (ECCRs)
- the Global Configuration Registers (GCRs)
- some various registers for direct-programming

Each Pixel Region has 8 Pixel Configuration Registers: four for the left half and four for the right. To configure two adjacent pixels, each group of four PCRs contains sixteen bits: to configure a pixel pair, the chip has to send the address to a configuration module located at the chip periphery which translates it into four block code: the Macro Column Address, the Pixel Region address, the Left/Right flag, the Pixel Configuration Register index.

Each SPI packet is composed by 24 bits:

- bits <23:20> corresponds to SPI command (see Table 3.4);

Figure 3.10: SPI packet division.

- bits <19:16> are unused;
- bits <15:0> payload bits; they may assume different purposes:
  - write-pointer:
    · bit 15: selection of auto-increment mode for PCR programming (active high);
    · bits <14:11>: unused;
    · bits <10:7>: selection of the Macro Column;
    · bit 6: selection of one out of the two Double Columns in the Macro Column;
    · bits <5:2>: selection of the Pixel Region in the Macro Column
    · bits <1:0>: selection of one out of the four double PCR registers;
  - write-data: bits <15:0> are used for the identification of the data need to be written in the four double PCR registers.

3.2.2.5 SLVS drivers and padframe

Since the strong radiation environment, which forces the use of transistor with thin gate oxide and 1.2 V supply voltages, SLVS standard has been adopted rather than a LVDS standard (which requires 1.8 V supplies). This standard furnishes up to 12

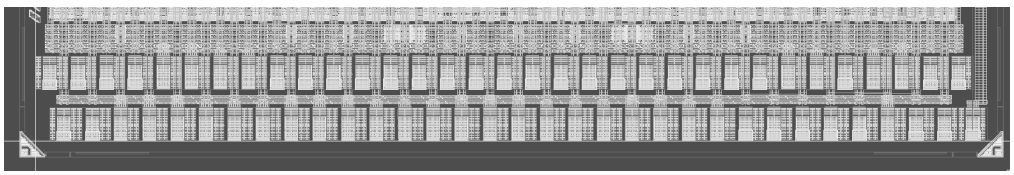


Figure 3.11: Drivers and SLVS pads.

Gbps link bandwidth with 200 mV differential swing and 200 mV common-mode voltage. SLVS drivers and I/O pads layout are depicted in Fig. 3.11.

MSB (bits <23:20>)	SPI command meaning
0000	Write POINTER register
1000	Read POINTER register
0001	Write DATA register
1001	Read DATA register
0010	Write STATUS register
1010	Read STATUS register
0011	Enable 8b/10b sync
1011	Disable 8b/10b sync
0100	Enable pixel-region debug mode
1100	Disable pixel-region debug mode
0101	Write SLVS configuration bits
1101	Read SLVS configuration bits
0110	Start autozeroing (enables PHI_AZ generator)
1110	Stop autozeroing (resets and disables PHI_AZ generator)
0111	ADC start of conversion
1111	Enable pixel-region debug mode

Table 3.4: SPI configuration commands.

3.2.3 Bias network and monitoring

In Fig. 3.12 a schematic view of the monitoring network and the bias is shown. All the bias currents and voltages for the fine-tuning of the analog performances are generated and shared by some programmable DACs [77].
A 12-bit ADC supplies on-chip monitoring capabilities. The synchronous front-end employs nine DACs, while six are utilized by the asynchronous one.
A common (to both front-ends) DAC is used for DC calibration level programming when the selected pixel is injected with a test charge pulse. A 4 μA reference current is provided to all the global DACs by a band-gap voltage reference (BGR) [78].

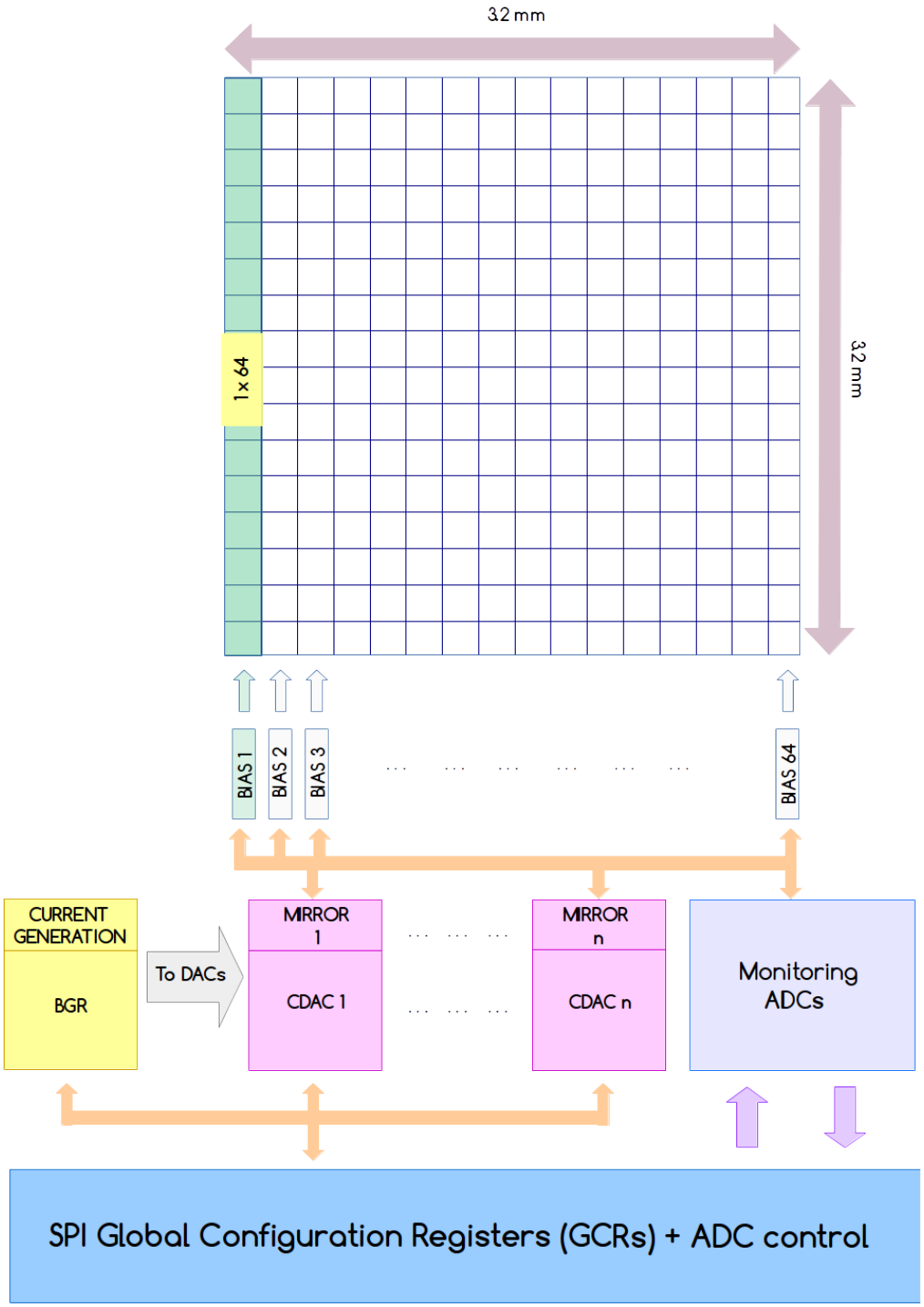


Figure 3.12: Block scheme depicting monitoring network and bias.

3.3 Test results

For testing purposes [2], the prototype ASIC has been wire-bonded to a custom test board developed by the INFN-Torino group. This PCB, equipped with some test points for measuring currents and global bias voltages, has been connected by mean of an FMC connector to a Xilinx KC705 FPGA Evaluation Board. The FPGA were running custom firmware communicating with LabVIEW calibration and control software via a custom UDP-Ethernet protocol.

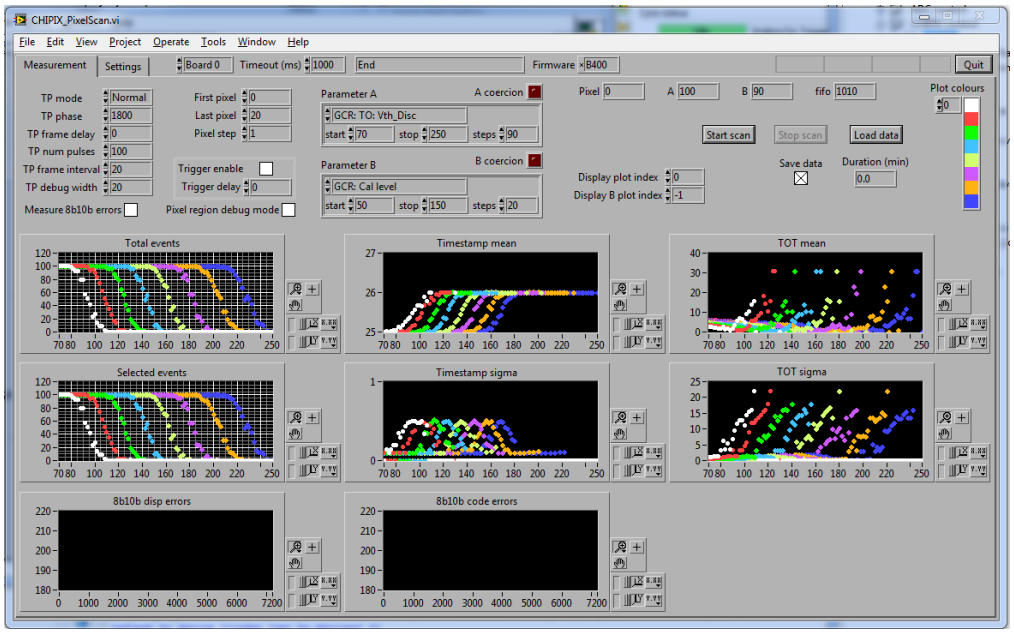


Figure 3.13: LabVIEW interface for data acquisition.

3.3.1 Calibration DAC and monitoring ADC

The output voltage variation with respect to DAC code is depicted in Fig. 3.15, while Fig. 3.16 illustrates the variation of ADC code versus the input voltage. Both plots shows results both for the laboratory measurement and the SPICE simulations, and the both reveal a good agreement between the two.

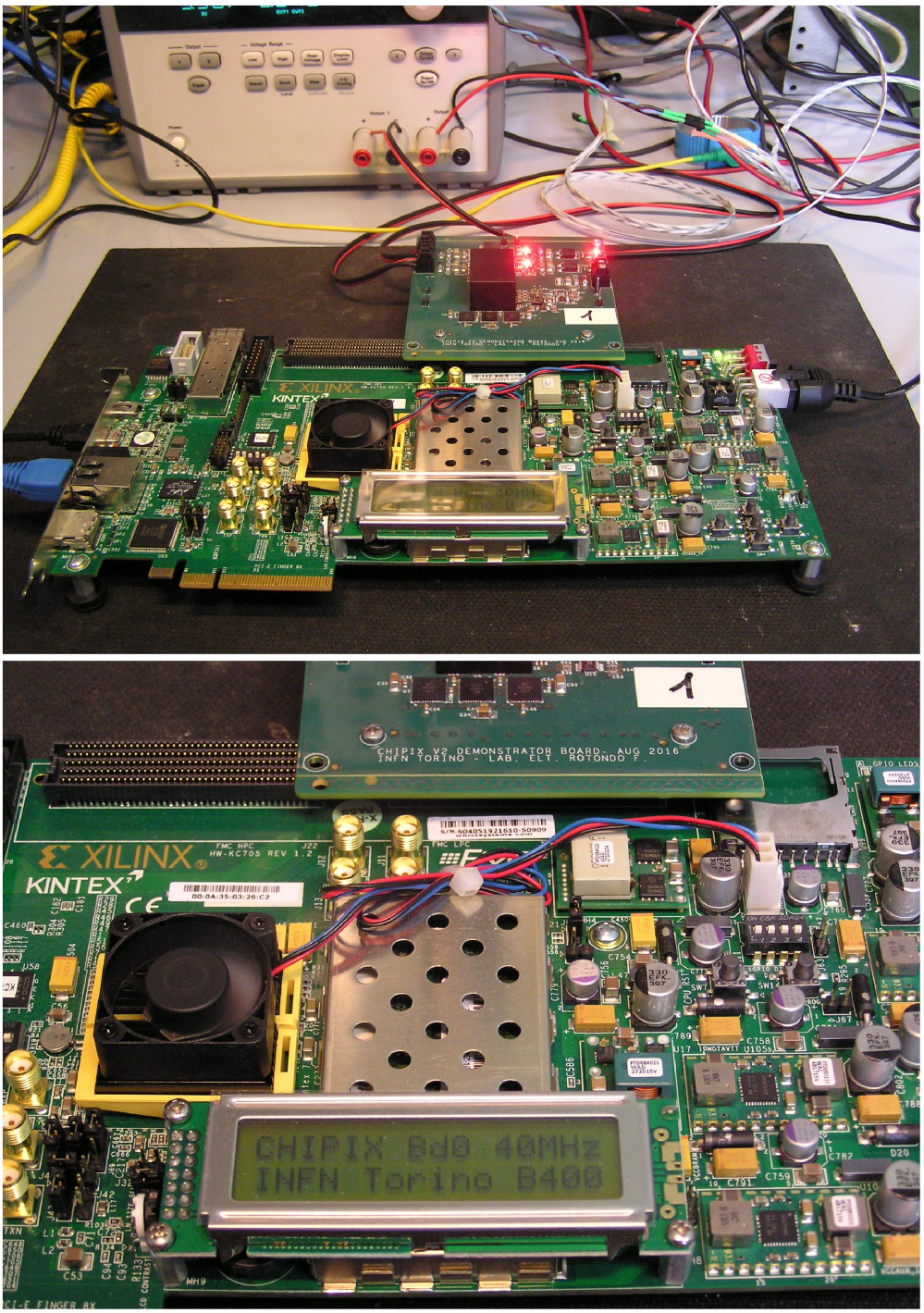


Figure 3.14: Test setup at the INFN Torino laboratory.

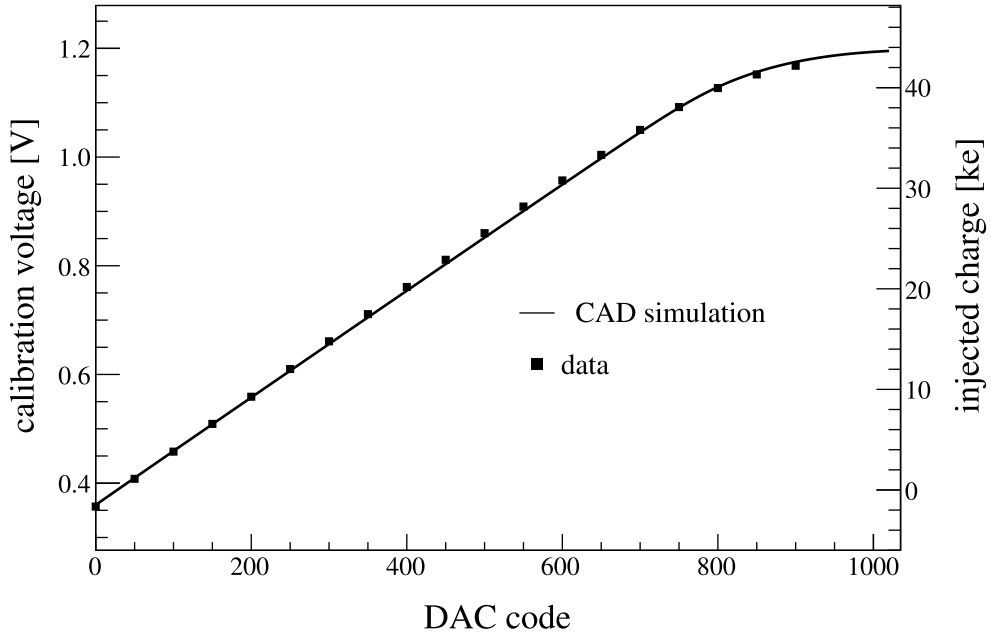


Figure 3.15: Test results and CAD simulation data of calibration DAC (plot via [2]).

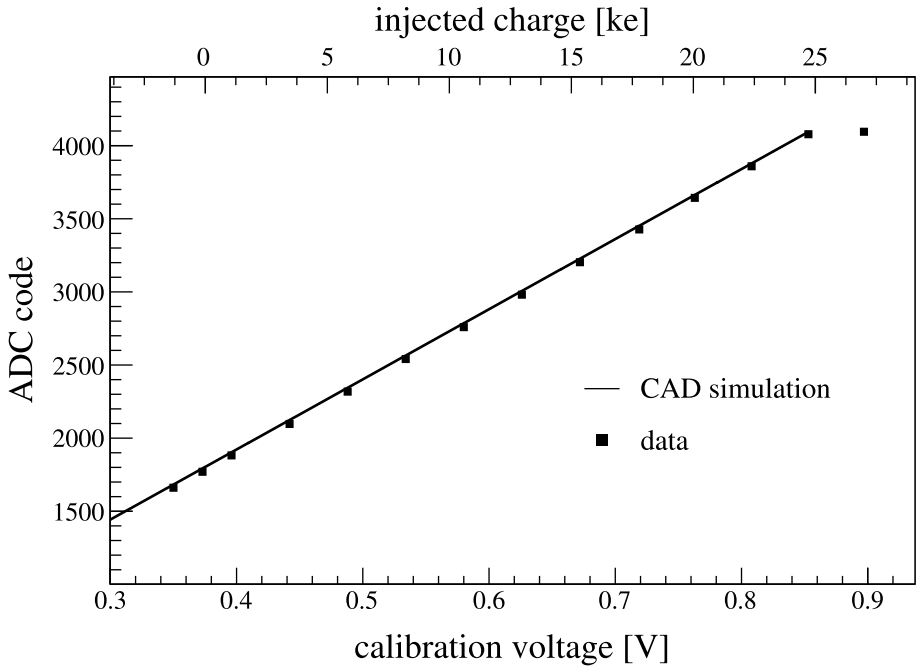


Figure 3.16: Test results and CAD simulation data of monitoring ADC (plot via [2]).

3.3.2 Synchronous front-end

In order to obtain some information regarding minimum thresholds and the noise of the synchronous front-end, two different approaches may be adopted:

1. with the fixed threshold, to vary the calibration charge;
2. to maintain the calibration charge constant and to vary the threshold.

3.3.2.1 Calibration voltage scans

In this instance, all pixels have been tested with a 75 ns long auto-zeroing procedure each 100 μs and with a 100 charge-injection pulses for each point hit efficiency in order to extract threshold and noise values from variances and mean distributions. A sigmoid error function has been utilized to fit the points: this allows to obtain the effective threshold value (which is the underlying gaussian distribution's mean) and the sigma value. Fig. 3.17 explains the results of this analysis.

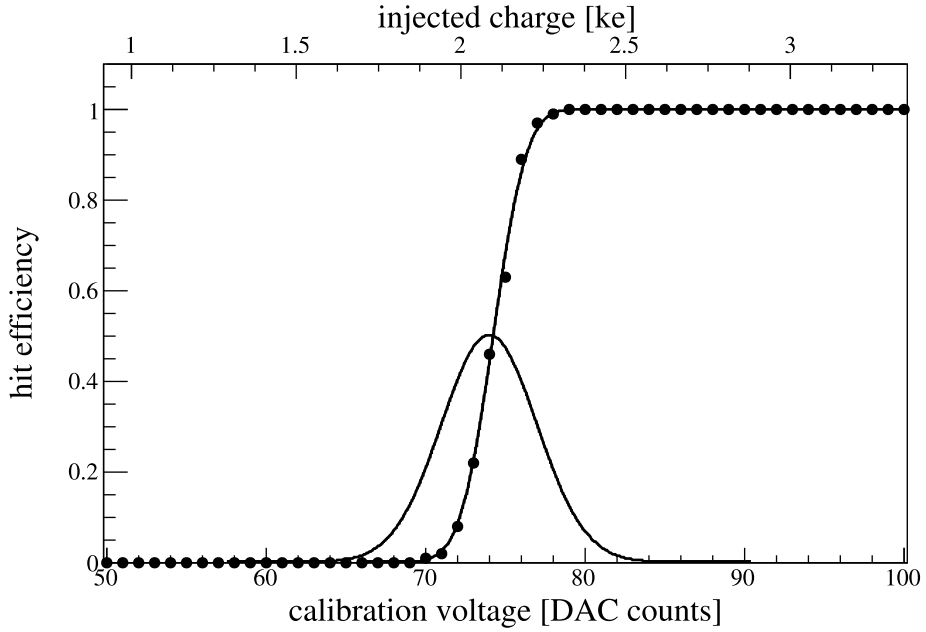


Figure 3.17: Charge scan measurements; fit by using a sigmoid error function (plot via [2]).

The scans of the calibration voltage and their fitting curves are depicted in Fig. 3.18.

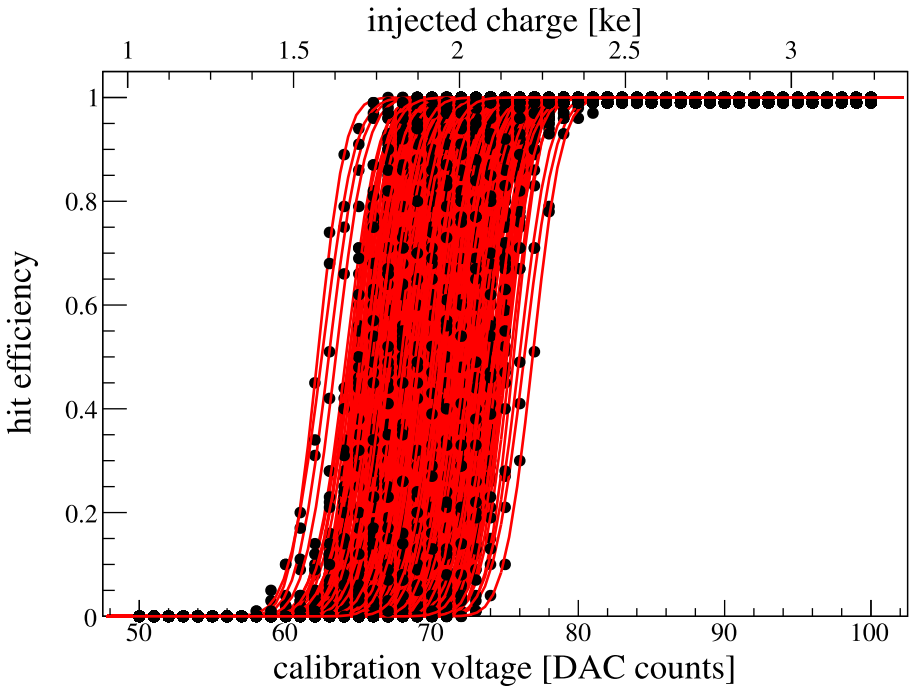


Figure 3.18: Synchronous front-end: calibration voltage scan for all the pixel (plot via [2]).

For a fixed injected charge of ∼2000 e^- and for different values of a fixed global threshold, effective threshold measurement have been done; the results distribution of those scans are Fig. 3.19

The good working operation of the auto-zeroing process is demonstrated by the about 100 e^- RMS value of residual latch dynamic offset, which also appears in good agreement with CAD simulations which shows a value of ∼70 e^- RMS. The distributions' peaks (depicted in Fig. 3.19) are plotted (see Fig. 3.20) vs the global threshold and then linearly fitted. The good quality of the linear fit demonstrates the high precision of the auto-zeroing process. Again, for different values of fixed global threshold some Equivalent Noise Charge (ENC) measurements have been performed. Fig. 3.21 shows, as expected, that the noise behavior remains constant with different threshold values. With respect to the intense logic switching activity of the region, the ENC ∼90 e^- RMS value appears to be low and matches with CAD simulations.

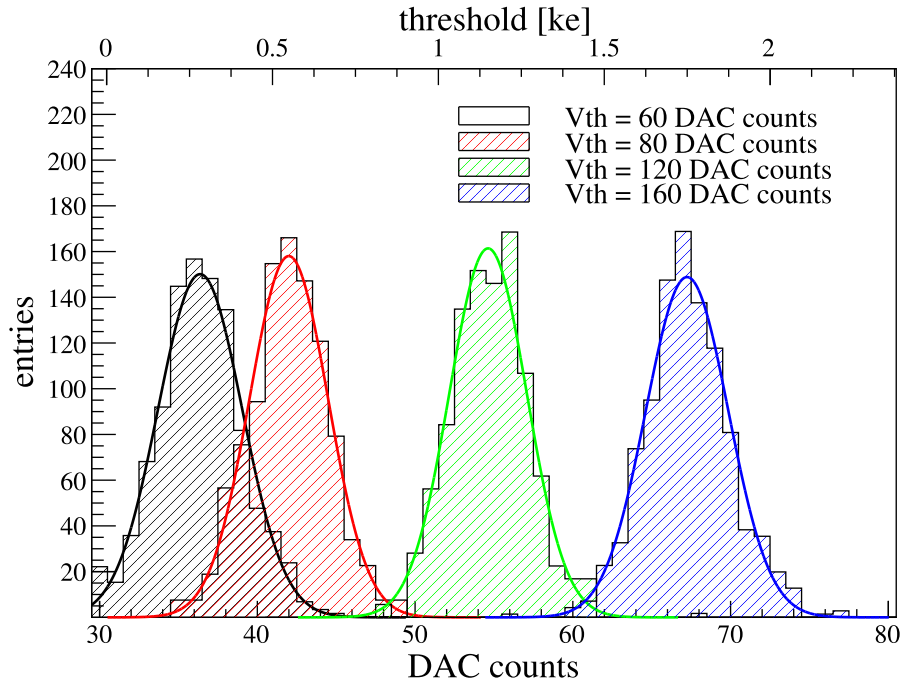


Figure 3.19: Synchronous front-end: effective threshold measurement distribution for different values of fixed global threshold (plot via [2]).

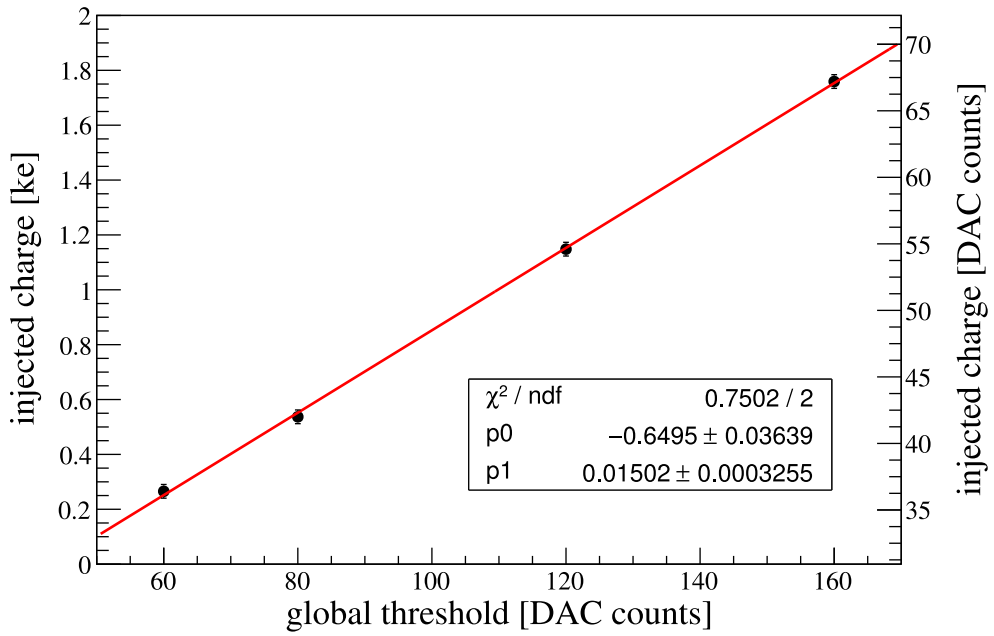


Figure 3.20: Global threshold expressed in DAC counts vs injected charge with linear fit (plot via [2]).

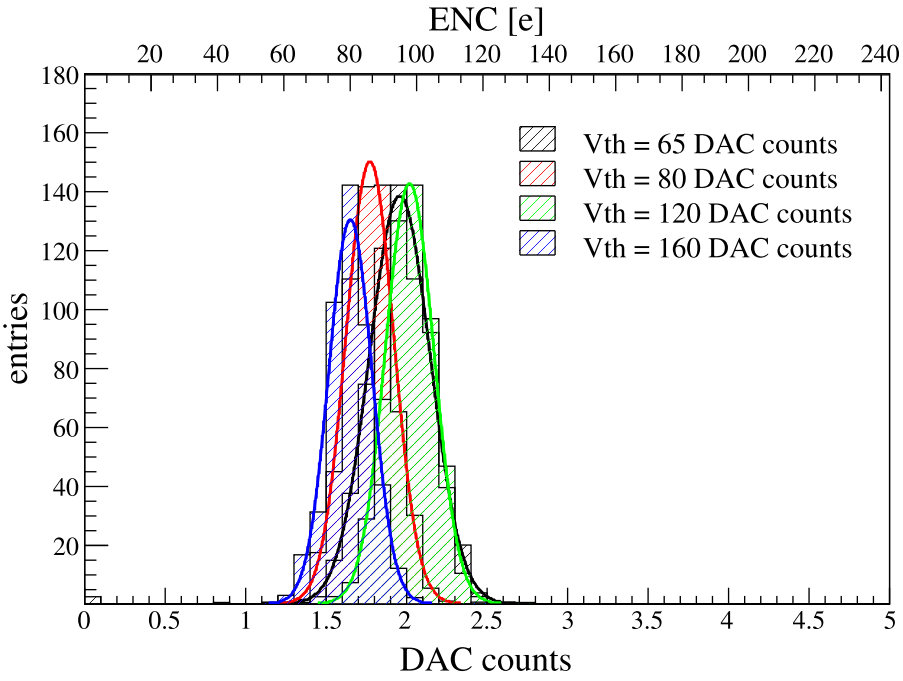


Figure 3.21: Synchronous front-end Equivalent Noise Charge (ENC) measurements for some different fixed global threshold values. All the pixels in the array use a minimum common threshold (equal to $\sim$250 e^-) [2].

3.3.2.2 Threshold voltage scans

Some threshold voltage tests have been performed starting firstly from the nominal baseline and then reducing the value with the aim of detect the minimum charge. In Fig. 3.22 those tests are depicted. As expected, a great number of pixels fires below $\sim$250 e^- due to noise fluctuations.

A Time-Over-Threshold technique is used to realize charge digitization. In Fig. 3.23 the linearity (for a single pixel) between the 5-bit fast ToT vs the calibration voltage is shown. The slope's distribution of the linear fit of the ToT vs. the calibration voltage tested for all pixels is then shown in Fig. 3.24 and appears in good agreement with CAD simulations. For a a 320 MHz frequency, the slope dispersion expected is of $\approx$10% due to analog parts mismatches.

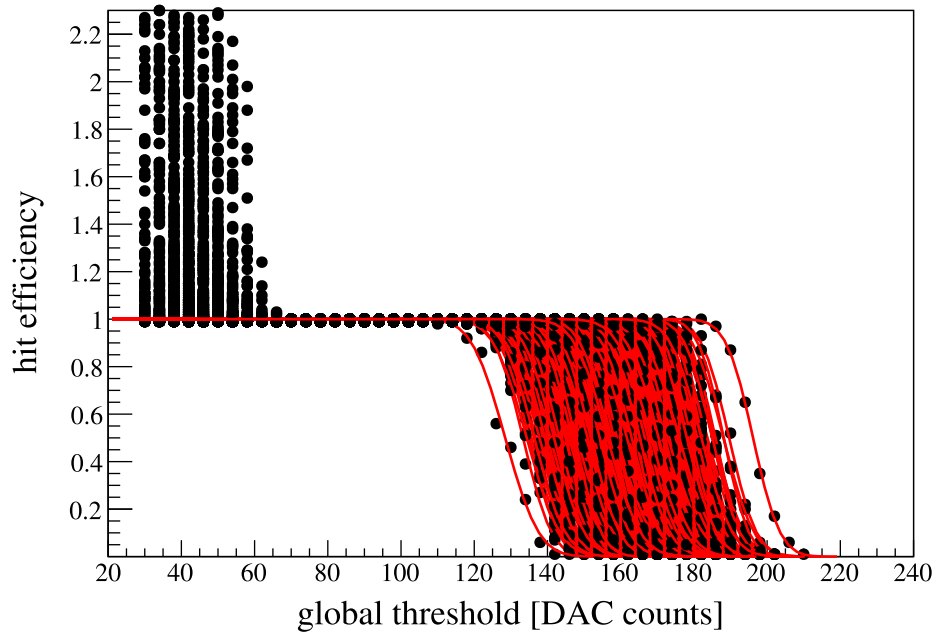


Figure 3.22: Fixed-charge scan curves (plot via [2]).

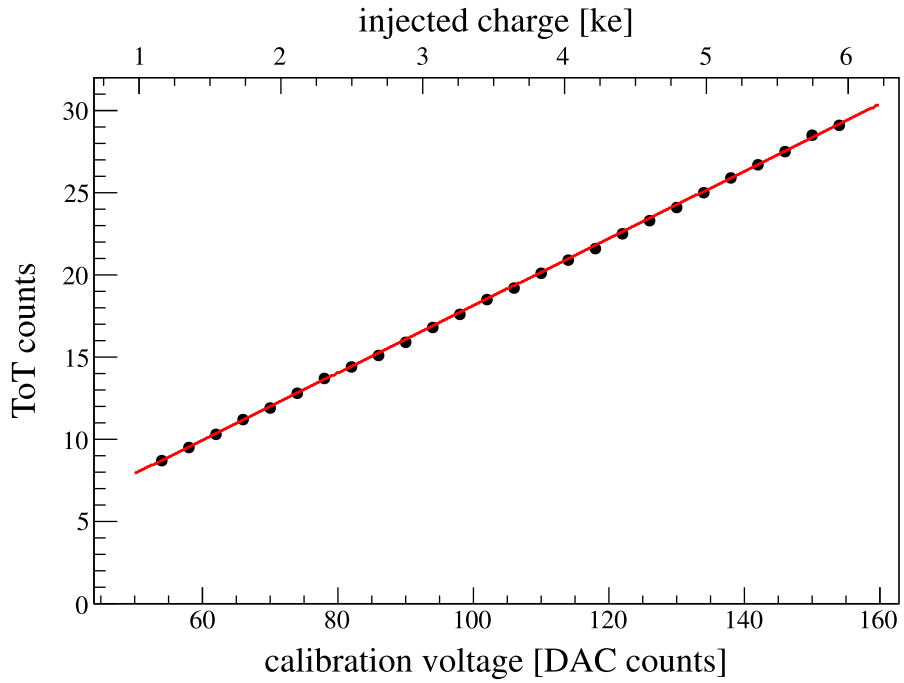


Figure 3.23: ToT linearity for a single pixel (plot via [2]).

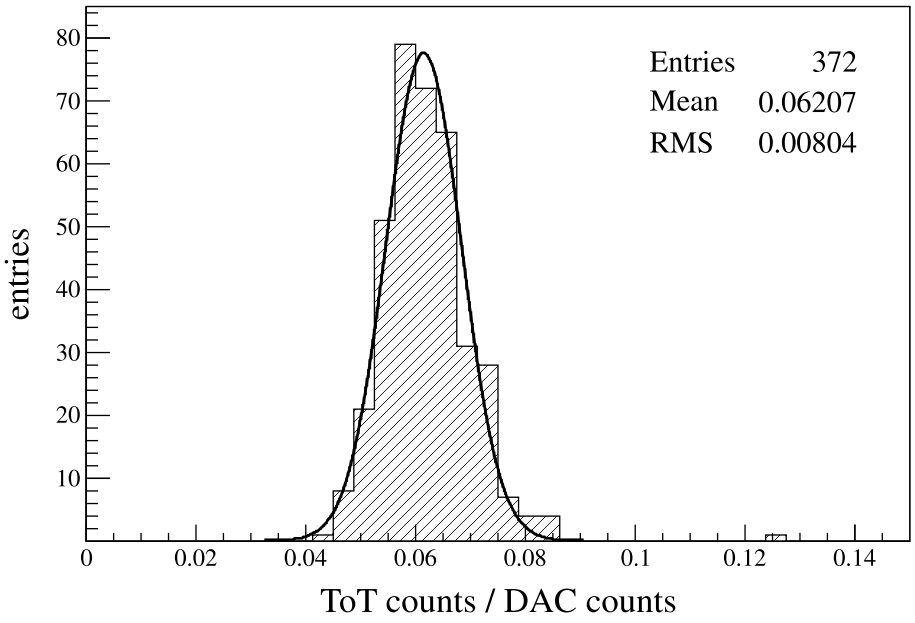


Figure 3.24: ToT slopes distribution (plot via [2]).

3.3.3 Asynchronous front-end

A continuous-time front-end occupies the second half of the matrix, where a threshold discriminator and a low-power trans-impedance amplifier based architecture allow fast switching operation.
A local and in-pixel circuit for threshold correction, based on a 4-bit binary weighted DAC solves the issue of the dispersion of the thresholds.
First tests indicated that all pixels were fully working as it is possible to see from Fig. 3.25 and 3.26: these preliminary tests showed a threshold dispersion without any trimming of $\sim$400 e^- with a ENC $\sim$85 e^-, in very good agreement with CAD simulations.

Recent irradiation test results can be found in [85].

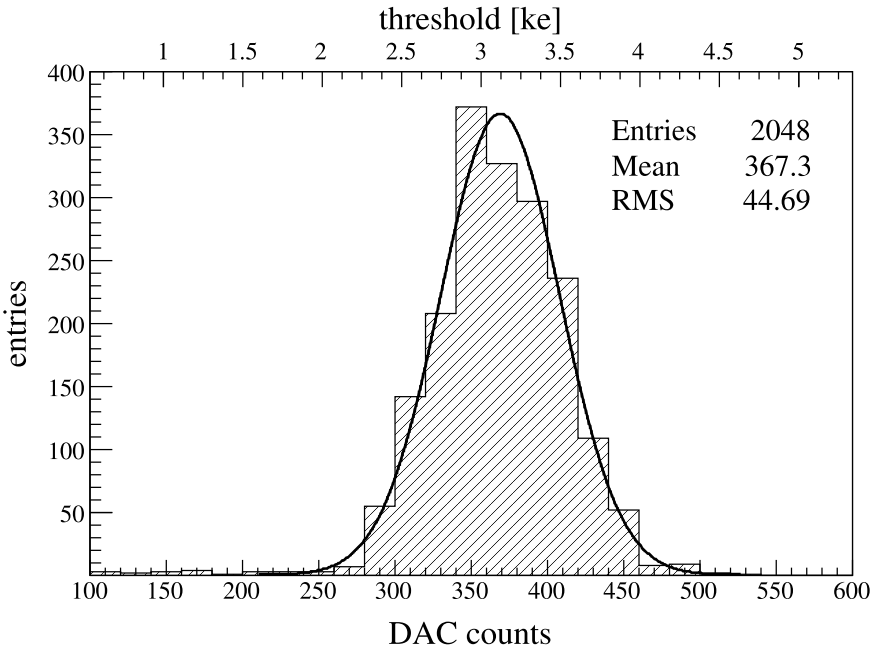


Figure 3.25: Distribution of effective threshold measured for different values of fixed global threshold for the asynchronous front-end (plot via [2]).

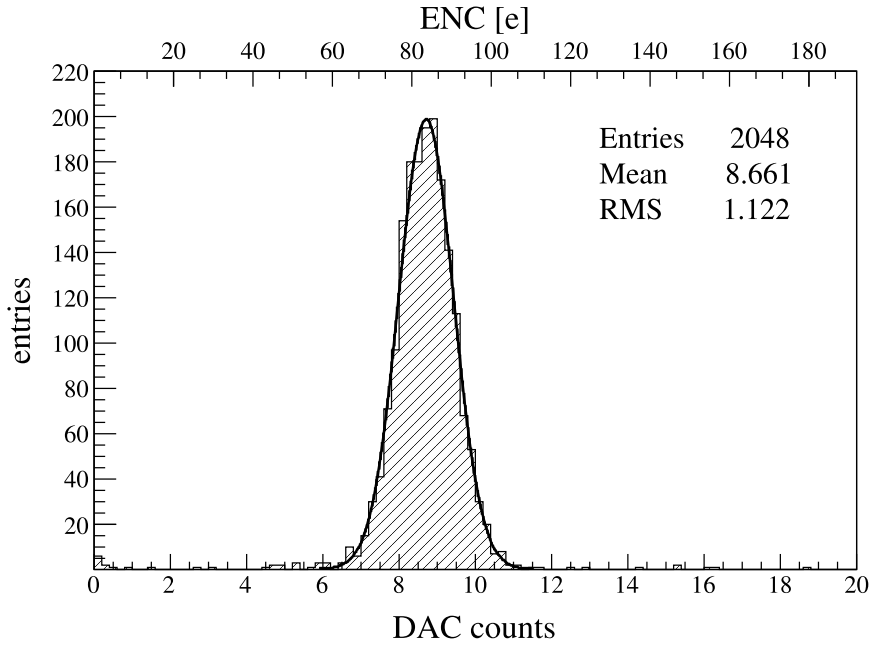


Figure 3.26: Equivalent Noise Charge (ENC) values measured for different values of fixed global threshold for the asynchronous front-end (plot via [2]).

3.4 Conclusions

A new prototype has been designed and tested as part as CHIPIX65 project.
With a cell size of 50×50 μm^2, the matrix is composed by 64×64 pixels with a full system IP-blocks integration.
Two different analog front-ends are included (synchronous and asynchronous design) and a top-down hierarchical workflow has been implemented for a full digital-on-top design methodology.
The test prototypes described in this chapter have been received in September 2016 in Turin and then tested.
Tests shows that both designs are fully working: for the synchronous one, a minimum threshold of $\sim$ 250 e^- with a residual offset of 100 e^- after auto-zeroing has been measured. In addition to that, low noise performance (ENC$\sim$85 e^-) has been achieved for both architectures proving an excellent insulation and integration between digital and analog parts. Irradiation tests have been performed later and results are showed in [85].

Chapter 4

Design and testing of a compact LC-VCO PLL for high-speed data transmission in 65 nm process

4.1 Introduction to phase-locked loops

A remarkable increase of data to be transmitted from the front-end electronics to the data acquisition systems can be observed in actual High Energy Physics experiments, which are continuously improved in terms of beam luminosity and resolution of the detectors.
As a matter of fact, high-speed links, in the range $1 \div 5$ Gb/s or more, are mandatory for high granularity detector as, for example, the silicon pixels.
High frequency clocks can be obtained from an external source by transmitting from the outside to the front-end electronics of the detector. However, for material budget and space reasons, in this specific field it could be convenient to generate the signal straight in the front-end area by using an appropriate circuitry for the multiplication of the system clock.

4.1.1 History and applications

Commonly, a PLL (*Phase-Locked Loop*)[86][87] is a circuit which helps synchronizing (in terms of phase and in frequency) a local reference (generated by an oscillator) with a reference input signal. When the synchronization between the two signals is obtained, the PLL is considered *locked* and the phase error between the local reference and the input signal is constant or zero. When the locking is lost, an internal mechanism allows to adjust the oscillator frequency in order to achieve again the synchronization and to reduce the phase error at minimum. In such a way, the phase of the reference signal is locked to the input one.
PLL can be also used for tracking input frequency or generating a frequency which is multiple of the input frequency; for these characteristics, PLLs are widely employed for computer, radio and telecommunication applications, such as frequency synthesis, computer clock recovery and signals demodulation.
Historically, a first prototype of PLL was designed in 1932 by Henri de Bellescize, a French engineer who firstly was involved in the study of the *coherent communications*. First PLL ICs were realized with discrete components during '60s, and they were totally analog linear devices (LPLLs) build in semiconductor technologies. In these first versions of the circuitry, a four-quadrant multiplier was utilized as phase detector and, for what concern the loop filter, a passive or an active *RC* filter was employed.
Later, digital PLLs (DPLLs, in which the phase detector is digital) came into view during '70s and they actually were hybrid devices (only the phase detector was digitally implemented); all digital PLLs (ADPLLs, where VCO and loop filters are digital as well) were fabricated some years later; in this case, no passive components are included into the design (such as resistors or capacitors).
Software PLLs (SPLLs) and neuronal PLLs are peculiar variants in which functional blocks are implemented just with software designs or neuronal networks rather than with specific hardware.
Because of all these remarkable design differences, no common theory could cover all the PLLs types. For our specific study, digital PLLs theory and traits will be considered in the following sections.

4.2 Phaselock-loop fundamentals

An elementary loop consisting of a phase detector (PD), a loop filter to remove undesired high frequencies and a *voltage-controlled oscillator* (VCO) is considered. In some cases a *current-controlled oscillator* (CCO) is used instead a VCO: here, the signal coming out from the PD is a controlled current source without any differences concerning to the operating principle with respect to a controlled voltage source. If the PLL is used as a frequency synthesizer, another block is inserted between VCO and output: a frequency divider, which allows to obtain an output signal with a higher frequency with respect to the input. Some assumptions concerning the loop

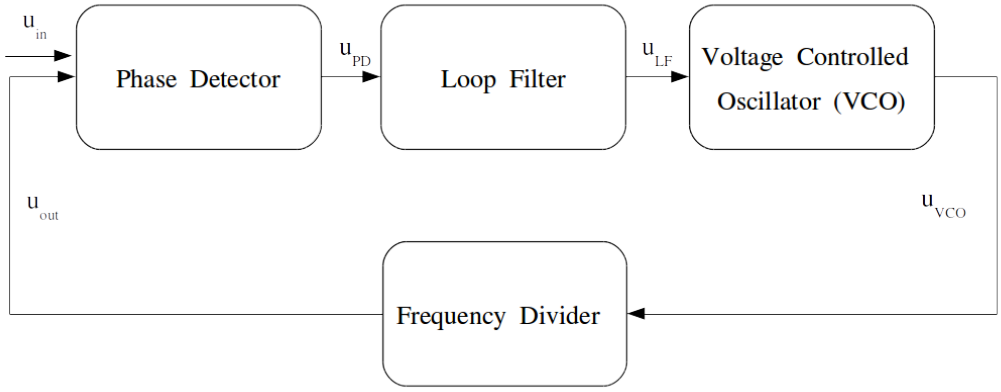


Figure 4.1: A basic phase-locked loop scheme.

need to be made; let us define:

- the phase detector is linear;
- an input signal $u_{in}(t)$ with a phase $\theta_{in}(t)$ and an angular frequency $\omega_{in}(t)$;
- an output signal $u_{out}(t)$ with a phase $\theta_{out}(t)$ and an angular frequency $\omega_{out}(t)$ coming out from the VCO;
- an output signal $u_{PD}(t)$ coming out from the phase detector;
- an output signal $u_{LF}(t)$ coming out from the loop filter.

The VCO works at a ω_{out} frequency, which is defined in the following way:

$$\omega_{out}(t) = K_0 \, u_{LF}(t) + \omega_0 \tag{4.1}$$

where K_0 is the *VCO gain* (rad $\cdot$ s^{-1} $\cdot$ V^{-1}) and ω_0 is its center angular frequency (rad $\cdot$ s^{-1}).
The output voltage $u_{out}(t)$ is proportional to the difference in phase between the two inputs

$$u_{out}(t) = K_d(\theta_{in} - \theta_{out}) = K_d\theta_e \tag{4.2}$$

where K_d is called *phase-detector gain factor* and it is expressed in V$\cdot$ rad^{-1} and θ_e is the *phase error* (rad).

4.2.1 Working principle

The phase detector output signal $u_{PD}(t)$ consists in a DC component superimposed to an AC one, which is deleted by the loop filter. It is possible to distinguish some working stages:

- $\omega_{in}(t) = \omega_0(t)$**:** in this case the VCO works at $\omega_0(t)$ and the error phase θ_e is zero. If θ_e is zero, $u_{PD}(t)$ and $u_{LF}(t)$ are zero as well. Thus, the VCO is able to continue working at the center frequency.

- $\omega_{in}(t)$ after a small time is increased of a $\Delta\omega$ quantity: in this condition, $u_{PD}(t)$ increases with time and $u_{LF}(t)$ as well after some delay given by the filter. For this reason, the frequency $\omega_{out}(t)$ increases and then θ_e decreases. In such a way, the VCO oscillates at the same angular frequency of the reference signal. After some iterations, θ_e reaches the zero value again and the condition $\omega_{in}(t) = \omega_0(t)$ is satisfied again.

4.2.1.1 Noise suppression

Let assume that $u_{in}(t)$ is affected by noise. For this reason $u_{PD}(t)$ starts to oscillate around the average value causing some jittering effects to the signal. $u_{LF}(t)$ would be affected as well, if the bandwidth of the filter itself is not wide enough. Otherwise, the VCO will continue to work to maintain the phase of $u_{out}(t)$ equal to the average phase of $u_{in}(t)$, hence keeping the phase of the output signal controlled.

4.3 Building blocks design and implementation

4.3.1 Voltage Controlled Oscillator (VCO)

Controlled oscillator could be of two different kinds: voltage-controlled (VCOs) or current-controlled oscillators. The main difference between them is the input signal (a voltage signal for the first kind and a current for the second).
The purpose of a controlled oscillator is to obtain a frequency or phase modulation depending on the input signal used. The frequency of the VCO output signal must be proportional to the input control signal coming from the loop filter. The ideal relationship is defined by the Equation 4.2. Even if the behavior of the ideal characteristic is linear, real VCOs work with a unipolar power supply (U_{supply}), so the u_{LF} range is from zero to U_{supply} and they are able to work at the center frequency depending on the control signal, which must be half of the supply voltage:

$$\omega_{out} = \omega_0 + K_0(u_{LF} - U_{supply}/2) \tag{4.3}$$

Furthermore, another limitation is about the output frequency of a practical VCO, which may not vary proportionally to the full range from zero to U_{supply} but with respect to a restricted range. In view of the above, the two key parameters for the VCO are the center frequency ω_0 and the VCO gain K_0.

4.3.2 Phase detector (PD)

The *phase detector* is the first element encountered in the chain of a PLL. Its purpose is to detect the differences in phase (and also in frequency, in the case of a *phase-frequency detector*) between the input signal and the feedback one hailing from the oscillator.

4.3.2.1 Multiplier phase detector

From an historical point of view, the first circuit used as a phase detector in linear PLL is the so-called *four-quadrant multiplier phase detector*, which was an analog device; lately digital PD became common (EXOR gates, edge-triggered JK-FF,

Phase-Frequency Detectors knows as *Phase-Frequency Detector* (PFD), as described in the following paragraphs. For a multiplier phase detector we can assume the input signal of the PLL as a sinusoidal signal

$$u_{in}(t) = U_{in-0}\sin(\omega_{in}t + \theta_{in}) \tag{4.4}$$

where U_{in-0} in the amplitude of the waveform, ω_{in} is the angular frequency (rad/s) and θ_{in} is the phase. As a second input signal, a Walsh [1] function (such like a symmetrical rectangular wave) can be used

$$u'_{out}(t) = U_{out-0}\text{rect}(\omega'_{out}t + \theta'_{out}). \tag{4.5}$$

For the sake of simplicity, let us assume:

- the phase is constant for all the waveforms;
- phases θ_{in} and θ_{out} are equal to zero;
- θ'_{in} and θ'_{out} are non-zero phases.

By multiplying $u_{in}(t)$ and $u'_{out}(t)$, the multiplier output signal can be obtained

$$u_d(t) = u_{in}(t) \cdot u'_{out}(t). \tag{4.6}$$

Introducing a formal Fourier analysis notation, we can write:

$$u'_{out}(t) = U_{out-0}\left[\frac{4}{\pi}\cos(\omega'_{out}t + \theta'_{out}) + \frac{4}{3\pi}\cos(3\omega'_{out}t + \theta'_{out}) + ...\right] \tag{4.7}$$

hence

$$u_d(t) = U_{in-0}U_{out-0}\sin(\omega_{in}t + \theta_{in})\left[\frac{4}{\pi}\cos(\omega'_{out}t + \theta'_{out}) + \frac{4}{3\pi}\cos(3\omega'_{out}t + \theta'_{out}) + ...\right]. \tag{4.8}$$

[1] Walsh functions comprehend a complete and orthogonal set of functions which represent the discrete digital counterpart of analog and continuous system of trigonometric functions used in Fourier analysis.

PLL locked. The condition of locking for the PLL system is stated when

$$\omega_{in} = \omega'_{out} \tag{4.9}$$

is satisfied; this implies

$$u_d(t) = U_{in-0}U_{out-0}\left[\frac{2}{\pi}\cos(\theta_{in} - \theta'_{out}) + ...\right] \tag{4.10}$$

where

$$\theta_e = (\theta_{in} - \theta'_{out}) \tag{4.11}$$

is the *phase error* between the two signals. Since the first term of these series is the DC term, then the remaining ones represent the higher frequency terms, which can be suppressed by the loop filter and then ignored in this dissertation; for this reason, $u_d(t)$ can be written like

$$u_d(t) \approx K_d \sin\theta_e \tag{4.12}$$

where K_d is the *phase detector gain* and it is defined such as

$$K_d = \frac{2U_{in-0}U_{out-0}}{\pi} \tag{4.13}$$

For small phase errors ($\theta_e \approx 0$), $\sin\theta_e \approx 1$, so we have

$$u_d(t) \approx K_d \tag{4.14}$$

which is the phase detector linearized model.

PLL unlocked. When the PLL is unlocked, since we have

$$\omega_{in} \neq \omega'_{out} \tag{4.15}$$

the output signal can be written as

$$u_d(t) = K_d \sin(\omega_{in}t + \theta_{in} - \omega'_{out}t + \theta'_{out} + ...) \tag{4.16}$$

Higher harmonics are hence removed by the loop filter; remaining terms are DC plus an AC term containing $\omega_1 - \omega'_2$ and this could suggest an average output signal

equal to zero, which would prevent the loop to get the lock. However, it could be demonstrated that the u_{PD} signal is an asymmetric sine wave, so a non-zero DC component could be obtained; it allows to push up or down the VCO frequency until the lock is reached.

4.3.2.2 EXOR phase detector

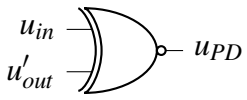


Figure 4.2: EXOR phase detector scheme.

EXOR phase detector are employed in digital PLLs. Thus, square wave input signal for the EXOR can be considered. Let us assume u_{in} and u'_{out} as input symmetrical square wave and let analyze two different situations.

Figure 4.3: EXOR phase detector waveforms. a) Zero-phase case. b) Case with a positive phase θ_e.

Zero phase error case: let us consider two signal u_{in} and u'_{out} out of phase of exactly 90 degrees (Fig. 4.3 *a)*). So the output signal u_{PD} frequency is twice the reference one and its duty cycle is precisely of 50%; Only the average value $\overline{u_{PD}}$ is considered because of the filtering of higher frequencies; it is represented by the dashed line and its value is the arithmetic mean of the two logic values; since it could be denoted as the quiescent point of the gate EXOR, in Fig. 4.3 is put equal to zero by definition.

Non-zero phase error case: if the two signals u_{in} and u'_{out} are out of phase, θ_e and the average value of u_d become positive since the duty cycle increases.
In general, it is clear that the phase error u_d oscillates between $-90^\circ < \theta_e < 90^\circ$ and follows a triangular trend, with respect to the sinusoidal trend of the four-quadrant multiplier; the average value is

$$\overline{u_{PD}} = K_d \theta_e \tag{4.17}$$

where the gain K_d is a constant and it is worth

$$K_d = \frac{U_b}{\pi} \tag{4.18}$$

by assuming a system with U_b and 0 as logic levels. For a EXOR phase detector

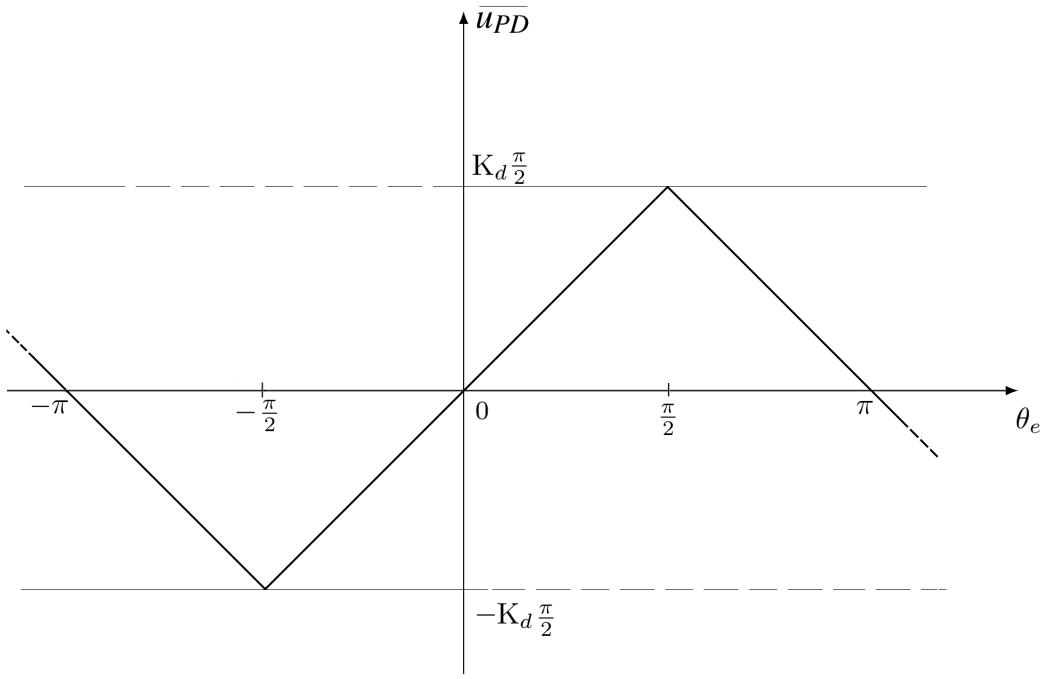


Figure 4.4: EXOR phase detector averaged output signal versus phase: case with u_{in} and u'_{out} symmetrical square waveforms.

is possible to maintain the phase locking if the phase error is enclosed between $-\frac{\pi}{2} < \theta_e < \frac{\pi}{2}$. Furthermore, if input signals u_{in} and u'_{out} are strongly asymmetrical, a clipping phenomenon can be noted in the average output value.

4.3.2.3 JK-FF phase detector

The JK-flipflop phase detector is an edge triggered device whose output Q assumes an high state value if a positive edge triggers the J input, whereas Q assumes a low value if the K input assumes a positive edge.

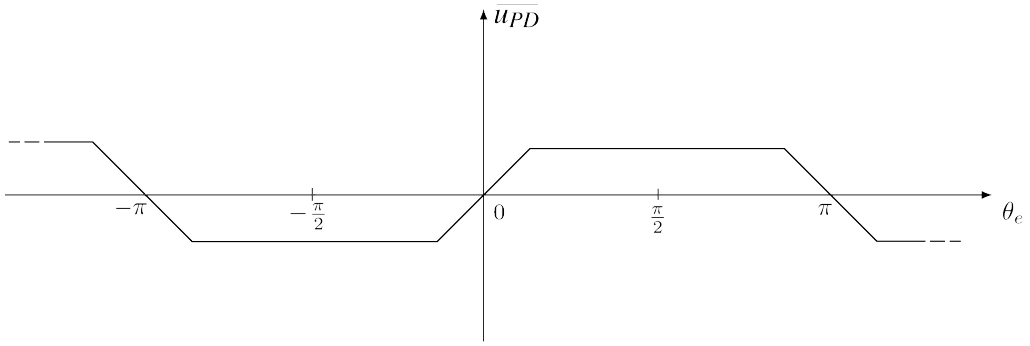


Figure 4.5: EXOR phase detector averaged output signal u_{PD} versus phase: case with u_{in} and u'_{out} asymmetrical square waveforms. It is possible to see a clipped curve behavior.

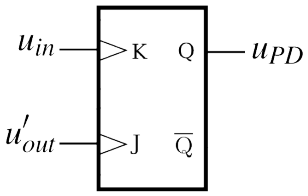


Figure 4.6: JK-flip flop phase detector scheme.

Zero phase error case: in this case the two input signals u_1 and u'_2 have opposite phase and the output signal u_{PD} is a square wave with the same frequency as the input signal; thus, the average value is zero since the duty cycle is 50%.

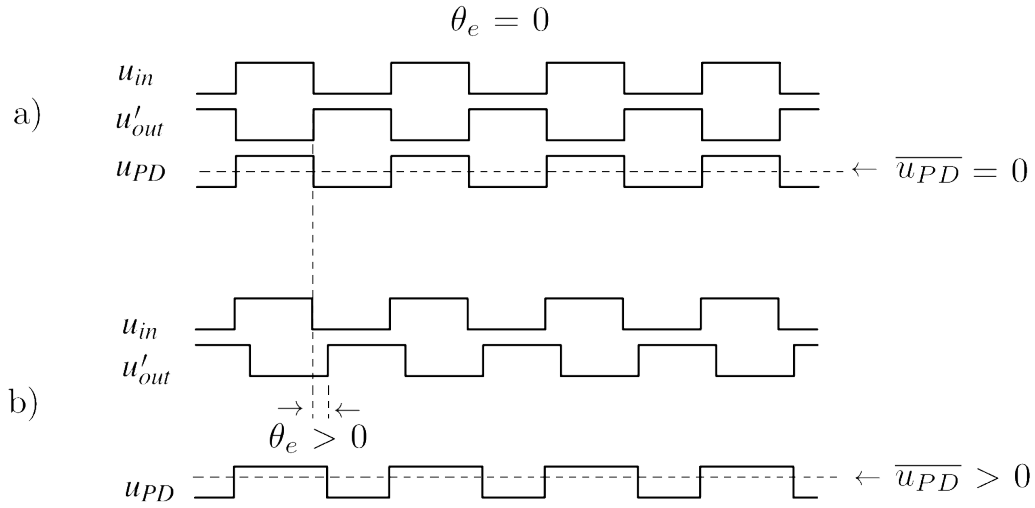


Figure 4.7: JK-flip flop phase detector waveforms. a) Zero-phase case. b) Case with a positive phase θ_e.

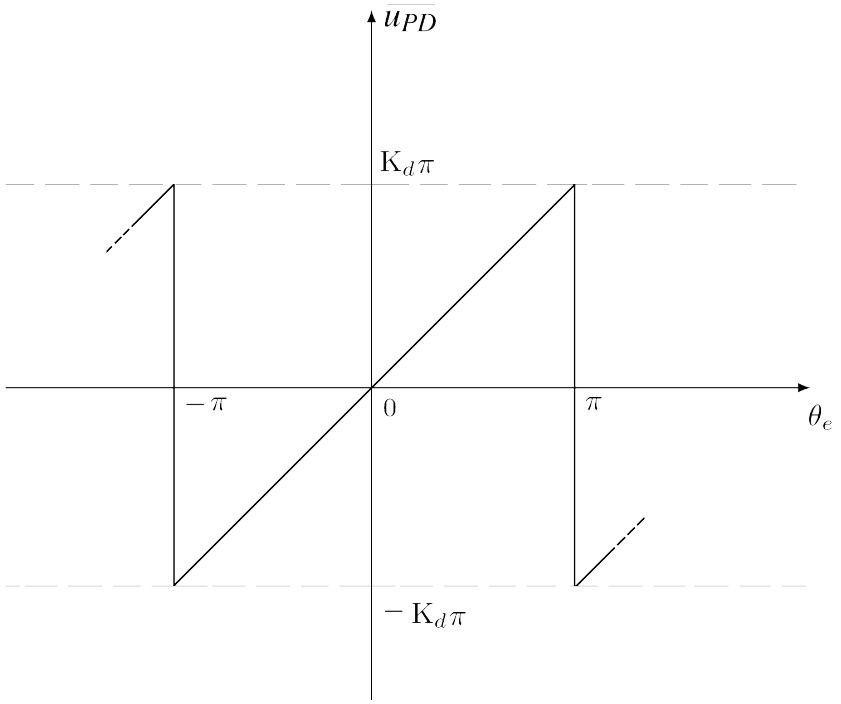


Figure 4.8: EXOR phase detector averaged output signal versus phase: in this case, in contrast with the previous ones, the asymmetry between input signals does not produce clipping.

Non-zero phase error case: when $\theta_e > 0$, the duty cycle becomes greater than 50% and $\overline{u_{PD}}$ becomes positive. It can be written as

$$\overline{u_{PD}} = K_d \theta_e \tag{4.19}$$

where the gain K_d is a constant and it can be demonstrated that

$$K_d = \frac{U_B}{2\pi} \tag{4.20}$$

where the logic level could be zero or U_B. Locking condition can be preserved in the range of $\pi < \theta_e < \pi$ and the characteristic plot is drawn in Fig. 4.8 For a JK-FF phase detector, the symmetry between input signals is pointless.

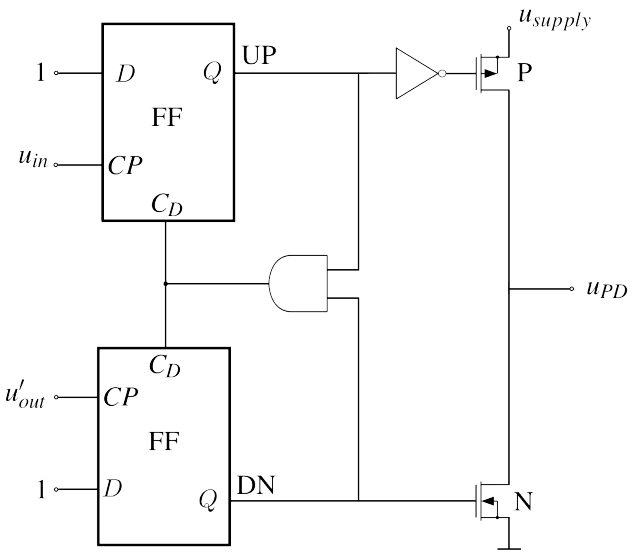


Figure 4.9: Phase-Frequency detector general scheme.

4.3.2.4 Phase and frequency detector

Whereas the phase detector notices differences just for what concerns the phase error θ_e of input signals, phase and frequency detector takes into account also angular frequency differences $\Delta\omega$ when the PLL is not yet in a locking condition. The traditional scheme is built by using two D-FF, which will be denoted as UP-FF and DOWN-FF. Four states can be defined (see Table 4.1).

UP output	DOWN output	STATE	output signal u_d
0	0	-1	negative
1	0	0	zero
0	1	+1	positive
1	1	[inhibited by the AND gate]	-

Table 4.1: Possible states for the PDF.

Practically, the PFD behaves like a tristate device, so it is possible to assign three different values to the outputs state: -1, 0, +1. On the other hand, when both UP and DOWN signals be worth 1, by mean of the AND gate, a logic high level output can reset both the flip-flops. The state diagram in Fig. 4.10 explains the variation of u_{in} and u'_{out}, assuming positive-edge transitions between logic states. The output signal

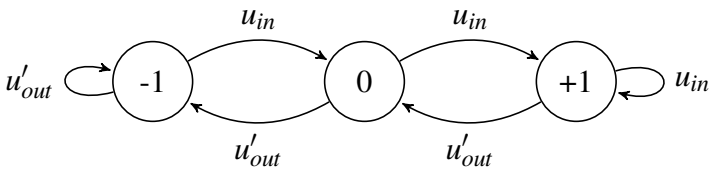


Figure 4.10: PFD state machine. State variations are rising-edge defined.

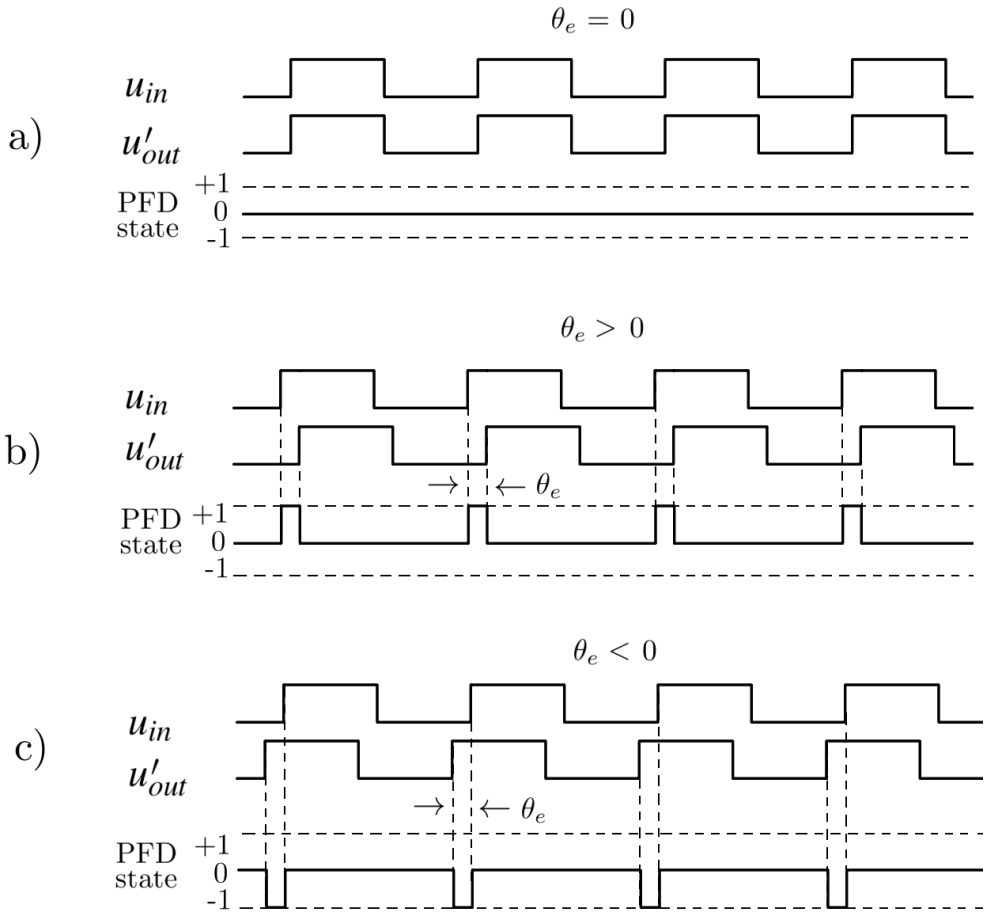


Figure 4.11: PFD phase detector waveforms. a) Zero-phase case. b) Case with a positive phase θ_e. c) Case with a negative phase θ_e.

u_{PD} in Fig. 4.9 is a function of the PFD state (Table 4.1). In order to understand the behavior of a realistic PFD, let us see Fig. 4.11

a) Initial state: 0, u_{in} and u'_{out} in phase, u_{in} and u'_{out} positive edge aligned (phase error equal to zero)$\rightarrow$ the PFD remains in 0 state .

b) u_{in} and u'_{out} positive edge not aligned (u'_{out} late with respect to $u_{in} \rightarrow$ the PFD

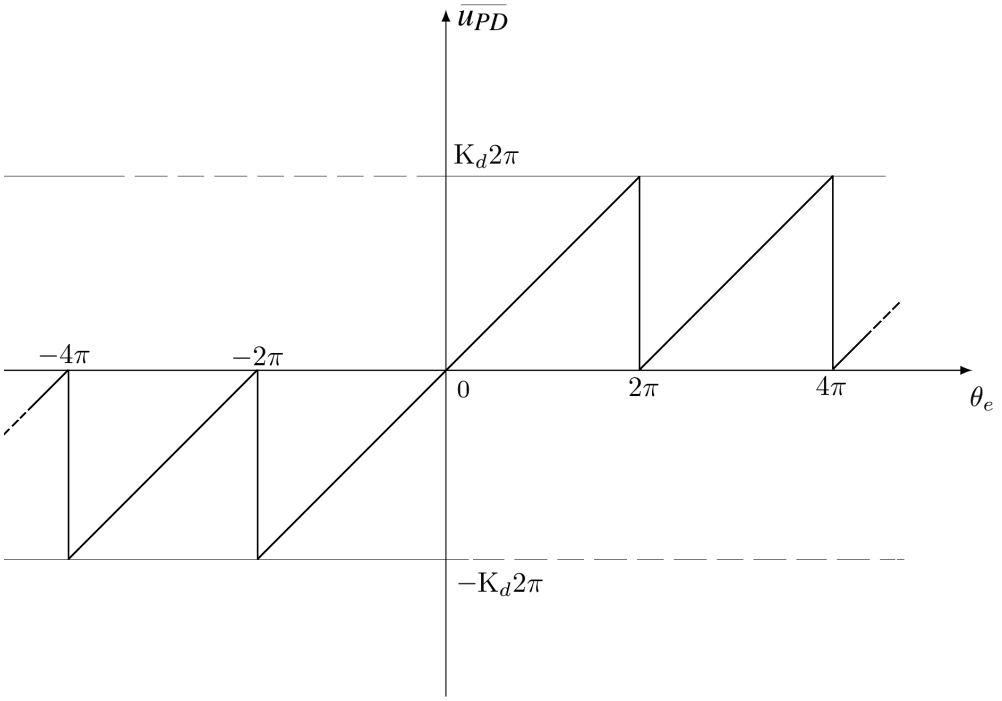


Figure 4.12: PFD average of u_d; here are depicted values for phase error values greater than 2π and smaller than -2π as well.

toggles between -1 and 0 state.

c) u_{in} and u'_{out} positive edge not aligned (u_{in} late with respect to u'_{out} $\rightarrow$ the PFD toggles between 0 and +1 state.

Plotting the average of the PFD output signal u_d in these three cases versus the phase error θ_e, we obtain the sawtooth waveform in Fig. 4.12.
Taking into consideration the range of phase error between $\pm 2\pi$, the average output signal is

$$\overline{u_{PD}} = K_d \theta_e \tag{4.21}$$

and the phase detector gain is worth:

$$K_d = \frac{U_B}{4\pi} \tag{4.22}$$

where, again, the logic level could be zero or U_B.
The advantage of using a PFD in most cases instead a JK-FF lies in the case of initial

unlocking of the PLL; actually it could be demonstrated [86] that the $\overline{u_{PD}}$ varies monotonically with the frequency error $\Delta\omega = \omega_1 - \omega_2$ when the PLL is unlocked; as said before, it varies with the phase error when the PLL is locked. This trait cannot be shown for both the EXOR and the JK-FF and allows a PLL which has a PFD in its building block locking regardless loop filter used.

4.4 Jitter

4.4.1 Timing jitter

Electrical systems which use voltage transitions in order to represent timing transitions are usually subjected to undesired noise effect known as timing-jitter[88]. Jitter appears as the deviation of timing edges from their ”correct” positions. A simple definition suggested by SONET (Synchronous Optical Network) is:
Jitter is defined as the short-term variations of a digital signal's significant instants from their ideal positions in time.
Even though this definition allows us to understand the essence of jitter, some further clarification needs to be done on the terms ”short-term”, ”significant instant”, ”ideal positions”.

Short-term variations. Timing variation can be distinguished in two class: *jitter* and *wander*, based on a Fourier analysis of these variations with respect to time. If time variations occurs slowly, which means below 10 Hz according to ITU (International Telecommunication Union definitions) we can talk about wander; otherwise jitter is a term more suitable to use.

Significant instants. ”Significant instants” are the precise moments when the transitioning signal passes through selected amplitude threshold, referred to a reference level or a threshold. ”Digital signal” need to be specified as well: for high-speed signals, transitions must be considered as analog phenomena sensitive to slew-rate and rise-time limitations: every voltage noise could corrupt the signal introduncing jitter in the waveform behavior.

Ideal positions For a clock-like signal, the ideal positions can be identified with a clock signal not-affected by jitter with the same mean frequency and the same phase. For a data signal a *clock recovery* procedure needs to be done in order to establish the timing of the referece clock signal.

4.4.1.1 Different kind of jitter

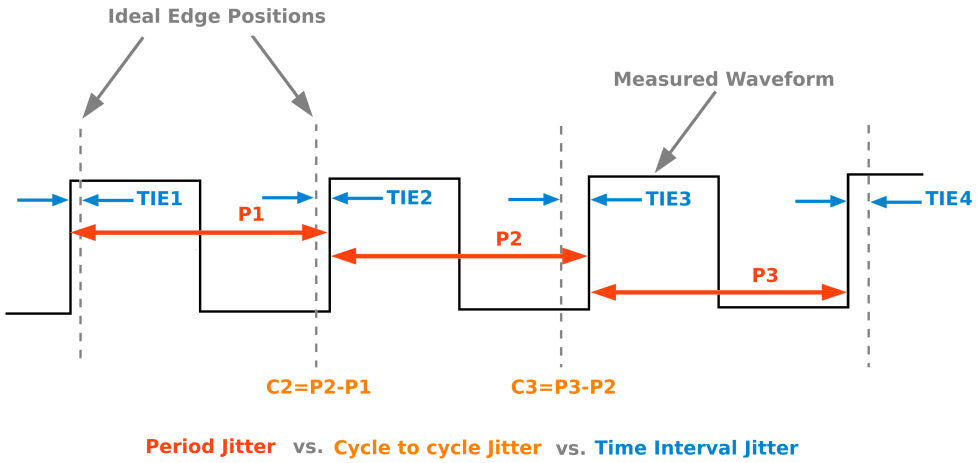


Figure 4.13: Different measurement of jitter. Dotted vertical lines represent ideal positions of the edges of a jitter-free clock-like signal.

There are three different ways to measure jitter affecting a single signal: *period jitter*, *cycle to cycle jitter* and *TIE* (Time Interval Error). In order to perform a complete analysis of the signal, a good understanding of the similarities and differences between them need to be done.

Period Jitter Period Jitter (in Fig. 4.13 indicated with P1, P2 and P3 in red) is the measure of the period of each cycle of the signal waveform. It is a peak-to-peak measure and it is the simplest way to reveal jitter influence into signal transmission. Jitter, if present, distorts the signal increasing or reducing the nominal waveform period.

Cycle to Cycle Jitter Cycle-to-Cycle Jitter (in Fig. 4.13 indicated with C2 and C3 in orange) shows the differences between periods for two adjacent signal cycles.

Time Interval Error (TIE) TIE (in Fig. 4.13 indicated with TIE1, TIE2, TIE3 and TIE4 in blue) measures how much the real edge of the clock moves away from its ideal edge position. For this measure, ideal edge position must be known. TIE analysis allows to understand how the cumulative effect of small amount of period jitter could affect the long-term behavior of the signal.

4.5 The prototype

A prototype of a compact low-jitter PLL developed for high-frequency clock multiplication has been developed in a CMOS 65 nm process. Generally in HEP, clock multiplication is realized by mean of ring oscillator VCOs since the achievable reduced size of the circuit [89][90][91]. However, LC-VCOs show better jitter performance with respect to ring oscillator ones but need more space for the implementation [92][93] because of the presence of the inductor integrated in it. This PLL, developed in the framework of the INFN CHIPIX65 CSN5 research project [61] shows a good trade-off between jitter and die area, which could represent an optimum in HEP experiment where good noise performance and small dimensions are strongly needed.

4.5.1 Design and implementation

The prototype scheme (Fig. 4.14) is based on the charge-pump PLL model [87]. By mean of a Phase and Frequency Detector (PFD), the 160 MHz input is compared to the 5.12 GHz clock signal generated by the VCO, after a 32$\times$ division. The phase difference signal is sent to the charge-pump circuit (CP) which manages the VCO control voltage. The frequency division is made in two step with two different divider circuits: the first one implemented in Current-Mode Logic (CML) in order to work properly at multi-GHz frequencies, and the second one designed in Standard-Cells (SC), aiming to save power.

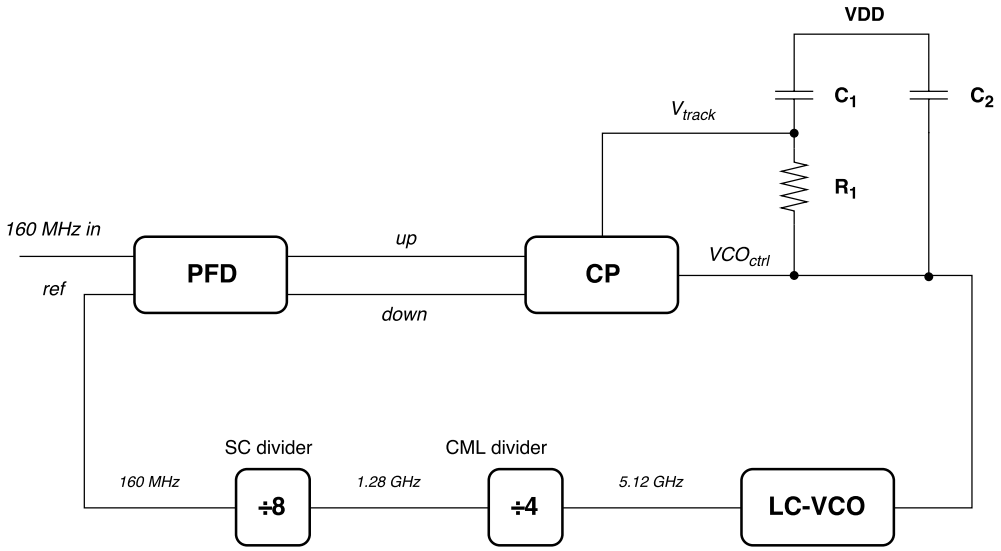


Figure 4.14: PLL general and simplified schematic.

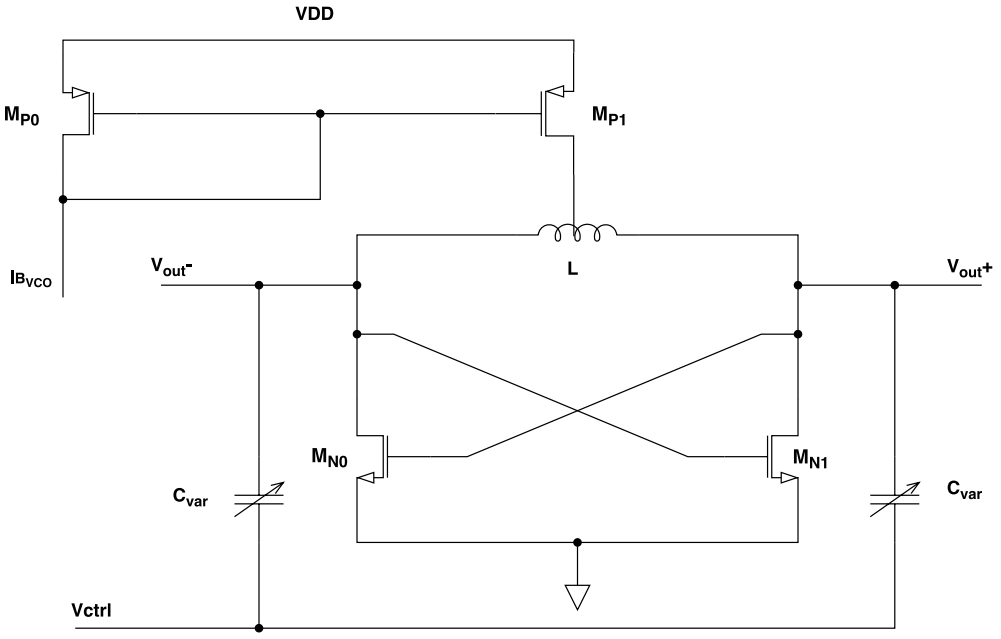


Figure 4.15: VCO general schematic.

4.5.1.1 LC-Voltage Controlled Oscillator

The VCO (Fig. 4.15) implemented for the PLL prototype, is based on the cross--coupled g_m-cell topology with an integrated LC resonator [94][95][96]; the frequency equal to:

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \tag{4.23}$$

The VCO common mode voltage is about half of the supply voltage; the output voltage swing is about 600 mV. nMOS transistors M_{N0} and M_{N1} get the negative impedance useful to balance the equivalent parallel resistance of the resonator, while pMOS transistors M_{P0} and M_{P1} have bias purposes. The VCO architecture is merely based on a nMOS design due to speed motivations (no switching pMOS and minimal parasitic capacitance) and good supply rejection [97].
The VCO tuning range is 4.8÷6 GHz with a nominal output frequency of 5.12 GHz for an input voltage of 600 mV. The oscillator output voltage can be defined such as

$$V_{OUT} = R_P I_{B_{VCO}} = 2\pi f_{osc} Q L I_{B_{VCO}} \tag{4.24}$$

where R_P is the parallel equivalent resistance of the LC resonator, $I_{B_{VCO}}$ is the bias current for the VCO, Q is the quality factor of the inductor which is directly proportional to its dimensions [98]. This relation shows that an higher f_{osc} allows a lower Q factor (and thus a smaller inductor) or a lower $I_{B_{VCO}}$ (which means a lower power consumption).
Here, the octagonal-shaped with center tap (T-coil) inductor is characterized by a total inductance of 1.54 nH with Q=17 and its size is 185×168 μm^2.
With respect to two single inductors, the T-coil shows a smaller area and a better matching compared to the case of the two inductances. Some n-MOS in n-well varactors are used as variable capacitances, with a value range of 900÷1.3 pF. The bias current is set at 5 mA. A differential buffer stage follows the VCO circuit with resistive load which helps the optimization of the oscillator load and its decoupling from PFD; this driver needs 2 mA and produces an output voltage in the range of 600÷VDD, which fits the CML stage of the frequency divider voltage requirements.

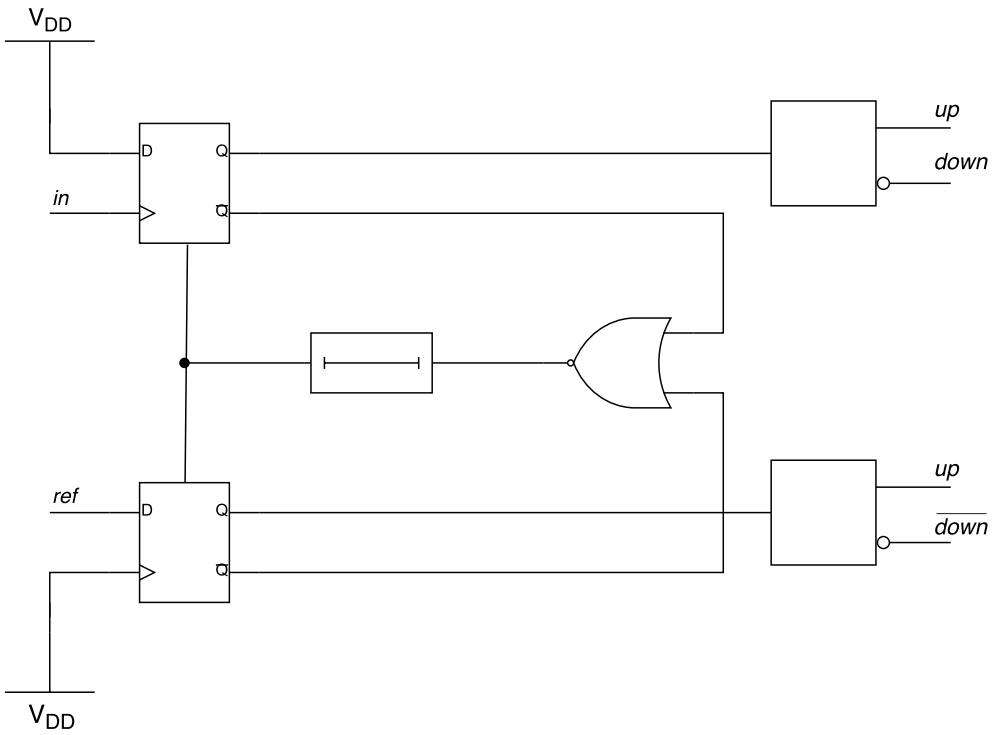


Figure 4.16: Phase and frequency detector scheme.

4.5.1.2 Frequency and Phase Detector

The implemented Phase-Frequency Detector is based on the Fig. 4.16 scheme. The input and the reference signal are compared by mean of the two edge detectors; based on which edge commutes first, one of the output (*up* and *down*) are set high; after the arrive of the second edge, the signal is then reset. On the reset path a short delay is set in order to have a little time during which both signals are high, avoiding dead time in the circuit. Edge detectors are reset each clock period, so no triple-redundancy is implemented. The combination of each PFD input with the reference clock provides a lock signal which is equal to 1 during the lock condition of the PLL. At the VCO input during one clock cycle, at the nominal condition of charge pump current and loop capacitance, the maximum voltage variation is <2 mV, which is a phase variation of $<0.1\%$.

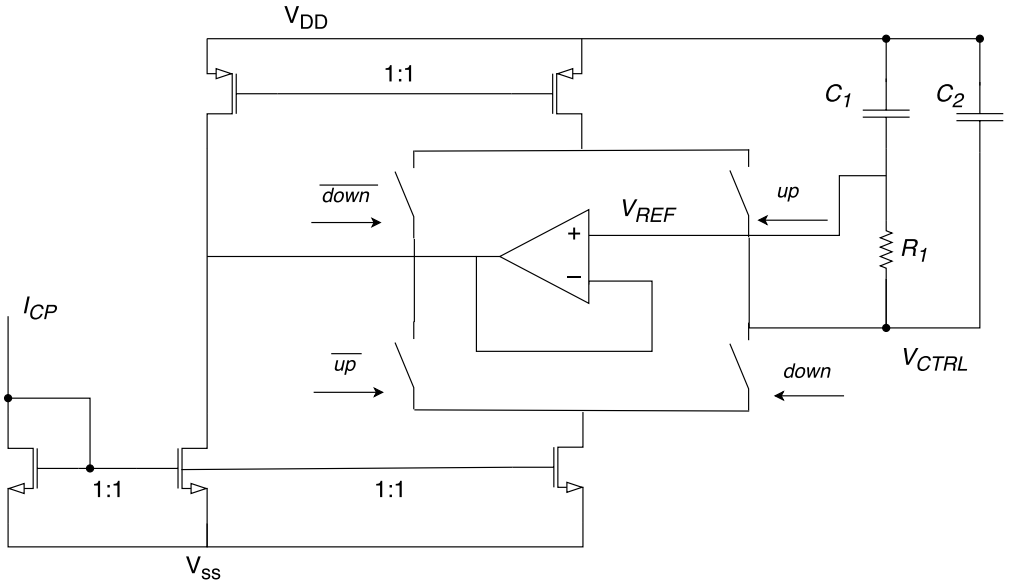


Figure 4.17: Charge-Pump circuit schematic.

4.5.1.3 Charge pump PD

The purpose of the Charge-Pump circuit is to convert the phase difference coming from the Phase and Frequency detector into a current which is in turn converted in a voltage with a loop filter; this voltage is used to control the VCO [99].
A Charge Pump model has been developed by F. M. Gardner in [87]. In particular, a distinction between a second-order and third-order RC loop filter has to be done. For the majority of the cases, third-order loop filters are utilized. In order to obtain a zero-stabilized loop filter, the loop filter function

$$Z_{F2} = R_2 + (sC)^{-1} \tag{4.25}$$

can be derived taking into account the series connection of resistors and capacitances. In order to characterize the time-averaged and linearized PLL behaviour, these relations

$$K = 2\zeta\omega_n \tag{4.26}$$

$$K\tau 2 = 4\zeta^2 \tag{4.27}$$

$$K/\tau 2 = \omega_n^2 \tag{4.28}$$

can be obtained by calculating these parameters:

$$\tau_2 = R_2 C_2 \tag{4.29}$$

$$\omega_n = \sqrt{\frac{K_0 I_p}{2\pi C}} \tag{4.30}$$

$$\zeta = \frac{\tau_2}{2}\sqrt{\frac{K_0 I_p}{2\pi C}} \tag{4.31}$$

$$K = \frac{K_0 I_p R_2}{2\pi} \tag{4.32}$$

where K is the loop gain, ω_n is the natural frequency, ζ is the damping factor, I_p is the pump current, R is the loop filter resistance, C is the loop filter capacitance, τ is the time constant of the loop filter. Even though the majority of the applications utilize second-order filters, in order to obtain a purer frequency spectrum by mitigating granularity and ripple issues, an additional filter could be used thus providing a third-order loop. The simplest way is adding a second capacitor in parallel to the earlier filter RC impedance. In such a way, the loop filter function becomes

$$Z_{F3} = \left(\frac{b-1}{b}\right)\frac{s\tau_2 + 1}{sC\left(\frac{s\tau_2}{b} + 1\right)} \tag{4.33}$$

where

$$b = 1 + \frac{C}{C_3} \tag{4.34}$$

A loop filter transfer function can be thus obtained

$$H(s) = \frac{K\left(\frac{b-1}{b}\right)\left(s + \frac{1}{\tau_2}\right)}{\frac{s^3\tau_2}{b} + s^2 + K\left(\frac{b-1}{b}\right)s + \frac{K(b-1)}{b\tau_2}} \tag{4.35}$$

which has a third-degree denominator (thus the PLL is third-ordered).

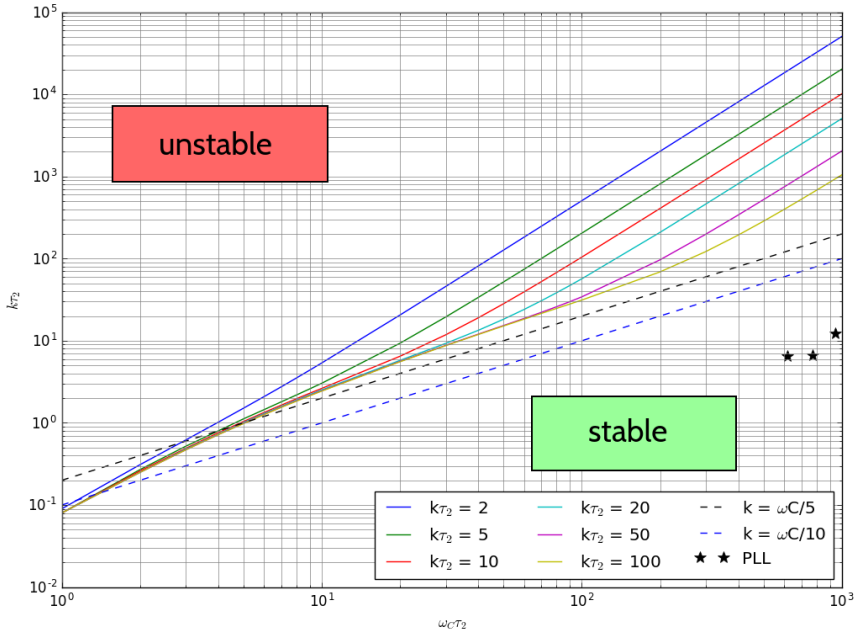


Figure 4.18: Stability limits (third order loop) for different values of b: values above the curve depict unstable loops while values below represent stable loops.

Studies on the stability limits based on the study of the value b with some transient response analysis can help to develop a good design. In Fig. 4.18 stability limits for different values of b. Given b and $\omega_i\tau_2$ values, any $K\tau_2$ value above the curve represents an unstable loop, while any below is yields a stable one. Little black stars (below the curves) correspond to the slow/typical/fast corner simulation of the prototype. Current mirrors provide bias current to nMOS and pMOS transistor used for up-down current generation purposes. These two are characterized by high output impedance (obtained by designing transistor with long length) to reduce the mismatch between different current sources because of different V_{DS}. To equalize the voltage on the two branches during the switching, a unity-gain amplifier is implemented.

In order to obtain the VCO voltage, the integration of the current happens over a 32 pF capacitor; to filter the noise and provide loop compensation, a resistor (24 Ω) and three capacitor (3 pF each). The dumping factor of the loop filter is equal to 1.27 (Figure 4.17).

4.5.1.4 Frequency Divider

As mentioned above, the frequency divider is made of two stages: the first one, which is a divider by 4, and a second one which divides by 8 (Fig. 4.14). The frequency divider is split into a divider by 4 and a divider by 8. The first one is based on a CML (Current-Mode Logic [100]) circuitry: this helps to overcome the high frequency of the oscillator. Since high-speed CML requires high current levels and thus quite large transistors (compared to standard cells ones), their larger capacitance restricts the probability to have a SEU-induced switch from one state to the other [101][102]. Furthermore, since CML is differential, the minimum charge required to have an upset doubles. A differential to single-ended converter is put at its output; it operates as the input of the second stage of the divider, this time based on standard cells. Four dividers by two are used in cascade in order to obtain a divider by 8. For radiation hardness purposes, each of them is designed with triple redundancy correction by using three D flip-flops and three majority voter circuits. The divider output and the input clock are then re-synchronized.

4.5.1.5 Output Driver

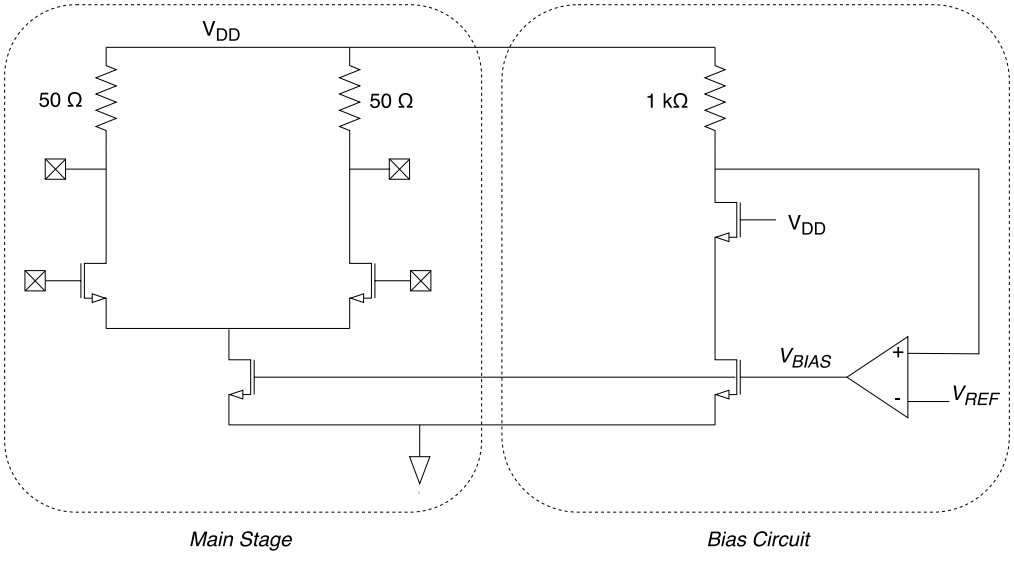


Figure 4.19: Output driver schematic.

The high-speed output driver is based on CML design with nMOS differential pairs. The output current is 10 mA with a 50 Ω load (to match the 50 Ω line

Parameters	**Value**
Process	commercial CMOS 65 nm
Die Area	$335 \times 370\ \mu m^2$
Test Chip Size	$1 \times 1\ mm^2$
Input Frequency	160 MHz (4× LHC clock)
VCO Running Frequency	5.12 GHz
Frequency Divider	32×
Tuning Range (for 600 mV input voltage)	4.8÷6 GHz
Supply Voltage	1.2 V
Common Mode VCO Voltage	600 mV
Internal Inductance	1.54 nH
Inductor Quality Factor (Q)	17
Inductor Size	$185 \times 168 \mu m^2$
Output Voltage Swing	600 mV
Filter Dumping Factor (all process variations)	1.27
Jitter	< 6 ps RMS
Power Consumption	18 mW

Table 4.2: LC-VCO PLL summarized parameters.

impedance) switched on one or another side of the pair. In order to guarantee the correct output voltage over temperature and process, the circuit is biased via a replica circuit. Given V_x the voltage on the minus node of the operational amplifier, we have

$$\frac{V_{DD} - V_x}{50 \times 20\Omega} = \frac{I_{BIAS}}{20} \tag{4.36}$$

and since V_x is forced to V_{REF}, we can say that the bias current is equal to

$$I_{BIAS} = \frac{V_{DD} - V_{REF}}{50} \tag{4.37}$$

so the output voltage is equal to

$$V_{OUT} = V_{DD} - I_{BIAS} \times 50 \tag{4.38}$$

which means when 4.37 is true

$$V_{OUT} = V_{DD} - \frac{V_{DD} - V_{REF}}{50} \times 50 = +V_{REF} \tag{4.39}$$

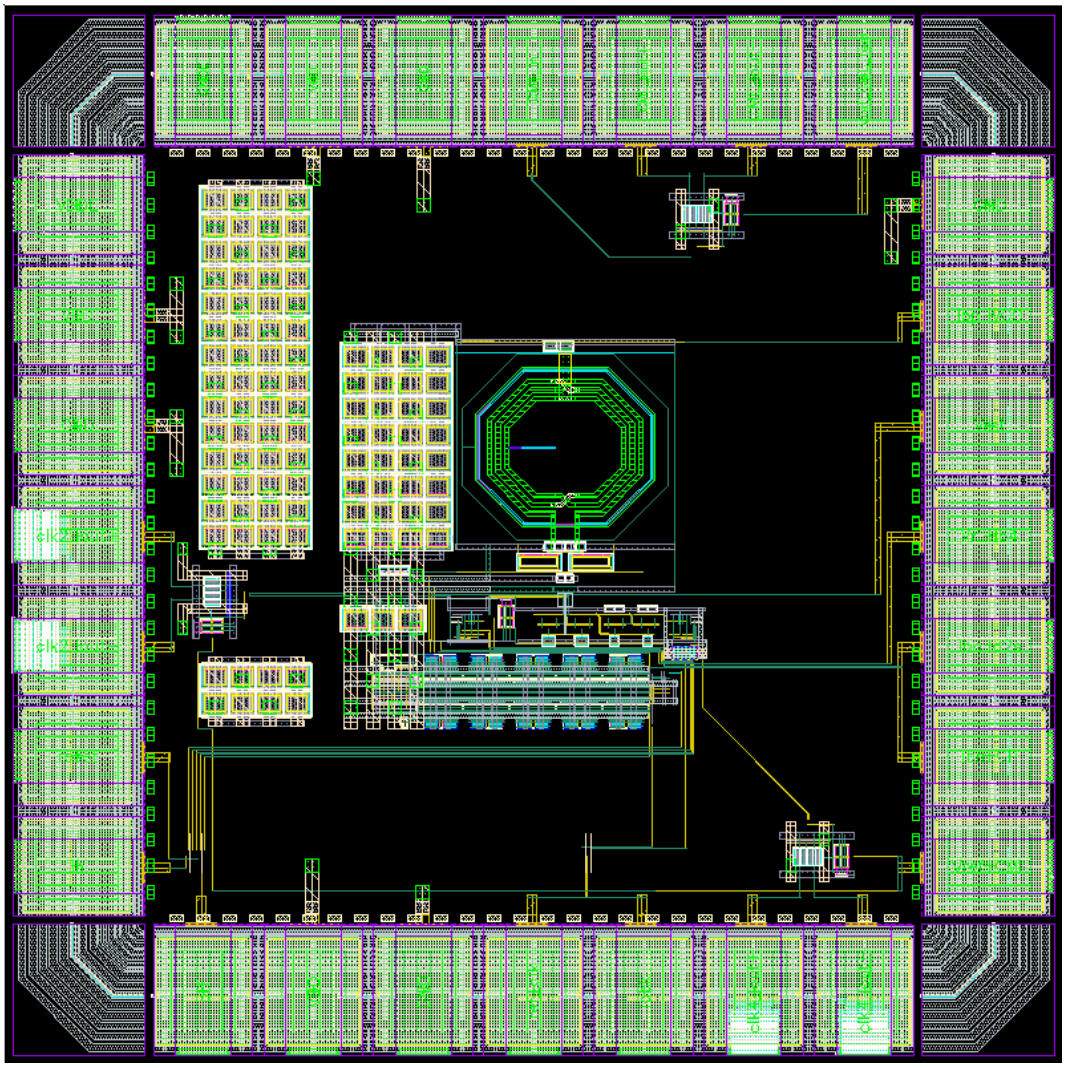


Figure 4.20: ECAD schematic view of the layout of the circuit.

4.5.2 Test results

The LC-PLL [101][102], once produced, has been tested in Torino and X-rays irradiation has been done in Padova in 2017. PLL laboratory measurements has

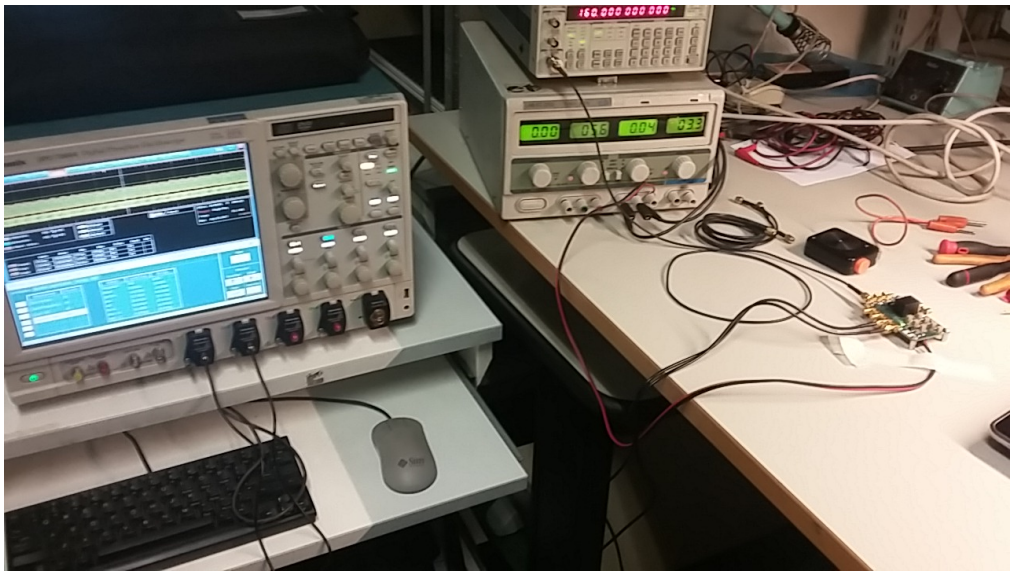


Figure 4.21: Test setup in Torino (Electronic Laboratory).

been done at the output $F_{VCO}/4$ (1.28 GHz) and $F_{VCO}/32$ (160 MHz); theoretically, the frequency division should not change the jitter level in the signal. Firstly, the PLL has been tested keeping it in reset mode and controlling just the input voltage of the VCO by mean of an external voltage supply. In Fig. 4.23, a comparison between simulated and measured data of the output frequency vs. the control voltage of the LC-VCO. The VCO gain is equal to 1.85 GHz/V (VCO gain in simulation is equal to 1.9536 Gz/V, 5.6% lower) and the jitter range is 2.25÷2.45 ps (see Fig. 4.24).

Output	**Av. Period Jitter [ps]**	**Av. TIE Jitter [ps]**
$F_{VCO}/4$ (1.28 GHz)	3.55	3.23
$F_{VCO}/32$ (160 MHz)	2.23	1.93

Table 4.3: Average period/TIE jitter values.

Afterwords, the PLL has been connected to a programmable clock generator (frequency range 150÷190 MHz, average jitter of 1.85 ps). By using the internal software of the oscilloscope, the picture in Fig. 4.25 showing the eye diagram of the signal and the TIE jitter distribution is obtained.

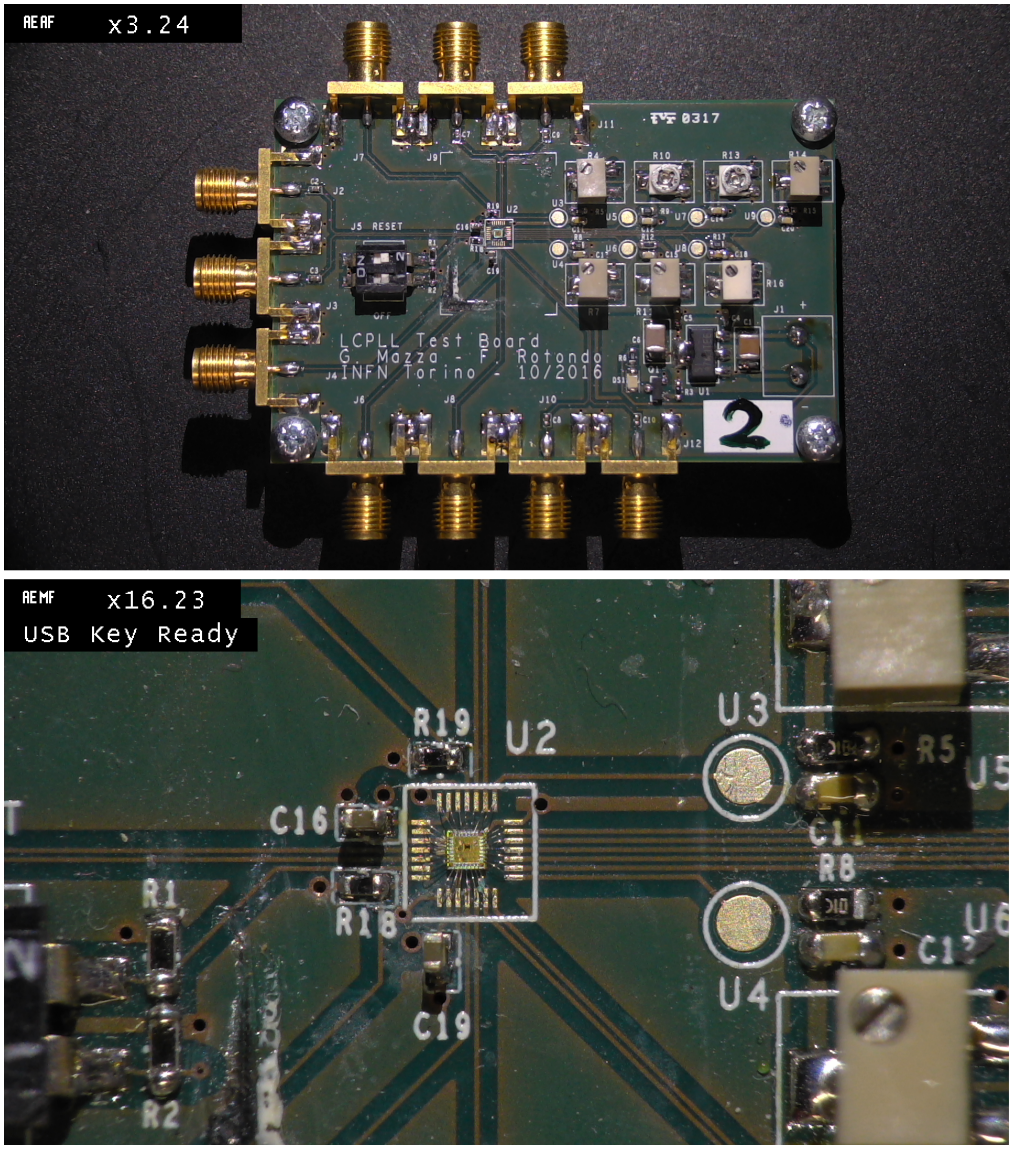


Figure 4.22: The PLL PCB board with a PLL on it

Period and TIE jitter measurements has been done, and the result plot is depicted in Fig. 4.26. Average values for both the outputs frequency are summarized in Table 4.3.

The jitter differences at $F_{VCO}/4$ and $F_{VCO}/32$ are not yet fully understood; a possible explanation is that the modulation of the VCO control voltage induced by the divider (which is synchronized with the VCO clock signal). Since the 160 MHz output it is averaged for a longer time during the measurements, it seems less sensitive to this modulation. Usually, typical jitter specification in serial links systems

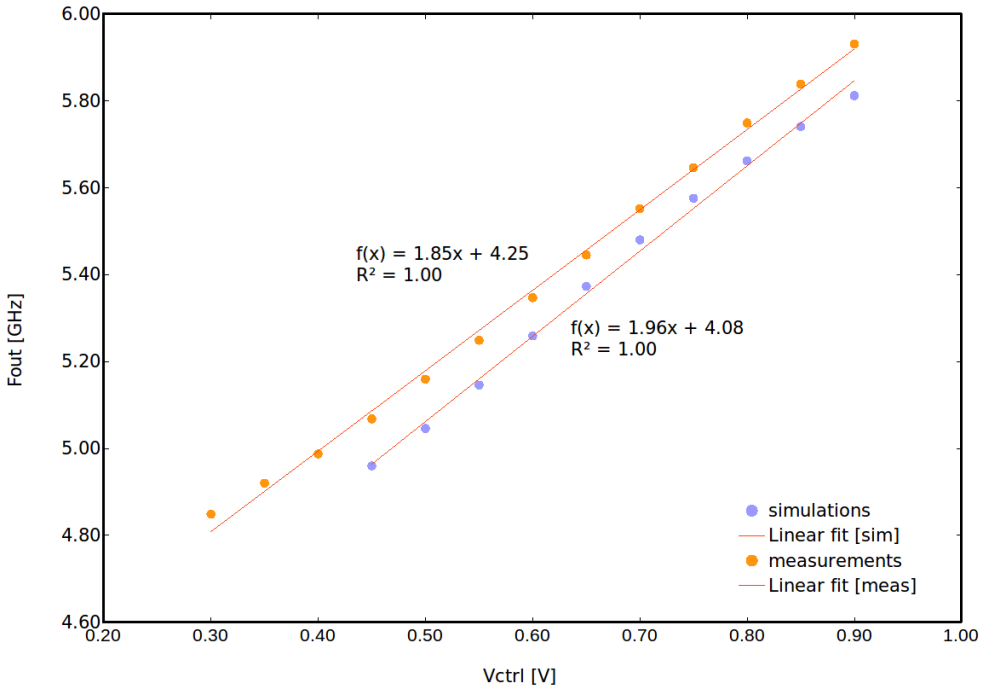


Figure 4.23: VCO transfer function: simulation vs measurement data.

with 10 Gb/s data rates are around 20% of the bit period (with a predominance of data dependent jitter), so jitter of few picoseconds are negligible.

4.5.3 N-cycle jitter performance

Some N-cycle jitter tests have been performed in order to study the behavior of the circuit by varying on the scope the N parameter for the N-cycle jitter measurement. The results shows a kind of periodic behavior, with minimum and maximum values in correspondence of multiples of two. This phenomenon could be explained by considering the noise effect on the frequency divider signal which is synchronous with the clock: this could show some minimum or maximum jitter values followed by a proportional increase/decrease of the N-cycle jitter.

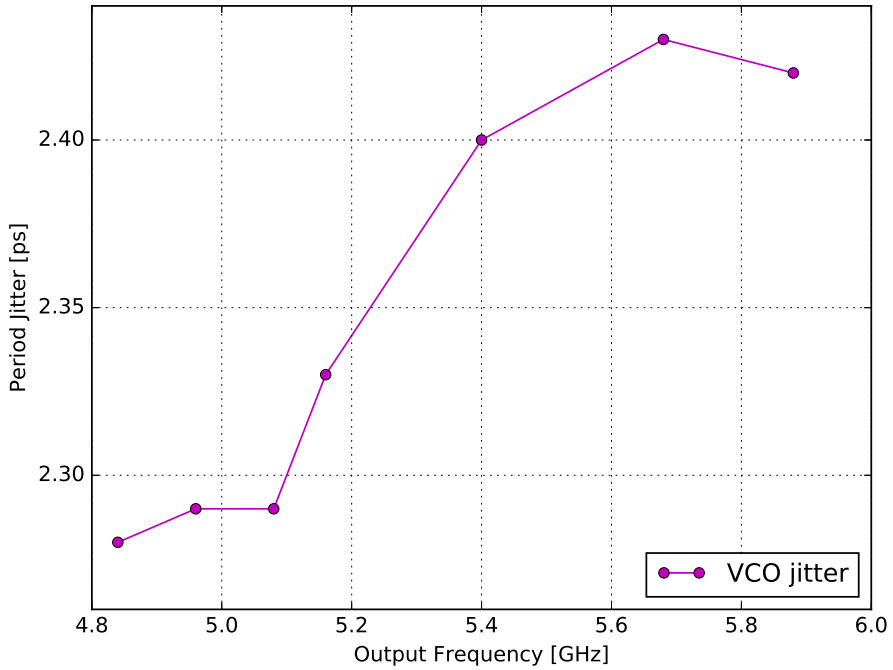


Figure 4.24: VCO period jitter.

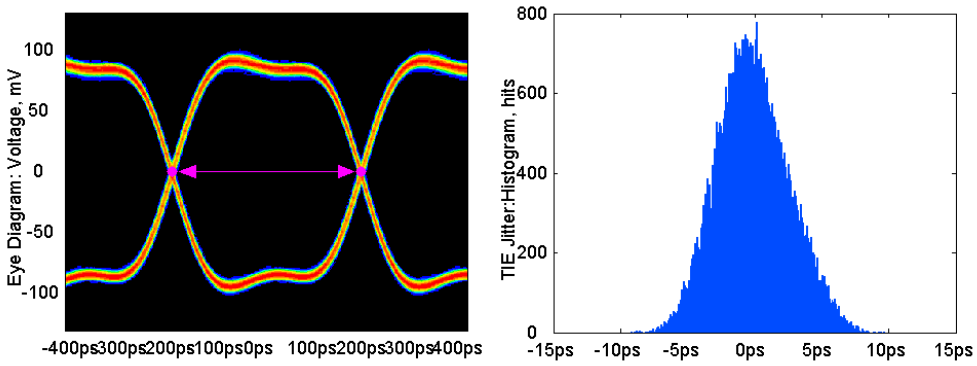


Figure 4.25: Eye diagram of the F_{VCO} output (1.28 GHz).

4.5.3.1 Total Ionizing Dose (TID) test results

The LC-PLL has been irradiated with X-rays in Padova (by mean of the X-ray facility located at the INFN Padova) with 10 keV up to a dose of 2.5 MGy (in SiO_2), with a dose rate of 35 Gy/s. Before the irradiation, tests with different length cable have been done: in this case, a jitter increase of a factor of 2 for longer cables has been

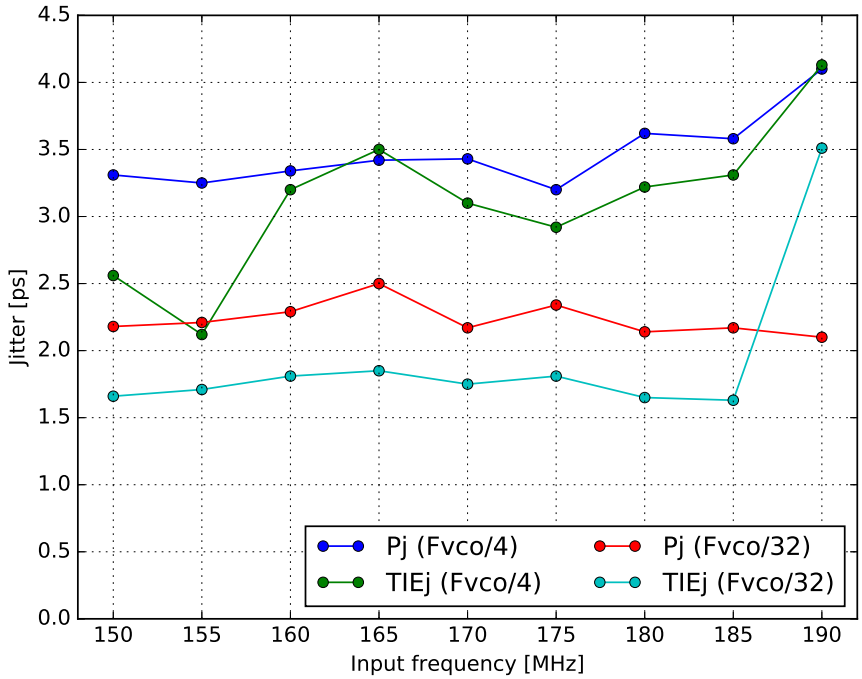


Figure 4.26: PLL jitter measurements.

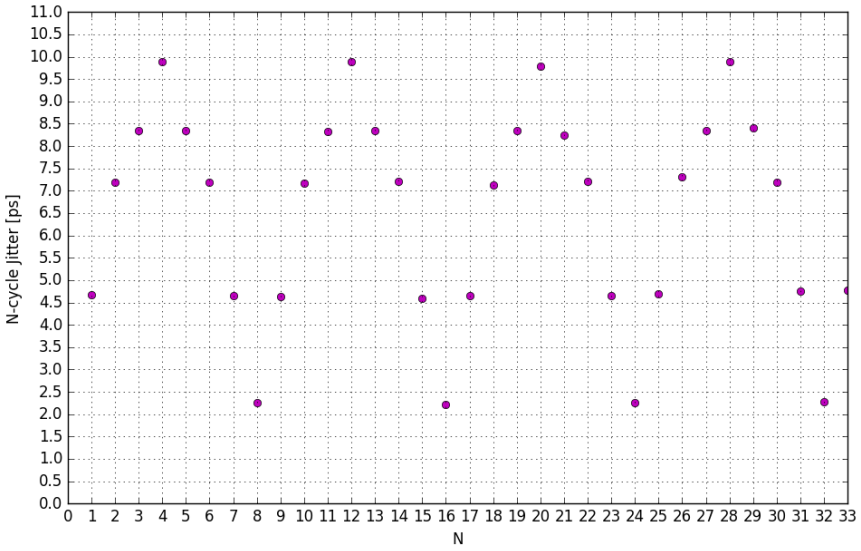


Figure 4.27: Peridicity of the N-cycle jitter vs N number.

noticed. During the irradiation the chip was continuously powered and fed with a 160 MHz clock signal and no changes have been observed; all the measurements have been taken during the switching-off of the beam. In Fig. 4.29(a) and 4.29(b) are respectively depicted period jitter and TIE jitter vs integrated dose measured on the $F_{VCO}/4$ output (corresponding to 1.28 GHz frequency). As it is possible to

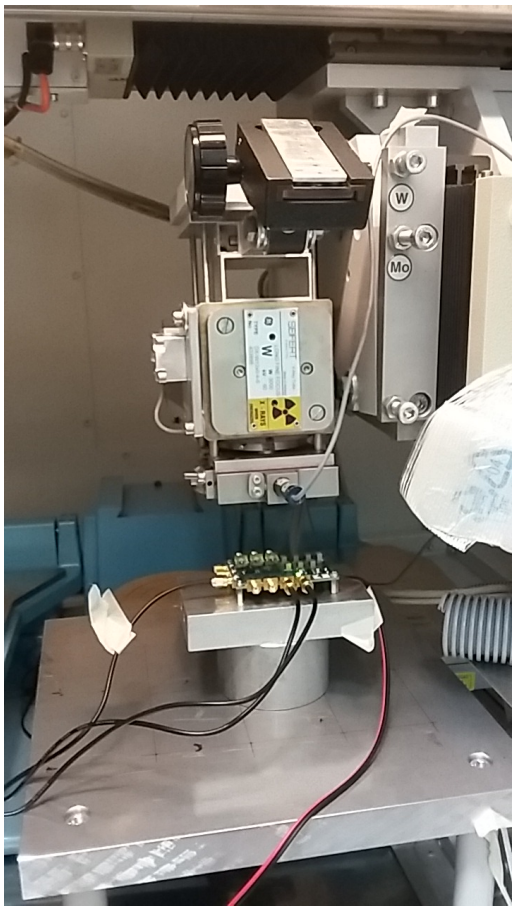
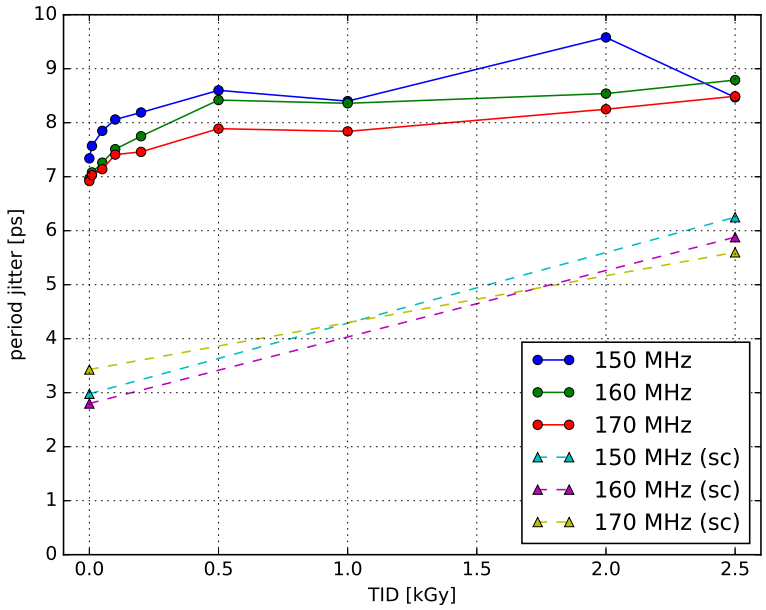
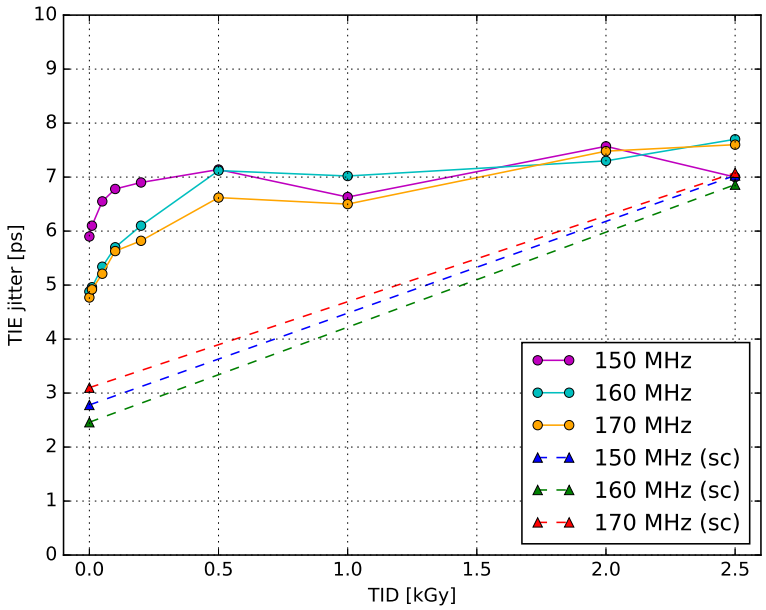


Figure 4.28: A picture of the X-ray facility at INFN Padova.

see, despite the PLL has continued to work properly up to 2.5 MGy, the irradiation deteriorate the jitter performance. However, jitter levels remain adequate for many applications in science. Furthermore, annealing measurements at room temperature have been performed. The PLL showed a kind of reverse annealing effect and it became stable in the first twenty-four hours. In other circuits fabricated in 65 nm technology has been already observed but it is not yet fully understood. In order to explain this phenomenon, some recent studies [103] hypothesize a radiation-induced damage in the spacer oxide and overlying silicon nitride layers above the LDD

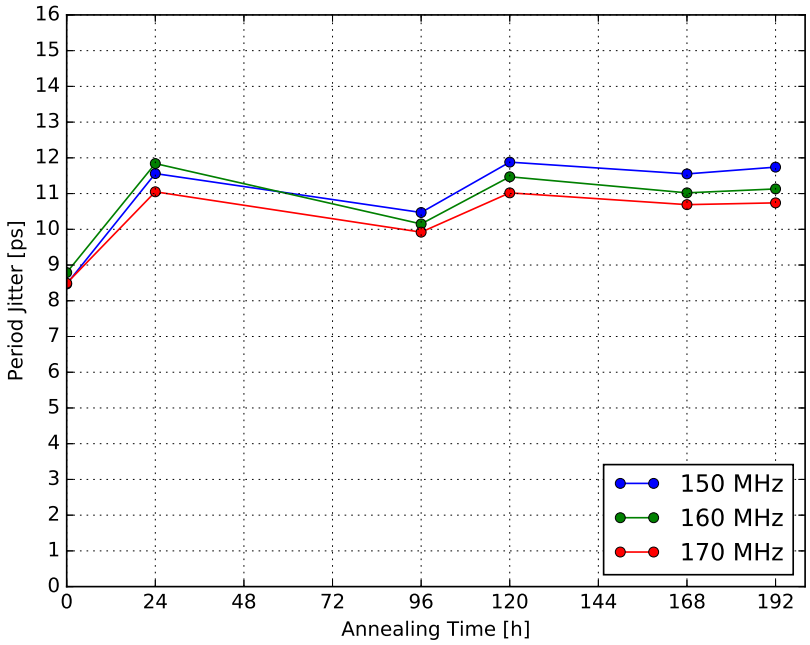


(a) Period jitter levels vs total dose. The test has been done with long table and short cable (”sc” in the legend).

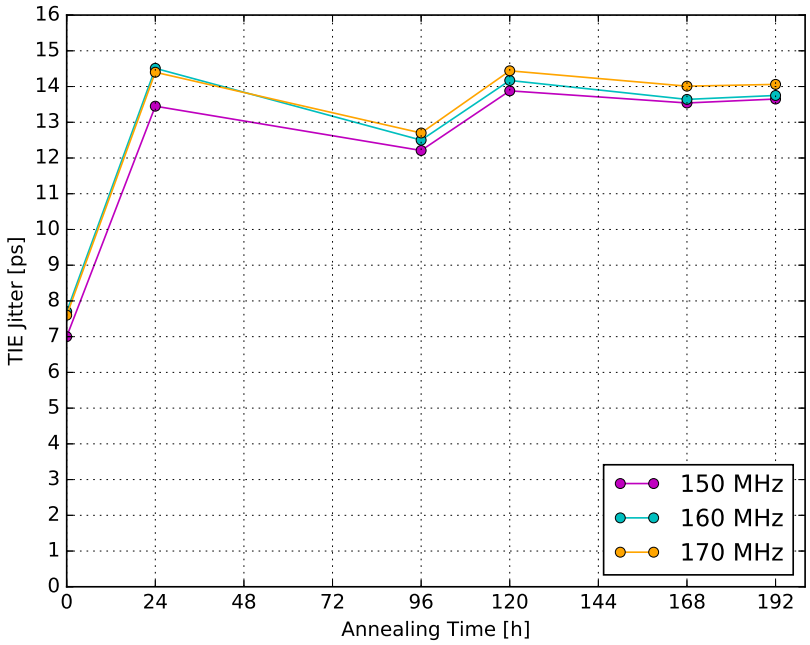


(b) TIE jitter levels vs total dose. The test has been done with long table and short cable (”sc” in the legend).

Figure 4.29: Jitter levels vs total ionizing dose.



(a) Annealing measurement: period jitter vs annealing time.



(b) Annealing measurement: TIE jitter vs annealing time.

Figure 4.30: Annealing measurements.

extensions. In those regions ionization can release hydrogen ions which could drift and consequently reach the gate-oxide interface; in this way the threshold voltages could show some variations.
However, in order to understand better the behavior of the circuit under radiation, some measurements in reset mode have been done. In Fig. 4.31 the results are shown, compared with the pre-irradiation values. Based on these last measurements, it is possible to affirm that the jitter increasing may be due to the LC-VCO degradation performance. In particular, since the CML frequency divider is designed using just

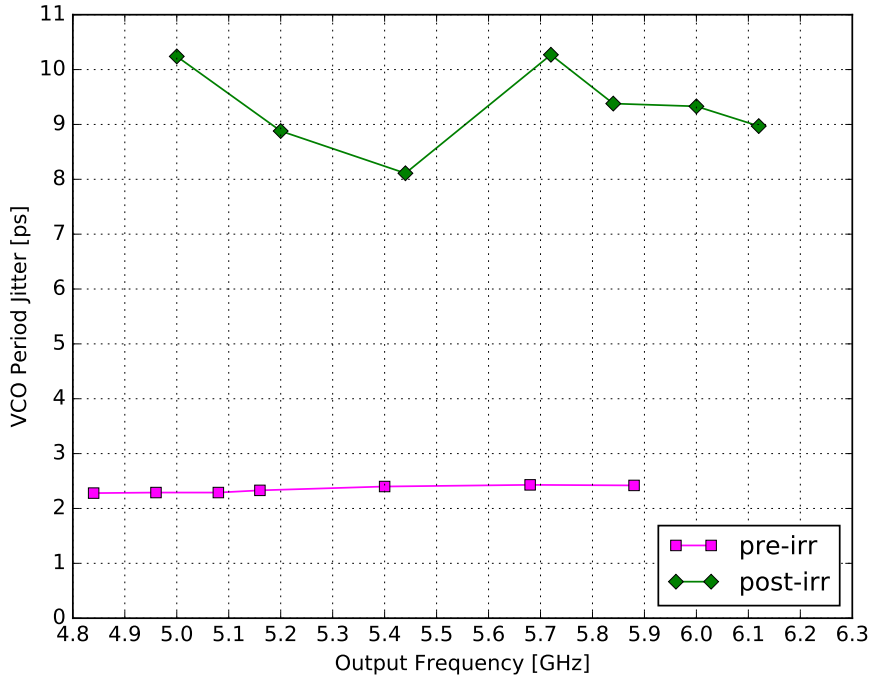


Figure 4.31: Pre and post irradiation periodic jitter measurements.

only nMOS transistors whereas the bias current mirror used for the oscillator is designed using pMOS transistor, and in [103] is demonstrated that nMOS transistor are generally less sensitive than pMOS, this increase may be due to the degradation of the bias circuit in Fig. 4.15. A possible solution for this issue may be the enlargement of the channel length (240 nm in this prototype version).

4.6 Conclusions

A LC-PLL clock multiplication PLL developed in a 65 nm CMOS commercial process has been designed and tested. With an input frequency range of 150-190 MHz, it is able to work by generating internally a VCO frequency which is 32 times the input one. Due to its low power consumption (18 mW) with a total area of 0.124 mm^2, it represents a good compromise for those area-critical ASIC integration environments which needs low power dissipation. Test measurements show jitter values below 4 ps during normal operations. After irratiation tests up to 2.5 MGy, the chip is still fully working and its jitter is adequate for the majority of applications as well.

Chapter 5

The MATISSE prototype

5.1 Background and motivation

MAPS are becoming increasingly attractive for the future generation of High Energy Physics expertiments as a novel technology for particle detector sensing devices.
In this context, several R&D projects are focused in the development of new architectures and technologies to increase their performance in terms of speed, radiation tolerance, signal-to-noise ratio.
Especially the versatility of the front-end electronics and its optimization is a crucial node in order to simplify and improve the integration of digital and analog electronics in the same pixel unit and the exploration of different silicon substrate configurations.
MATISSE (**M**onolithic **A**c**TI**ve pixel **S**en**S**or **E**lectronics) is a demonstrator chip developed inside SEED collaboration (*Sensor with Embedded Electronics Development*) which involves the Torino, Padova INFN groups, University of Trento and TIFPA and the collaboration with LFoundry.
The aim of this first prototype is to study a new topology of MAPS with the development of readout electronics for the caracterization of a sensor with a 30 μm or more depletion depth. Characteristics of versatility, scalability and adaptability for both polarities of implemented sensor ease the investigation to the compatibility between fully-depleted sensitive nodes and readout electronics integrated in the same silicon wafer.
The MATISSE ASIC has been developed in a 110 nm low power (1.2 V) CMOS

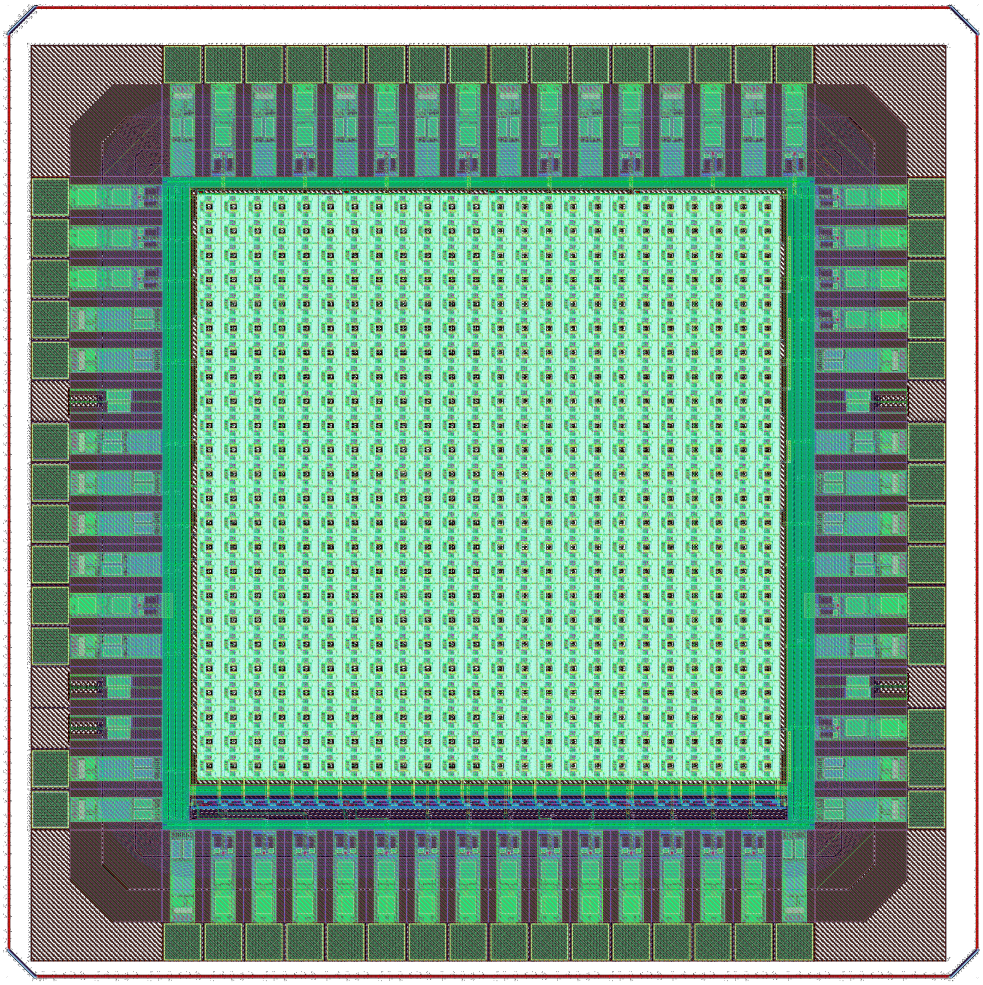


Figure 5.1: Layout of MATISSE.

process; the total die area covers 2×2 mm^2 while each pixel covers an area of 50×50 μm^2: 20×20 μm^2 are used for the implementation of the sensor, while the remaining area is dedicated for the in-pixel front end electronics.
Its architecture is based on two main blocks: the 24×24 pixel matrix organized in four independent 6×24 pixel sectors and the EoC (End Of Column) logic. Each sector shows a different sensor topology maintaining the same electronics as well. The readout electronics is based both on NMOS and PMOS transistors and includes both analog and digital parts, which are divided physically in two different power domain.
The in-pixel readout electronics is based on a CSA (Charge Sensitive Amplifier) with two local memories, two CMOS switches, four data transmission buffers and a

Parameter	**Value**
Technology	110 nm CMOS
Chip area	2×2 mm^2
Matrix area	24×24 pixels, 1200×1200 μm^2
Pixel area	50×50 μm^2
Sensor area	20×20 μm^2
Analog gain	$\approx$130 mV/fC (2.1 mV/100 e$^-$)
Power consumption (transmission)	$\approx$370 μW
Power consumption (waiting)	$\approx$6 μW
Sensor Capacitance	40 fF
Storage Capacitance	$\approx$70 fF (MIM CAPS)
Linearity Range	400 mV - 950 mV
Readout Speed	Up to 5 MHz
Other features	- Internal Test Pulse - Mask Mode - Baseline Regulator
Shutter type	Snapshot Shutter
Readout Type	Correlated Double Sampling

Table 5.1: MATISSE parameter summary.

feedback transistor for the reset operation.

It is based on a telescopic cascode amplifier with a feedback capacitor for the voltage gain conversion to 130 mV/fC. By mean of a DC coupling through a PMOS (to provide low power operations), the CSA stage is connected to the sensor: the CSA itself allows a quite good low sensitivity to the sensing node capacitance. MIM capacitors are used for memory units in order to optimize the pixel area. Each memory is equipped with a low power buffer instead source followers to avoid dynamic range limitations. To send analog data off chip, two additional buffers based on switched op-amps (able to maintain a reasonable dynamic range driving capacitive loads up to 10 pF) are implemented. In order to reduce injection of charge, the switches are based on CMOS gates allowing rail-to-rail operation range. The full charge is optimized for the maximization of the dynamic range (up to 550 mV) with low power dissipation (see Table 5.1). Three flip-flops are used for readout, baseline regulation and generation of test pulse or pixel masking. Additional test structures are made to inject additional noise into the substrate for testing purposes.

Readout is performed in a snapshot shutter fashion: integration time starts at the

same time for all the pixels in the array and it is short as 100 ns. The collected charge information is obtained from the difference between the baseline (at the beginning of the readout) and signal (at the end of the readout) values, which are stored in two dedicated memory slots and then sent off-chip. Each sector is equipped with two output pad for these values since the readout of each submatrix is independently managed by the EoC. Full matrix readout can be performed in less than 40 μs with a 5 MHz clock frequency and a 0.7 mV voltage drop. In order to subtract common baseline-signal offset and switching noise, the architecture supports a CDS (Correlated Double Sampling) [104].
The prototypes have been received in April 2017 and tests were carried on until first months of 2018.

5.2 Sensor development

5.2.1 State of the art

The actual state-of-the-art of the monolithic sensor development involves, on one hand, partially-depleted sensors, where the main mechanism for charge collection is represented by *diffusion* and, on the other hand, fully-depleted sensors, where the charge is collected by mean of *drift* (faster than diffusion). Partially-depleted

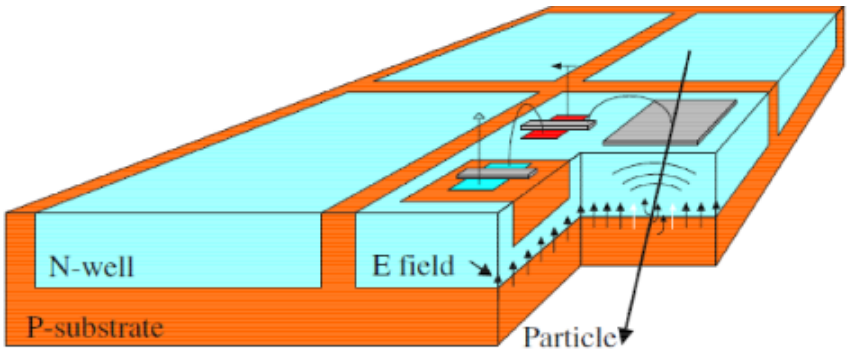


Figure 5.2: Cross section of a fully-depleted sensor (via [3]).

sensors are characterized by a low parasitic capacitance, which means low noise inside the system. However, charge collection by diffusion is pretty inefficient and slow, especially for radiation-damaged sensors. Furthermore, the charge collection

speed is strictly position-dependent, since it is function of the position of the incident particle. A partially-depleted sensor example can be the TowerJazz monolithic sensor used for the development of ALPIDE chip [105] (Fig.5.3. Fully-depleted sensors,

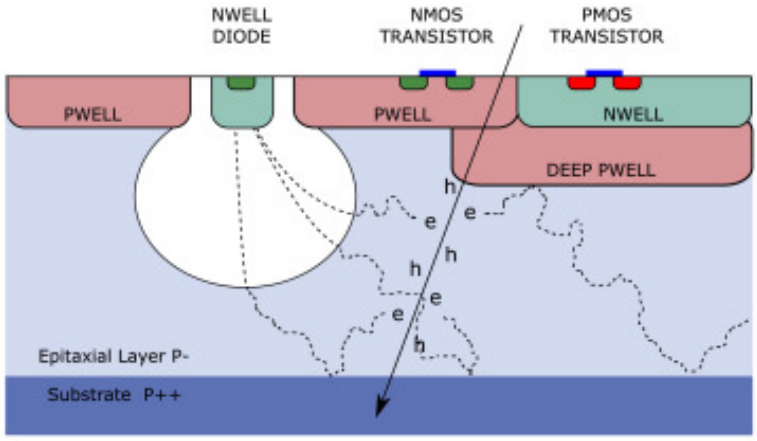


Figure 5.3: Section of a Tower Jazz 180 nm MAP sensor (image via [1]).

instead, show encouraging efficiency and speed traits but the actual set up establish they need a special well used as sensor cathode in which the readout electronics must be placed. Unavoidably, this region shows a considerable parasitic capacitance and, thus, noise. Recently, high-resistivity epitaxial layer sensor for imaging have been

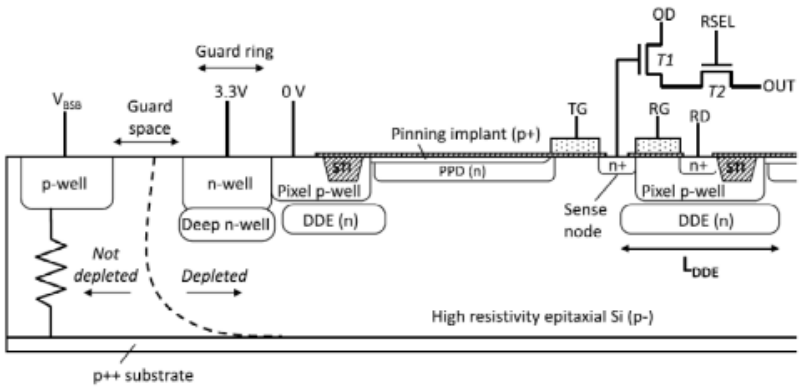


Figure 5.4: Cross section of an imaging sensor with a fully-depleted epitaxial layer (via [4]).

developed; in this kind of process, the epitaxial layer is completely depleted and thus they are characterized by an extremely high charge collection speed. The limitation is about the bias voltage which needs to be applied to the front-side of the sensor, this limiting the volume of the depleted zone.

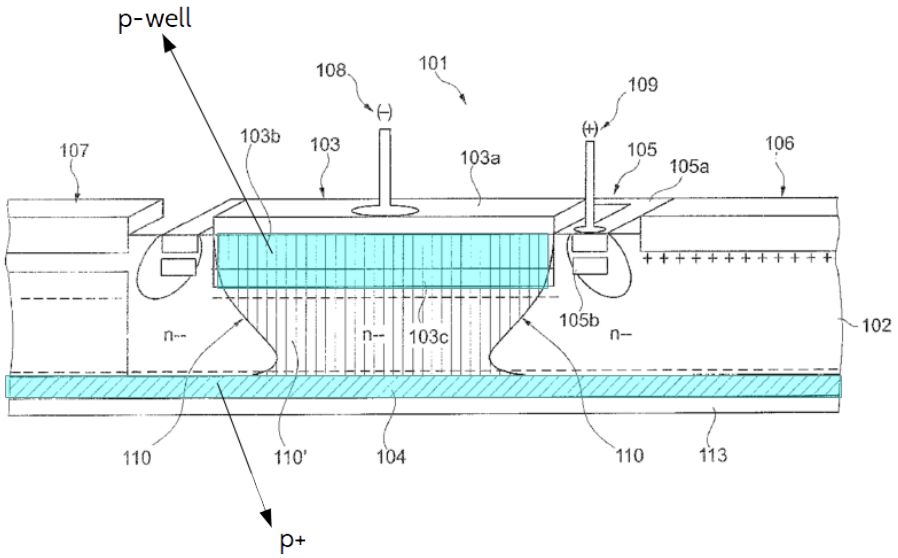


Figure 5.5: Cross-section of an optical sensor developed on a fully-depleted substrate, with a back-side and front-side pn-junction. In this picture, p-regions highlighting and labels are added for a better clarity with respect to the patent one [5].

In Figure 5.5 a similar approach, with a thicker ($\approx$50 μm) high-resistivity substrate, is described in a ESPROS photonics patent [5]. This particular device shows a n-tyoe substrate and p-type electrodes. The sensor has two junctions: one on the front-side and another one on the back-side to simplify the depletion of the substrate.
A particular case of back-side depleted sensors [6][106] differs from the previous typologies becaus of the active junction on the baskside and the electrodes doping, where the high-resistivity charge collection is of the same type of the substrate. Different pixels electrodes are the insolated between each others just only with the full sensor depletion, which is provided by inverse polarization of the baskside junction. This process allows the combination of a low parasitic electrodes capacitance with speed and charge collection efficiency, and it is suitable for pixel sensor for imaging applications (X, UV, visible and near-IR spectrum). An additional advantage is the possibility to use low-voltages for the front-side, which means low-voltage processes electronics. The back-side implant needs a double side processing: in the latest examples, the backside junction is pre-processed (which means that it is realized before the processing of the front-side electronics).
This technology shows an essential issue: the acceptable polarization voltages range is low-limited by the need to deplete completely the sensor in order to isolate the

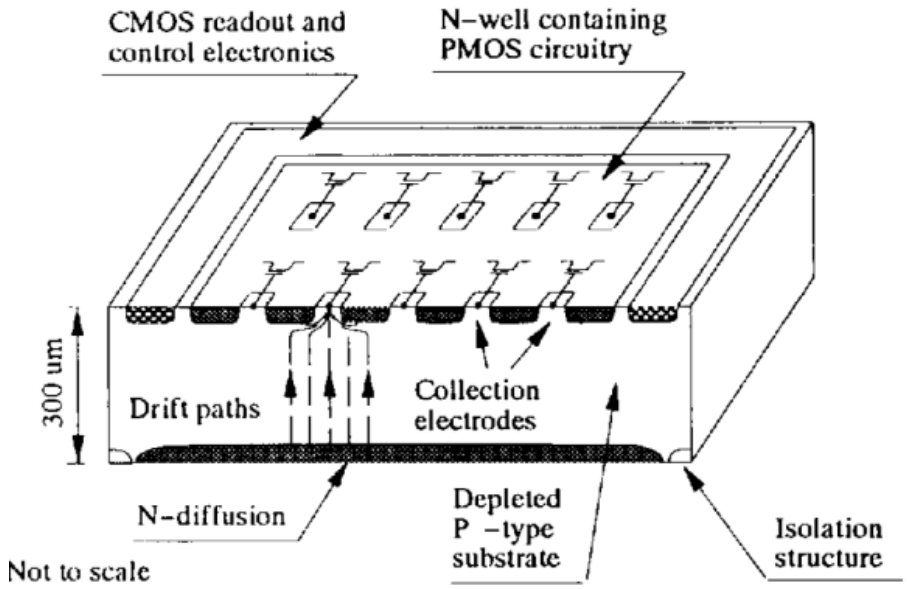


Figure 5.6: Cross-section of a fully-depleted monolithic sensor developed in a p-type substrate, with n-type electrodes and back-side junction (via [6]).

collecting electrodes and high-limited by the need to avoid the punch-through current between the backside electrode and the front-side well dedicated to the readout electronics. In order to obtain a good separation between the full-depletion voltage and the punch-through one it is necessary to apply a voltage high enough to the charge collection electrode; unluckly, this solution is not so compatible with deep-submicron processes.

5.2.2 The MATISSE sensor

For the MATISSE chip, sensors have been developed in a n-type high-resistivity substrates with a thickness of 300 μm. While the front-side wafer has been fabricated with a conventional 110 nm CMOS process electronic flow with six metal layers and 1.2 V transistors, the p-n junction on the backside has been created with a p+ implantation. The double side processing involved the development of sensors but, however, the front-side flow has been fully compatible with the standard CMOS process. The in-pixel sensing electrodes for radiation charge collection has been formed with a n-well implantation. Between different sensing nodes some resistive paths are present when the sensor is not yet depleted. In order to perform the

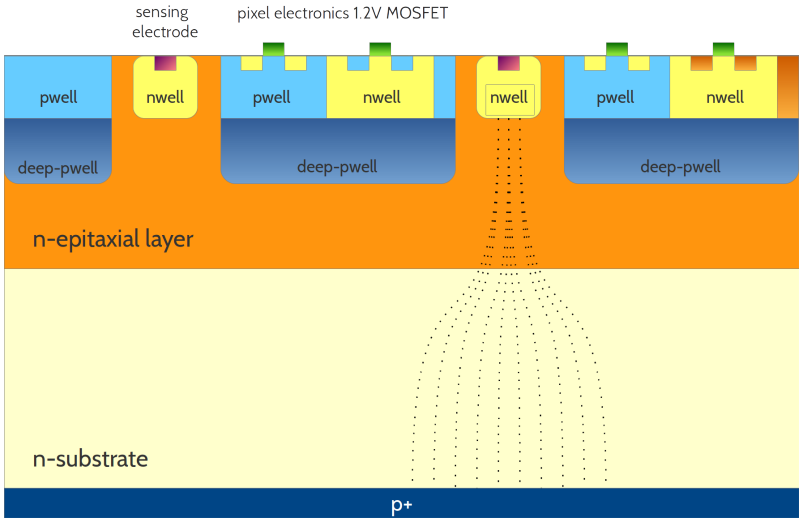


Figure 5.7: Cross section of the monolithic double-sided processed sensor of MATISSE.

electrical isolation between n-wells, the substrate needs to be fully depleted by using an inverse polarization voltage from the backside junction [106] [6]. The front end electronics is located inside n-wells and p-wells on the front-side part of the sensor. The n-wells are isolated by deep n-wells from the bulk in order to avoide competition between charge collection diodes. In order to prevent the punch-through current between the backside p+ zone and the deep p-well frontsize region the sensor is fully depleted, a superficial region with an higher doping concentration formed on a n-type epitaxial layer has been created. In such a way low bias voltage can be applied to the front-side and sensing nodes can be DC connected to the readout electronics. Inside the substrate, charges may move by drift, allowing high speed collection. The sensor cross section and a qualitative scheme of the electric field inside sensor is shown schematically in Figure 5.7.

5.3 Front End Electronics

5.3.1 Pinout description

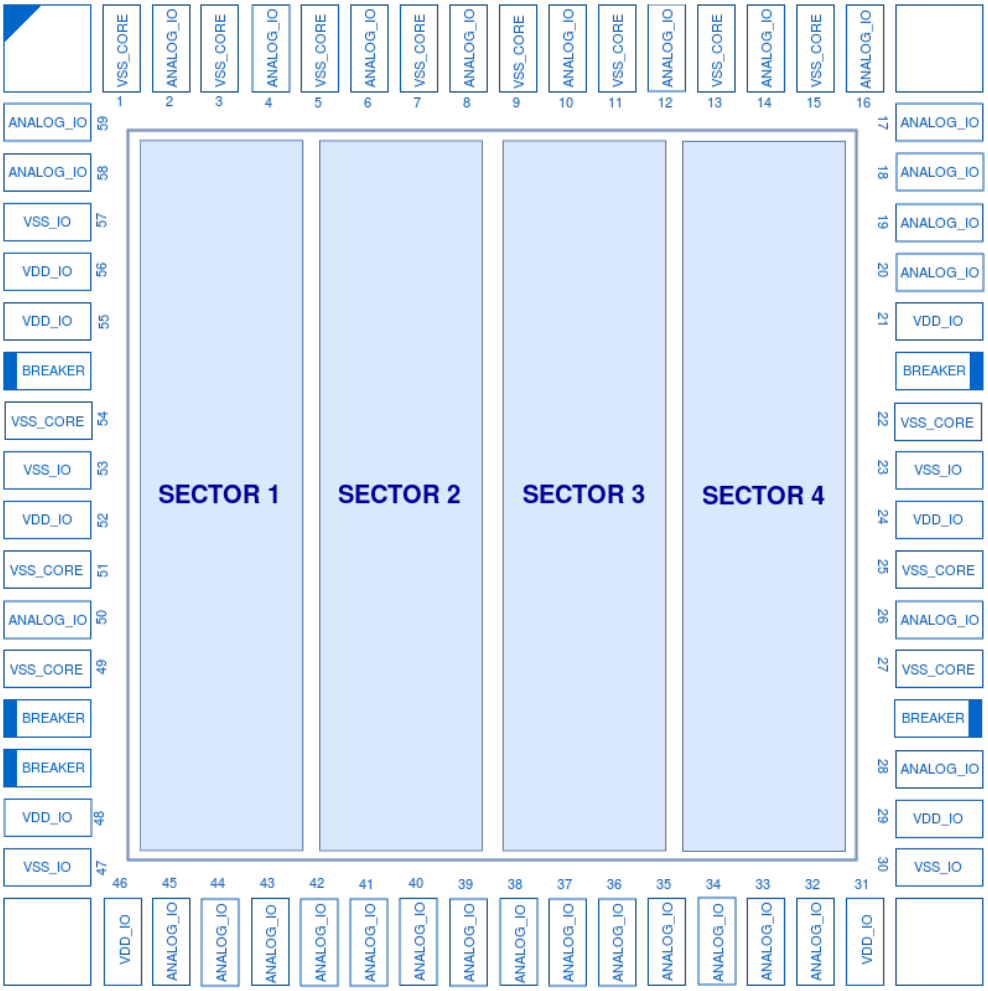


Figure 5.8: Pinout of MATISSE.

In Figure 5.8 the pinout scheme of MATISSE is depicted. It is constituted by 59 pads for these following purposes:

- 7 pads dedicated to the bias (4 voltages and 3 currents);
- 14 digital control pad (on the bottom side);
- 29 pads dedicated to the voltage supply (VDDs and VSSs);

- 8 pads used for to the analog outputs: they are located on the top side od the ring;
- 1 pad for the unique digital output;

The 8 analog outputs are used to provide the charge collected by the pixels diodes. Given the importance of this information, from the point of view of the design some effort has been done in order to remove noisy influences from the digital logic parts: for this reason, all the digital inputs and outputs are circumscribed in a single block separated from the analog domain with some ”breaker” blocks.
In the analog domain as well, some essential parts of the front end (the preamplifier) have been separated from the remaining electronics: the upper left and right breakers are utilized to implement this split. Because of these breakers, the pinout appears divided in four blocks. For each block all the protection diodes need to be polarized; in order to perform a proper polarization, VDD and VSS pads are inserted (VSS IO/CORE, VDD IO/CORE). Tables 5.2, 5.3, 5.4 and 5.5 lists all the pinout pins name with the correspondent typology.

5.3.2 Pixel matrix

The pixel array is composed by 24×24 pixels and it is divided in four sectors composed by 6 columns of 24 pixels.
The difference between sectors consists into the geometry of the sensors implemented in its pixels: for this reason, this feature allows the test of the behavior of eight different diode typologies with the same front-end electronics. Figure 5.9 shows all the typologies of diodes implemented. All the sectors share the bias voltages, the voltage supplies and all the readout signals dispatched through the digital inputs. Bias currents, however, are managed differently because the signal sent through the dedicated pad is distributed to all pads: in such a way, each pad grabs a quarter of the total amount.

The pixel area is the fundamental unit of the matrix and its area comprehends both the sensor and the readout electronics. It occupies an area of 50×50 μm^2 while the sensor area covers 20×20 μm^2 in the middle of the pixel (16% of the total area). The remaining area is occupied by the circuitry which is nearly totally analog and based on a snapshot shutter readout [104].

Top				
N	**Pin name**	**Type of pad**	**Purpose**	**Comments**
1	gnd_1	VSS CORE	GROUND	Ground.
2	outBsln_1	ANALOG I/O	ANALOG OUTPUT	Output for the baseline for the sector 1.
3	gnd_2	VSS CORE	GROUND	Ground.
4	outSignal_1	ANALOG I/O	ANALOG OUTPUT	Output for the signal for the sector 1.
5	gnd_3	VSS CORE	GROUND	Ground.
6	outBsln_2	ANALOG I/O	ANALOG OUTPUT	Output for the baseline for the sector 2.
7	gnd_4	VSS CORE	GROUND	Ground.
8	outSignal_2	ANALOG I/O	ANALOG OUTPUT	Output for the signal for the sector 2.
9	gnd_5	VSS CORE	GROUND	Ground.
10	outBsln_3	ANALOG I/O	ANALOG OUTPUT	Output for the baseline for the sector 3.
11	gnd_6	VSS CORE	GROUND	Ground.
12	outSignal_3	ANALOG I/O	ANALOG OUTPUT	Output for the signal for the sector 3.
13	gnd_7	VSS CORE	GROUND	Ground.
14	outBsln_4	ANALOG I/O	ANALOG OUTPUT	Output for the baseline for the sector 4.
15	gnd_8	VSS CORE	GROUND	Ground.
16	outSignal_4	ANALOG I/O	ANALOG OUTPUT	Output for the signal for the sector 4.

Table 5.2: Top side pads.

Right				
N	**Pin name**	**Type of pad**	**Purpose**	**Comments**
17	VBsln_regulator	ANALOG I/O	ANALOG INPUT	Voltage to set the baseline.
18	VTP	ANALOG I/O	ANALOG INPUT	This sets the amplitude of the test pulse.
19	pCas	ANALOG I/O	ANALOG INPUT	Bias for cascode p-type.
20	nCas	ANALOG I/O	ANALOG INPUT	Bias for cascode n-type.
21	vdd_buff_1_b	VDD I/O	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the buffer 1.
-	BREAKER	BREAKER	BREAKER	Breaker.
22	vdd_buff_2_b	VDD CORE	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the buffer 2.
23	gnd_9	VSS I/O	GROUND	Ground.
24	vdd_preamp_b	VDD I/O	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the preamplifier.
25	gnd_10	VSS CORE	GROUND	Ground.
26	vdd_grdr_b	ANALOG I/O	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the guardring.
27	gnd_11	VSS CORE	GROUND	Ground.
-	BREAKER	BREAKER	BREAKER	Breaker.
28	prg_bit_out	ANALOG I/O	DIGITAL OUTPUT	Programming bit output.
29	vdd_dig	VDD I/O	VOLTAGE SUPPLY (1.2 V)	Voltage supply for digital logic parts.
30	gnd_eoc	VSS I/O	GROUND	Ground.

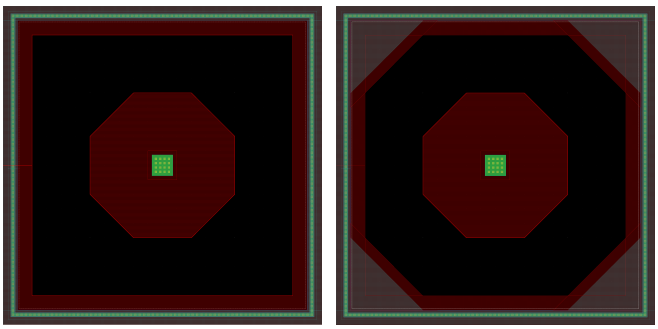
Table 5.3: Right side pads.

Bottom				
N	**Pin name**	**Type of pad**	**Purpose**	**Comments**
31	gnd_eoc_2	VSS I/O	GROUND	Ground.
32	TP	ANALOG I/O	DIGITAL INPUT	Test pulse for the input signal.
33	Bsln_regulator_ctrl	ANALOG I/O	DIGITAL INPUT	Control signal for the baseline.
34	SampleSignal	ANALOG I/O	DIGITAL INPUT	Sampling signals for the input signal.
35	SampleBsln	ANALOG I/O	DIGITAL INPUT	Sampling signals for the baseline.
36	ResetRead	ANALOG I/O	DIGITAL INPUT	Bit to force to zero all the read flip flops (active low).
37	ResetPrg	ANALOG I/O	DIGITALINPUT	Bit to force the TP and mask register (active low).
38	feReset	ANALOG I/O	DIGITALINPUT	Front-end reset (active low).
39	DiodeReset	ANALOG I/O	DIGITALINPUT	Initialization chip bit (connect the diode to VDD).
40	Digital_in	ANALOG I/O	DIGITALINPUT	Digital input for the digital noise stage; if not used, connect it to the ground.
41	v_read_clk	ANALOG I/O	DIGITAL INPUT	Vertical readout clock signal.
42	h_read_clk	ANALOG I/O	DIGITAL INPUT	Horizontal readout clock signal.
43	v_prg_clk	ANALOG I/O	DIGITAL INPUT	Vertical programming clock signal.
44	h_prg_clk	ANALOG I/O	DIGITAL INPUT	Horizontal programming clock signal.
45	prg_bit_in	ANALOG I/O	DIGITAL INPUT	Digital input programming bit.
46	vdd_dig_2	VDD I/O	VOLTAGESUPPLY (1.2 V)	Voltage supply for the digital logic parts.

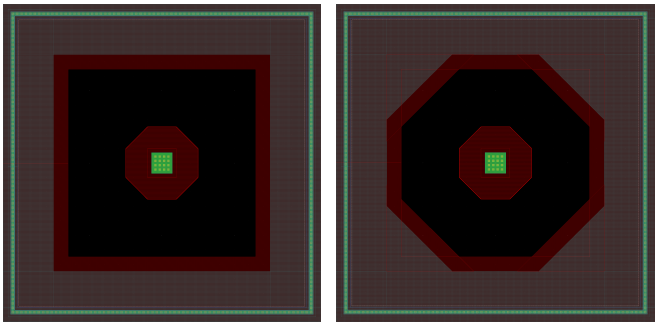
Table 5.4: Bottom side pads.

Left				
N	**Pin name**	**Type of pad**	**Purpose**	**Comments**
47	gnd_eoc_3	VSS I/O	GROUND	Ground.
48	vdd_dig_3	VDD I/O	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the digital logic parts.
-	BREAKER	BREAKER	BREAKER	Breaker.
-	BREAKER	BREAKER	BREAKER	Breaker.
49	gnd_12	VSS CORE	GROUND	Ground.
50	vdd_grdr	ANALOG I/O	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the inner guardring (NWELL).
51	gnd_13	VSS CORE	GROUND	Ground.
52	vdd_preamp	VDD I/O	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the preamplifier.
53	gnd_14	VSS I/O	GROUND	Ground.
54	vdd_buff_2	VDD CORE	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the buffer 2.
-	BREAKER	BREAKER	BREAKER	Breaker.
55	vdd_buff_1	VDD I/O	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the buffer 1.
56	gnd_grdr	VSS I/O	GROUND	Ground.
57	biasPreamp	ANALOG I/O	ANALOG INPUT	Bias for the preamplifier.
58	biasBuffer2	ANALOG I/O	ANALOG INPUT	Bias for the buffer 2.
59	biasBuffer1	ANALOG I/O	ANALOG INPUT	Bias for the buffer 1.

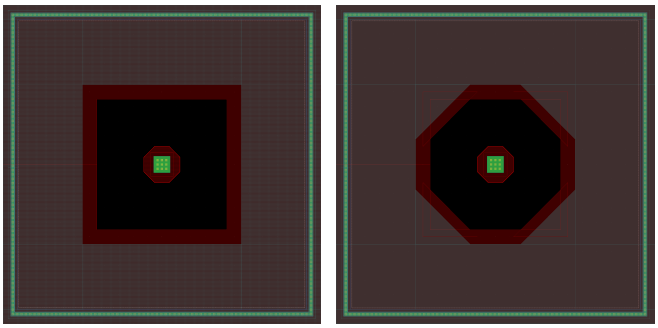
Table 5.5: Left side pads.



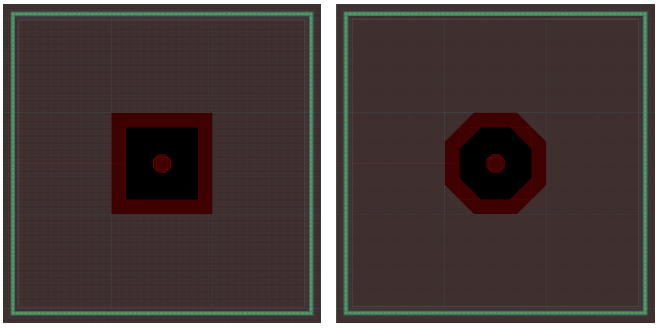
(a) #1 Diode sector. (b) #2 Diode sector.



(c) #3 Diode sector. (d) #4 Diode sector.



(e) #5 Diode sector. (f) #6 Diode sector.



(g) #7 Diode sector. (h) #8 Diode sector.

Figure 5.9: Diode sectors' different sizes and shapes.

The readout chain is made up of a preamplifier, a capacitor C_p implemented for the baseline output change and for the test pulse injection, two capacitors $C_{baseline}$ and C_{signal} for, respectively, baseline and signal storing, some switches CMOS and four buffers to drive the data bus. The readout scheme is shown in Figure 5.11.
Some digital blocks are dedicated for the control tasks at the pixel level: this circuitry occupies an area of 15×50 μm^2 and consists of three flip-flops and some digital buffers used to regenerate the signals propagated through the column.

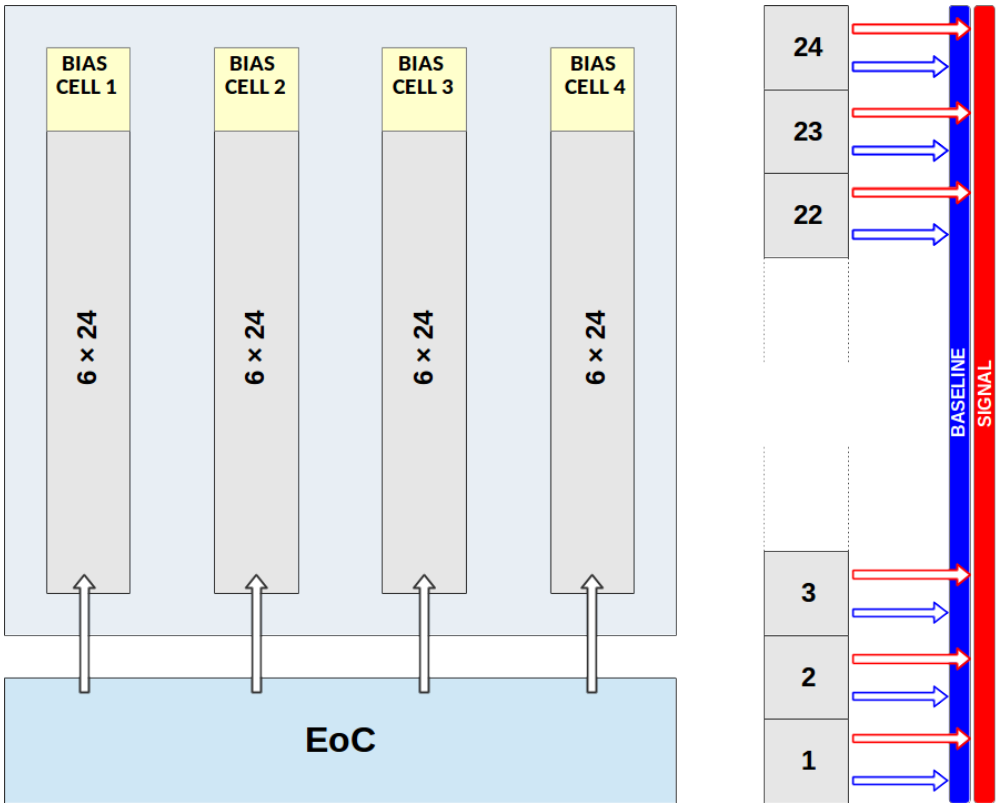


Figure 5.10: Readout of MATISSE.

The three flip-flops have different roles:

1. *Read flip-flop*: it is used for the management of the single channel connection to the output data bus. All these flip-flops of a single column are connected together and form a 24-bits register utilized fot the sequential connection of all the 24 pixels to the data bus during the readout operations. This process is timed by a clock signal (*v_read_clk*) distributed to all the columns by the end of column circuitry.

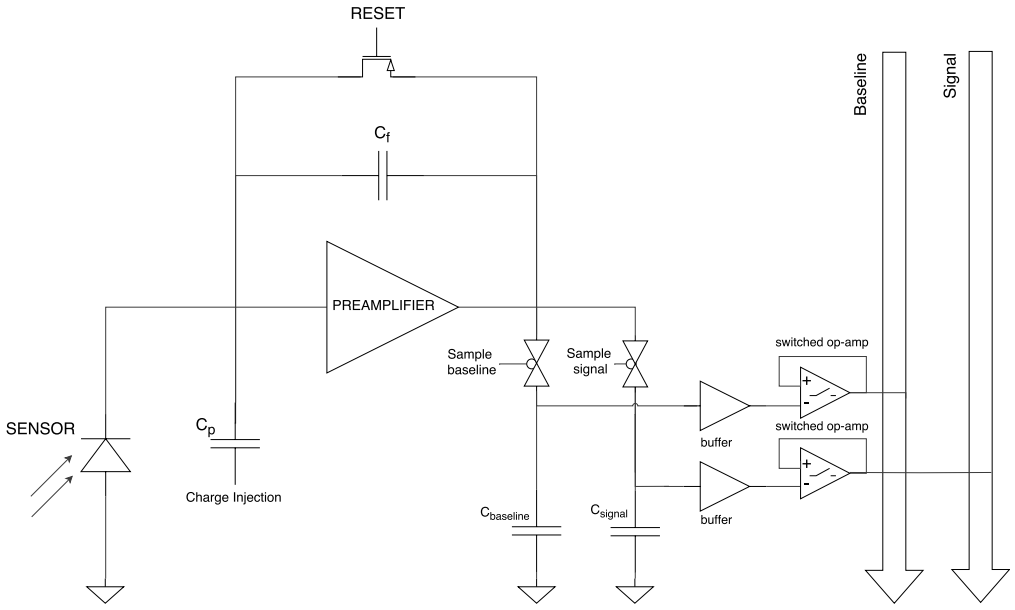


Figure 5.11: MATISSE front-end electronics schematic.

2. *TP flip-flop*: it is used for the test-pulse readout mode. By default the operation is disabled and this bit is set to zero while, when it is set to 1, it is possible to generate internally a pulse with electronics testing purposes. To perform this operation, the TP input needs to be used; the amplitude of the generated signal depends on the C_p (5.8 fF) and the VTP signal.

3. *MASK flip-flop*: it is used to switch of a particular pixel. Default mode forces all the pixels on: mask mode is performed when this bit is equal to 0 (otherwise is set to 1).

Due to the TP and MASK flip-flops features, the matrix readout may be performed in two different ways:

- *Normal mode*: the signal generated inside the diodes are processed by the circuitry. This can be done by setting the proper flip-flops value or by mean of resetting the configuration with the ResetPrg signal on Pad 37.

- *Test Pulse mode*: in this mode some internal pulses may be generated into the channels setting the TP flipflop of the choosen pixel to 1 . These signals' amplitude depends on the VTP value and on C_p capacitor.

Masking of one or more pixel can be applied in both modes by selecting 0 value for

the MASK flip-flops. Table 5.6 summarizes setting values fot these modes.

FF	Nomal Mode	Mask Mode	Test Pulse Mode
Test Pulse	0	X	1
Mask	1	0	1

Table 5.6: Readout modes.

5.3.3 End of Column

Inside the End of Column (EoC) all the logic necessary for performing readout, programming and managing of all the pixels' information is contained. The circuitry is composed by some digital blocks arranged at the bottom of the pixel array and separated by the matrix by a guard-ring.

5.3.4 Readout management signals and timing

The matrix has been divided in 4 sectors composed by 6 columns $\times$ 24 pixels for readout purposes. At the bottom of each column a shift register is designated to address the columns. Each sector is equipped with two analog output lines so the four sector may be read in a parallel mode; furthermore, a dedicated 6-bits shift register is implemented for the column selection in each sector. For this reason, a 5 MHz clock is enough for a complete readout in $\approx$30 μs. Three signals are used to perform the readout.

- ResetRead (pad 36): active low signal. It allows resetting the read flipflop inside the pixel array and the flip-flops in the column addressing shift register;
- v_read_clk (pad 41): it is sent by each column to its pixels; it propagates "vertically".
- h_read_clk (pad 42): it manages and controls the column addressing shift register and points from a column to the next one; it propagates "horizontally";

Horizontal and vertical clock for the sake of simplicity are fed independently to the array; v_read_clk frequency is twenty-four times h_read_clk frequency.
ResetRead signal needs to be set everytime a new readout cycle must start:

- ResetRead=0: reset active → readout disabled, in-pixel 24 flip-flops are reset.
- ResetRead=1: reset no more active → readout enabled, propagation of the signal read_enable into in-pixel flip-flops; readout is performed by reading a pixel each cycle of vertical clock and, once a column is completely read, the horizontal clock is asked to point to the next column and the operation is thus repeated for all the 24 columns. Once the matrix is fully read, ResetRead is again put to 0.

Signal	**Value**			**Description**
	min	**typ**	**max**	
v_read_clk	1	5	7	clock of the vertical shift register to sequentially select the pixel to be read inside a column
h_read_clk	1	≤ 0.2	0.3	clock of the horizontal shift register to sequentially select the column for readout
v_prg_clk	1	≤ 20	≤ 40	vertical clock used to program the pixel matrix
h_prg_clk	1	500	1000	horizontal clock used to program the pixel matrix

Table 5.7: Digital clock values.

For a frequency value of 5 MHz for the v_read_clk clock signal (as a target frequency, see Table 5.7), the readout timing can be evaluated as described in Table 5.8:

Parameter	**Operations**
vertical clock frequency	$f_{v\_read\_clk} = 5$ MHz $\rightarrow T_v = 200$ ns
horizontal clock frequency	$f_{h\_read\_clk}$ $f_{v\_read\_clk}/24$ 208 kHz $\rightarrow T_h = 4.8\ \mu$s
reading an entire column	$t_{column} = 24$ pixel $\times T_v = 4.8\ \mu$s
reading the entire matrix	$t_{matrix} = 6$ column $\times t_{column} = 28.8\mu$s

Table 5.8: Evaluation for timing for readout.

5.3.5 Programming

Each pixel is equipped with two programming bits:

- one for test pulse (TP) activation;

- the other one for the pixel masking (MASK).

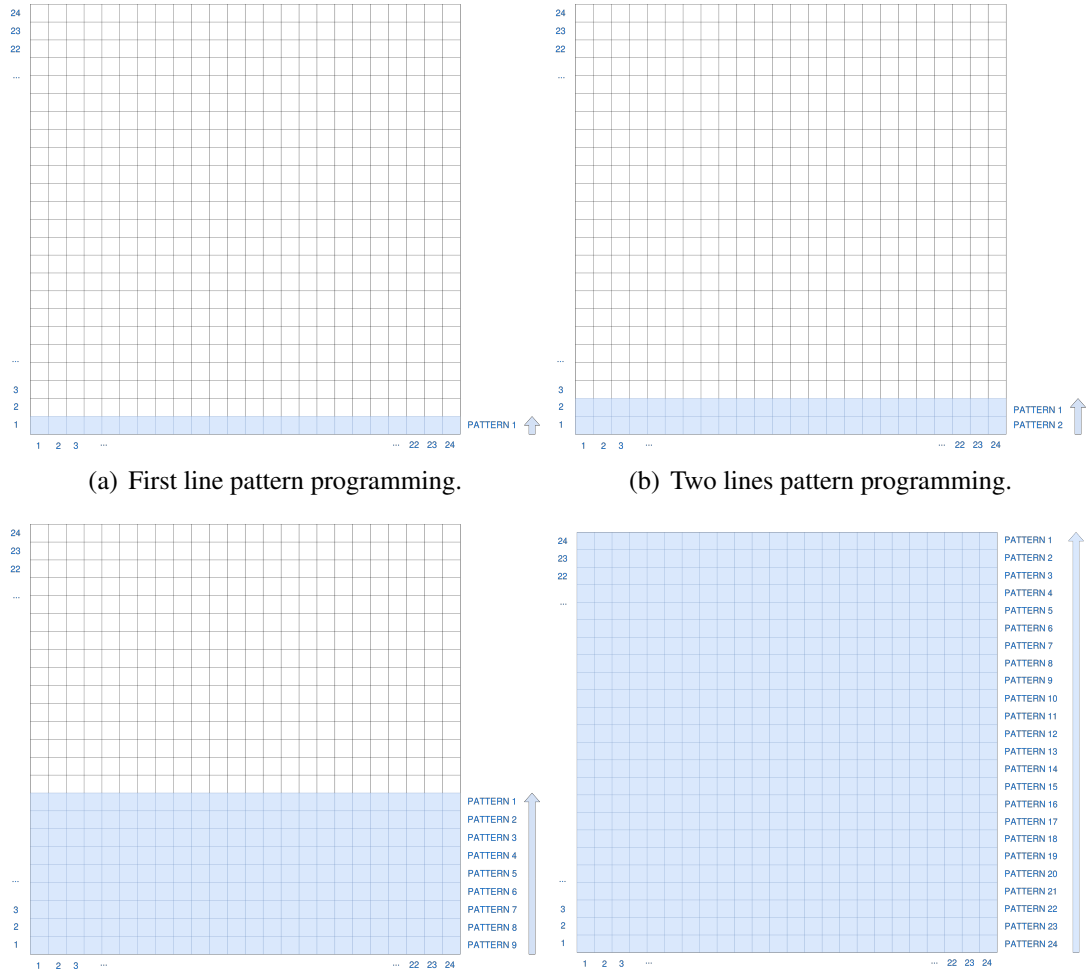
Masking pixels means keeping some pixel reset during the acquisition: this is a useful feature when some pixels appear faulty and the test may be impaired by their noise). To perform the masking feature:

- the input of the preamplifier must be connected to VDD: in this way its output is essentially put to zero;
- feReset signal must not be selected to avoid possible swings in the preamplifier output voltage;
- readEnable signal must not to be selected for power consumption reasons (because the two output buffers do not need to be turned on).

5.3.5.1 Procedure

The dedicated EoC programming shift register (EoC prgSR) manages the entire programming procedure. It consists of 48 flip-flops; each column uses two cells to store the TP and the MASK bit. Five signals are utilized to perform the programming procedure:

- ResetPrg (pad 37): used to reset the in-pixel programming flip-flops and the flip-flops in the column programming shift register;
- prg_bit_in (pad 45): used as the first incoming bit into the input of the column programming shift register;
- h_prg_clk (pad 42): used to manage the column programming shift register by ”moving” the programming bits along the register’s cells;
- v_prg_clk (pad 43): used to manage the shifting of a 48-bit (test pulse and mask value times 24 pixels) pattern among the matrix line; its frequency is worth 1/48 the h_prg_clk one (for the sake of simplicity, both v_prg_clk and h_prg_clk are fed separately);
- prg_bit_out (pad 28): it is the unique digital output of the entire architecture. It is the programming bit coming out of the column programming shift register.



(a) First line pattern programming.

(b) Two lines pattern programming.

(c) Nine lines pattern programming.

(d) Full matrix programming.

Figure 5.12: Matrix programming sequence.

To enable or disable the programming procedure, the ResetPrg (active low) signal is used; for this reason, this bit must be kept equal to 1 during the programming procedure. When it is set to 0 the programming bits are set to the default value (MASK=1, TP=0); this default configuration can be run when neither masking nor test pulse are needed.
The programming cycle can be outlined as follows:

1. loading of a 48 bits pattern in the horizontal programming column shift register by using prg_bit_in (for the configuration of the input bit) and h_prg_clk (horizontal programming clock)

2. once the pattern is loaded, all the bits are shifted vertically among the column covering the first row. To do that, v_prg_clk signal is used;

3. now a second 48 bits pattern can be loaded into the shift register (see point 1);

4. again, as the content of the first row is shifted to the second line, the second pattern is shifted vertically in order to cover the first row.

5. this operation must be iterated as the full matrix is completely loaded.

6. in such a way, row 1 is programmed with the last 48-bit pattern loaded inside the EoC prgSR, while row 24 is loaded with the first pattern loaded (Figure 5.12).

7. in order to do a further check on loaded patterns, when a 48-bit pattern is loaded, the old pattern is sent to prg_bit_out output port.

For a frequency value of 500 MHz for the v_prg_clk clock signal (as a target frequency), the programming timing can be evaluated as described in Table 5.9:

Parameter	Operations
horizontal clock frequency	$f_{v\_prg\_clk}$ = 500 MHz $\rightarrow$ T_h = 2 ns
vertical clock frequency	$f_{h\_prg\_clk}$ $f_{v\_read\_clk}$/48 $\approx$ 10 KHz $\rightarrow$ T_v $\approx$100 ns
programming an entire row	t_{row} = 48 bits $\times$ T_h = 96 ns
programming the entire matrix	t_{matrix} = 24 rows $\times$ t_{row} = 2.3 μs

Table 5.9: Evaluation of timing for programming.

5.3.6 Voltage supply and analog bias

MATISSE has been developed in a 110 nm CMOS process and the needed power supply is 1.2 V. The ASIC domain is divided in five blocks as described in Table 5.10. In detail:

- Voltages VDD_buff_1_X (pads 21 and 55), VDD_buff_2_X (pad 22 and 54) and preamp_X (pads 24 and 52) operates as analog supply of the pixel matrix. They are put on the right and left sides of the pinout but they are internally connected each other.

- VDD_grdr_X (pads 26 and 50) act as polarizaton of the n-well ring implemented with isolating purposes of the pixel array with respect to the end of column; the two pads are connected internally.
- VDD_dig (pads 29 and 48) operate as supply for the digital parts of the pixel matrix and of the EoC. They are internally connected each other as well.
- Ground: seven pads are dedicated to the general ground.
- Bias of the chip: seven pads are dedicated to this purpose. Pads 57, 58 and 59 are utilized for the four buffers and the preamplifier. Table 5.11 shows the recommended values for all the blocks. Remember that each current is used to supply all the sectors, so 1/4 of the total current is dedicated to each of them.

Furthermore, there are four bias voltages:

- VBsln_regulator (pad 17): used to modify the baseline value; the nominal value (see Table 5.12) sets a 450 mV baseline; by decreasing VBsln_regulator, the baseline increases.
- VTP (pad 18): during the Test Pulse Mode, it defines the amplitude of the signal generated.
- pCas (pad 19): used by the preamplifier.
- nCas (pad 20): used by the preamplifier.

5.3.7 Readout modes

5.3.7.1 Diode reset

During the turning on phase pf the chip, all the diodes must be reset by enabling the DiodeReset signal. It is active low, so when it is enabled (DiodeReset=low) the n-well voltage of the diode is put to VDD. Typical pulse width of these signals is 250 ns.

Afterwords, three different readout modes are possibile:

- *Standard mode*: the entire matrix is read with no test pulse signal applied.

Signal	Value [V]			Description
	min	typ	max	
VDD_buff_1_X	1	1.2	1.4	feeding of the 1st buffer stage and polarizing the VDD_IO line
VDD_buff_2_X	1	1.2	1.4	feeding the 2nd buffer stage and to polarizing the VDD_CORE lin
VDD_preamp_X	1	1.2	1.4	feeding of the preamps and to polarizing the VDD_IO_2 line
VDD_grdr_X	1	1.2	1.2	polarizing the nwell ring around the pixel matrix and the EoC
VDD_dig_X	1	1.2	1.4	feeding of all the digital logic of the ASIC
GND_X	-	0	-	General ground

Table 5.10: Voltage supply values.

Signal	Value [μA]			Description
	min	typ	max	
biasPreamp	1	4	8	feeding 4 sectors $\rightarrow$ each sector needs 1 μA
biasBuffer1	4	8	15	feeding 4 sectors $\rightarrow$ each sector needs 2 μA
biasBuffer2	100	200	400	feeding 4 sectors $\rightarrow$ each sector needs 50 μA

Table 5.11: Bias current values.

Signal	Value			Description
	min	typ	max	
VBsln_regulator	0V	370 mV	1.2 V	0 V = no regulation; 1.2 V = max $\rightarrow$ baseline moved to 0 V)
VTP	0V	X	VBsln_regulator	0 V to get the biggest signal
pCas	300 mV	400 mV	500 mV	Bias for cascode p-type
nCas	550 mV	650 mV	750 mV	Bias for cascode n-type

Table 5.12: Bias voltage values.

Figure 5.13: Diode reset.

- *Test Pulse mode*: the entire matrix is read but all the pixels are programmed with the Test Pulse signal (TestPulse enable to receive a test signal).
- *Fixed Pixel mode*: a selected pixel (the same pixel in the each sector) is continuously read.

5.3.7.2 Standard mode

Standard mode represents the usual way to read the pixel array: in this mode it is possible to read the entire matrix without test pulse signals. The way to perform this reading can be summarized as follows:

1. feReset and Bsln_regulator_ctrl are active low signals; feReset resets the preamplifier, Bsln_regulator_ctrl sets the baseline based to the Vblsn_regulator analog signal (with typical pulse width $\approx$ 50 ns).
2. SampleBsln is an active high signal; it is able to store the preamplifier output to the baseline value (with typical pulse width $\approx$1 μs).
3. Then at this phase the signal is expected to arrive;
4. SampleSignal is an active high signal; as SampleBsln, it is able to store the preamplifier output to the signal value (with typical pulse width $\approx$1 μs).
5. Here, starts the reading phase:
    - this phase starts with the disabling of the ResetRead (active low) signal; to properly start the readout cycle, ResetRead must be low until the end of the SampleSignal duration and then it must switch to 1: in other words, the rising edge of the ResetRead can be considered as a StartRead signal. ResetRead must be kept disabled (equal to 1) until the end of the readout phase (30-50 μs, based on the frequency to the read clock).
    - Clock signals enabled (h_read_clk and v_read_clk).

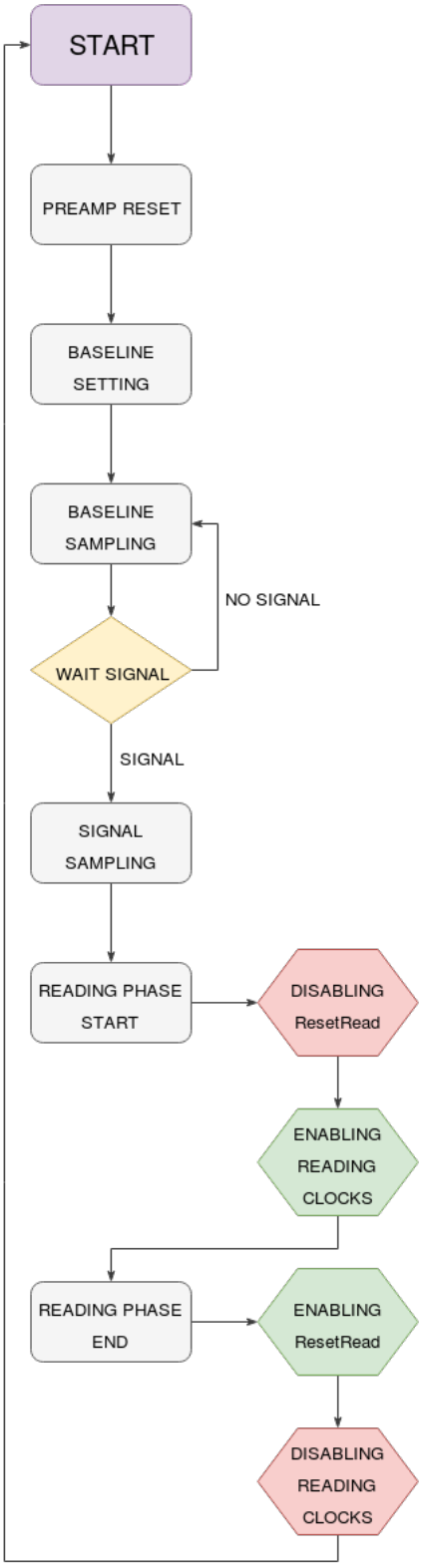


Figure 5.14: Standard mode readout flow of MATISSE.

6. Re-enabling ResetRead signal setting it to 0. Eventually, clock signal may be stopped.

7. The readout cycle may be started again. (go to point 1).

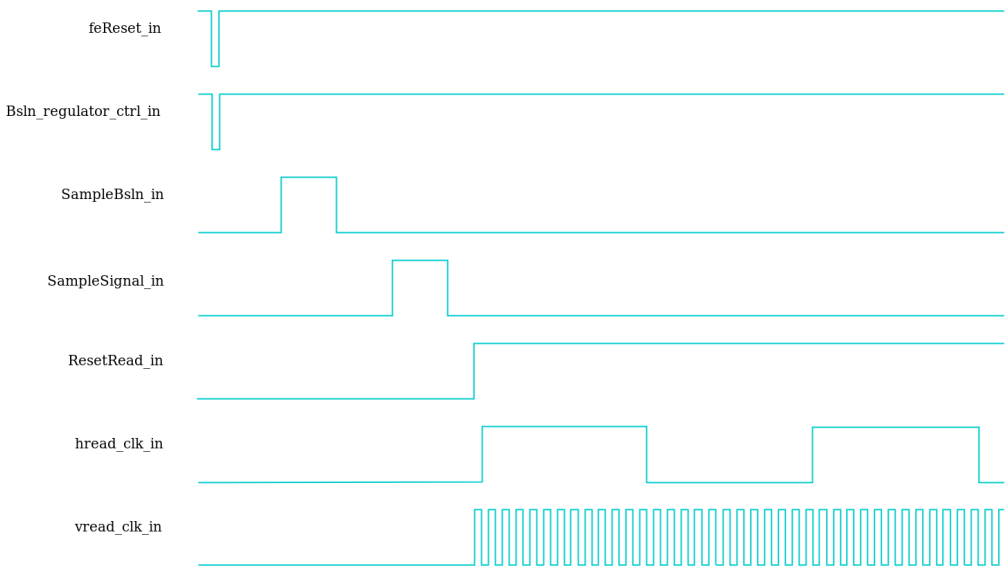


Figure 5.15: Standard mode.

5.3.7.3 Test pulse mode

Test pulse mode is quite similar to the standard mode to read the pixel array: however, in this mode it is possible to send a test pulse to some selected pixels as well.

The way to perform this reading can be summarized as follows:

1. feReset and Bsln_regulator_ctrl are active low signals; feReset resets the preamplifier, Bsln_regulator_ctrl sets the baseline based to the Vblsn_regulator analog signal (with typical pulse width $\approx$ 50 ns).

2. SampleBsln is an active high signal; it is able to store the preamplifier output to the baseline value (with typical pulse width $\approx$1 μs).

3. Test Pulse (TP) is an active high signal; it enables the analog VTP signal for the test pulse phase. VTP has to remain active during the SampleSignal phase for test pulse signal sampling with typical pulse width $\approx$2 μs).

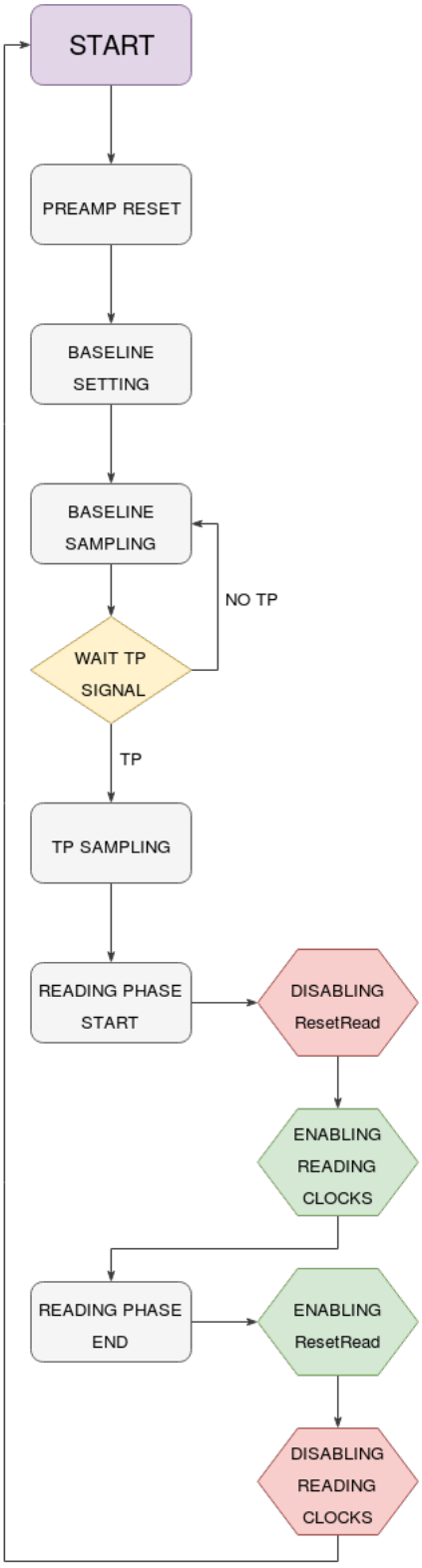


Figure 5.16: Test pulse mode readout flow of MATISSE.

4. SampleSignal is an active high signal; as SampleBsln, it is able to store the preamplifier output to the signal value (with typical pulse width $\approx$1 μs).

5. Here starts the reading phase:

   - This phase starts with the disabling of the ResetRead (active low) signal; to properly start the readout cycle, ResetRead must be low until the end of the SampleSignal duration and then it must switch to 1: in other words, the rising edge of the ResetRead can be considered as a StartRead signal. ResetRead must be kept disabled (equal to 1) until the end of the readout phase (30-50 μs, based on the frequency to the read clock).
   - Clock signals enabled (h_read_clk and v_read_clk).

6. Re-enabling ResetRead signal setting it to 0. Eventually, clock signal may be stopped.

7. The readout cycle may be started again. (go to point 1).

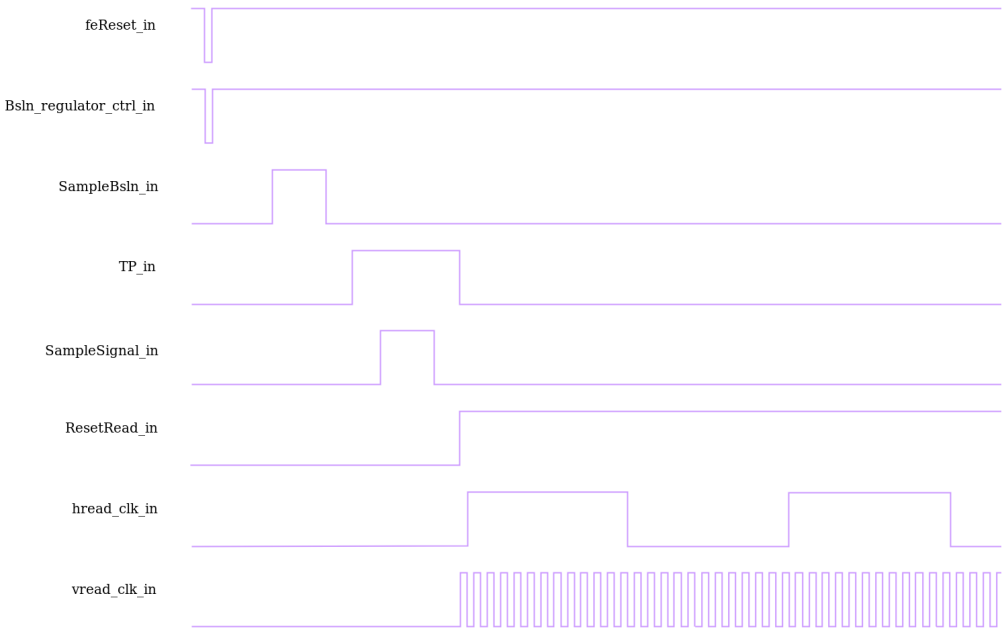


Figure 5.17: Test pulse mode.

5.3.7.4 Fixed pixel mode

In this mode the same pixel in each sector is uninterruptedly read: to do that, the SampleSignal is maintained always active and the two clock signals (vertical and horizontal) are stopped.

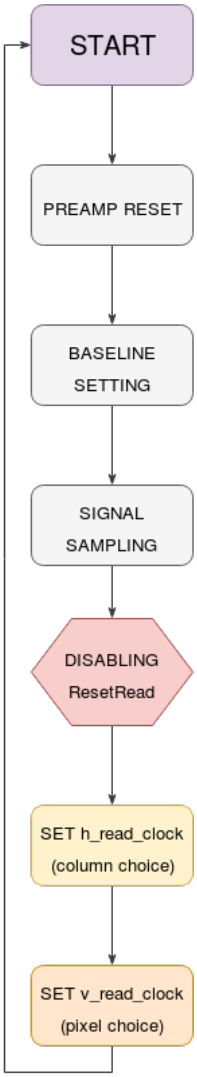


Figure 5.18: Fixed pixel mode readout flow of MATISSE.

The fundamental aim of this reading mode is the preamplifier output monitoring. It may be performed in the following way.

1. feReset and Bsln_regulator_ctrl are active low signals; feReset resets the

preamplifier, Bsln_regulator_ctrl sets the baseline based to the Vblsn_regulator analog signal (with typical pulse width $\approx$ 50 ns).

2. SampleSignal is an active high signal; it is able to store the preamplifier output to the signal value. In this mode it needs to be kept active for the entire acquisition cycle.

3. This phase starts with the disabling of the ResetRead (active low) signal; to properly start the readout cycle, ResetRead must be low until the end of the SampleSignal duration and then it must switch to 1: in other words, the rising edge of the ResetRead can be considered as a StartRead signal. In this specific mode, differently to the previous ones, ResetRead must switch.

4. to select the pixel to read it is necessary to select the column by using the h_read_clk signal (the number of column is equal to the number of clock rising edges).

   - first rising edge $\rightarrow$ first column;
   - second rising edge $\rightarrow$ second column;
   - third rising edge $\rightarrow$ third column;
   - fourth rising edge $\rightarrow$ fourth column;
   - fifth rising edge $\rightarrow$ fifth column;
   - sixth rising edge $\rightarrow$ sixth column;

   Once the selected column is reached, the horizontal clock must be stopped.

5. Similarly, the selection of the pixel happens by using the v_read_clk: the pixel number corresponds to the number of its falling edges:

   - first rising edge $\rightarrow$ first pixel;
   - second rising edge $\rightarrow$ second pixel;
   - third rising edge $\rightarrow$ third pixel;
   - ...
   - twentyfourth rising edge $\rightarrow$ twentyfourth pixel;

   Once the selected pixel is reached, the vertical clock must be stopped.

6. The preamplifier output of the four pixel selected (one for each sector of the matrix) can be read on the four outSignal analog signals.

7. To read another different pixel, the enable of the ResetRead signal is necessary. Then points 3 and 4 can be repeated.

Signal	Active	Description
Bsln_regulator_ctrl	LOW	If it is set to 0 V the baseline is tuned on the VBsln_regulator value.
Digital_in	-	Generation digital noise purposes.
DiodeReset	LOW	If it is set to 0 V it resets all the 576 collection diodes.
feReset	LOW	If it is set to 0 V it resets the full front-end.
prg_bit	-	It is used to write the register of the EoC (digital input).
ResetPrg	LOW	It is used to reset all the 1152 configuration registers.
ResetRead	LOW	It is used to reset the 572 readout registers.
SampleBsln	HIGH	If it is at 1.2 V, the baseline is sampled.
SampleSignal	HIGH	If it is at 1.2 V, the signal is sampled.
TP	HIGH	Test pulse injection signal.

Table 5.13: Digital input values.

5.4 Tests

MATISSE chips have been received in April 2017 from the foundry and successively wire-bonded on custom mezzanine boards developed by the Padova and Torino INFN groups. Deep verification tests has been performed during the following months [7] [107].

5.4.1 Data Acquisition System

In order to perform some laboratory tests regarding both the sensor and readout electronics of MATISSE, a easily reconfigurable and versatile DAQ system for pixel detectors has been employed [8]. It consists of a modular configuration based on a

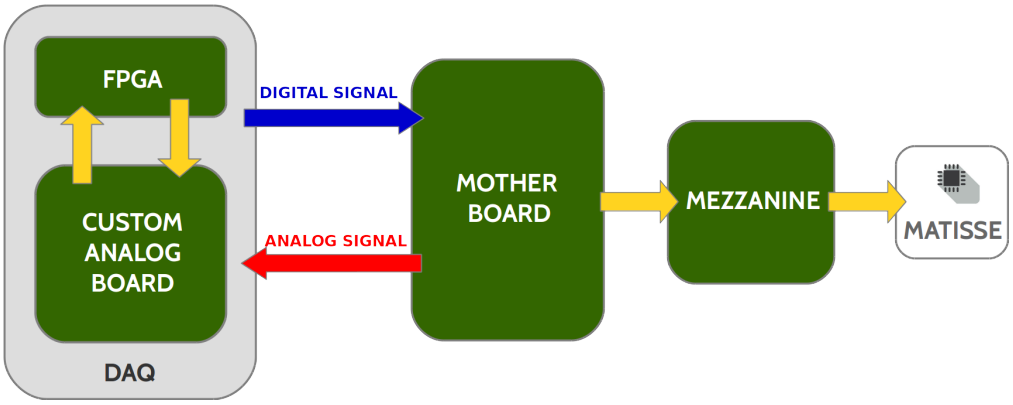


Figure 5.19: Schematic view of the DAQ used for MATISSE tests.

commercial FPGA evaluation board and a custom-developed analog board. Both at the software and at the firmware level, it is able to perform the management and the reading of several different chips, minimizing the effort for the implementation of new test procedures and the updating of the system. The DAQ scheme is depicted in Figure 5.19.

The custom analog board is dedicated to the biases and signals management is characterized by five analog channels each equipped with 14 bit ADCs and an analog (differential or single ended) input stage. An internal clock generator supplies a 100 MHz clock for circuitry operations. Concerning input/output features, 16 LVDS input and 16 LVDS output are provided and 25 pins (single ended/differential I/Os) are left free to be programmed based on the circumstance; overall, 57 lines are

dedicated for I/O communication.
The modular approach adopted for this DAQ system allows the easy replacement of various parts of the circuitry, especially for what concerns the FPGA board, which may be substituted with another version on need.
Going into details, the MATISSE custom mother board (developed for this specific occasion) is able to furnish needed biases and to commmunicate with the analog custom board. A custom-developed mezzanine, at the end, hosts MATISSE chip bonded on it and provides ancillary circuitry (test points, trimmers...) for data communication between DAQ and chip.
This communication is then performed by mean of a custom C++/ROOT software; its GUI simplifies online tuning of the acquisition parameters' changes and allows direct control on them: Figure 5.20 i.e. shows an online acquisition screenshot: this plot represents the pixel map itself: a color code from white to black permits to map the hit values range and to reconstruct the laser halo on the sensor, evaluating the collected charge value for each pixel. In addition to that, some data analysis plot (based on ROOT interface) are returned by the software.

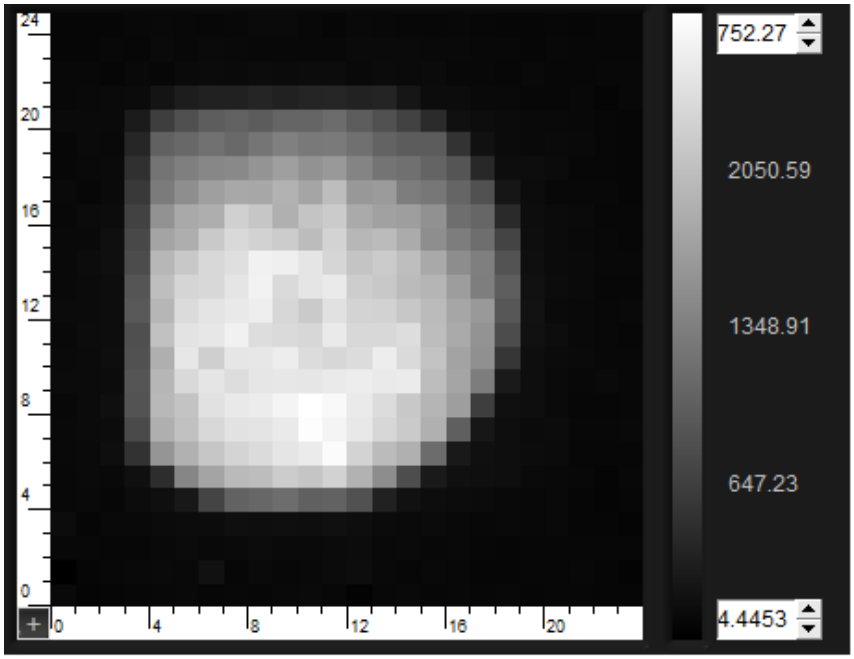


Figure 5.20: An example of an online matrix view with a laser spot reconstruction built with the C++/ROOT software interface (plot via [7]).

5.4.2 Power consumption

Power consumption represents a crucial node for the particle detectors: since the huge number of single chips arranged in hundreds of meter squares inside the inner layers of particle detectors, a low power consumption of the single chip becomes a central issue for the developers. For this reason, the analog chain of MATISSE has been developed to reach low power dissipation throughout the normal chip functioning.

Here, some power test were performed and comparison with the simulations has been done, in order to pinpoint possible discrepancies. First of all, a full check of the external nodes has been done: this operation has revealed a full uniformity for the pixel array and for the DC input voltage. Device tests have been performed so that three different configurations may be observed: the first, just with the Mother Board switched on without any MATISSE chip; a second, with the MATISSE chip mounted and configured in an idle mode and a third with the ASIC in transmission mode. These test results are shown in Table 5.14.

The Mother Board power dissipation has been measured in two different nodes: for the $\pm$5 V and $\pm$1.2 V power supply values. In the higher power condition a 2.4 mW has been found, while a 0.54 mW power dissipation has been recorded in the second case, lower with respect to the simulated value (0.57 mW, about 5%). The second and the third configuration has been compared with simulation results. In detail, for MATISSE in idle configuration, simulation data shows a 6 μW/channel and $\approx$3.6 mW during the integration time while 14.4 mW has been found for the transmission mode.

Measurements appear in good agreement with what expected: 6 mW for the idle configuration and 13.2 mW for the transmission mode. In both case, these measurements demonstrate that all parts work properly. Table 5.14 summarizes these results.

Measurement	**Simulated**	**Measured**
Mother board [$\pm$5 V]	-	2.4 mW
Mother board [$\pm$1.2 V]	0.57 mW	0.54 mW
Mother board + ASIC in Idle [1.2 V]	$\approx$4.7 mW	6 mW
Mother board + ASIC in data trasmission [1.2 V]	14.4 mW	13.2 mW

Table 5.14: Power dissipation measurements (table via [7]).

5.4.3 Test pulse linearity

In order to maximise the flexibility of the characterization of the sensor, some effort has been put into in-pixel circuitry design, especially for what concerns the optimization of the dynamic range and the linearity. Internal test pulse feature (see Section 5.3.7.3) allows to verify these parameters locally and without need of real external signals; however, even if there is no need to use the real sensor signal, it is important to fully deplete the sensor in order to avoid leakage current issues.
Injected charge and test pulse amplitude can be tuned through their full dynamic range and linearity by mean of a trimmer put in the ASIC mezzanine: top plot in Figure 5.21 shows the off-chip voltage amplitude (V_{signal} - $V_{baseline}$) for several input charges from 0 fC up to 2.2 fC: these values corresponds full range of pulse amplitudes that can be produced.
The difference between measured and theoretical linear trend between voltage and charge is approximately of 0.5%, as can be seen in the bottom plot in Figure 5.21.
Baseline regulation analysis can be employed to make some consideration on dy-

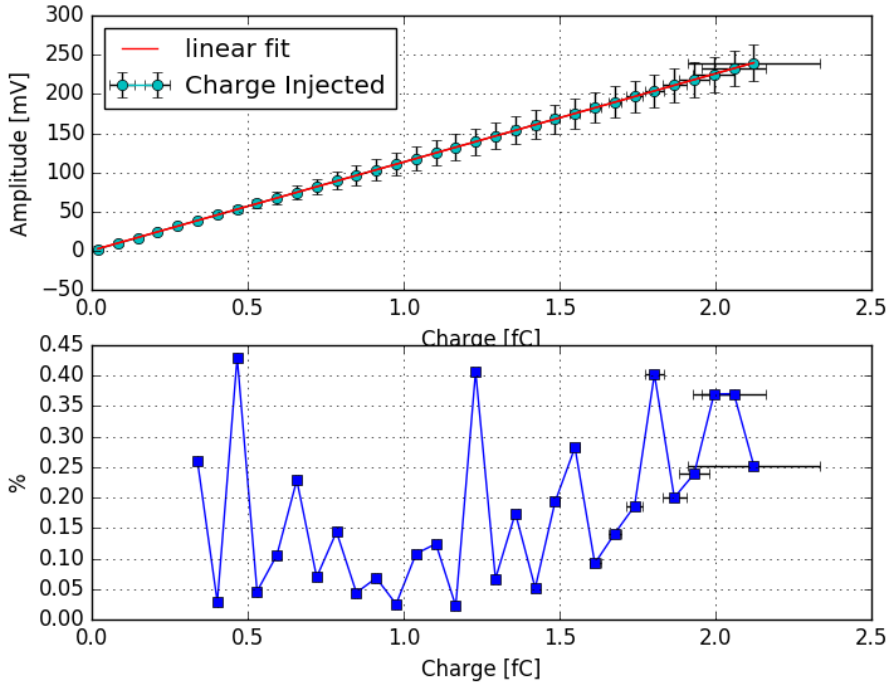


Figure 5.21: Test pulse linearity.

namic range. Baseline can be modified by mean of a dedicated trimmer: in such a way, regulation can be performed through a wide range (of ≈400 mV) for all the pixel array. Figure 5.22 shows the extremely good linearity of the readout electronics chain, in good agreement with simulations.

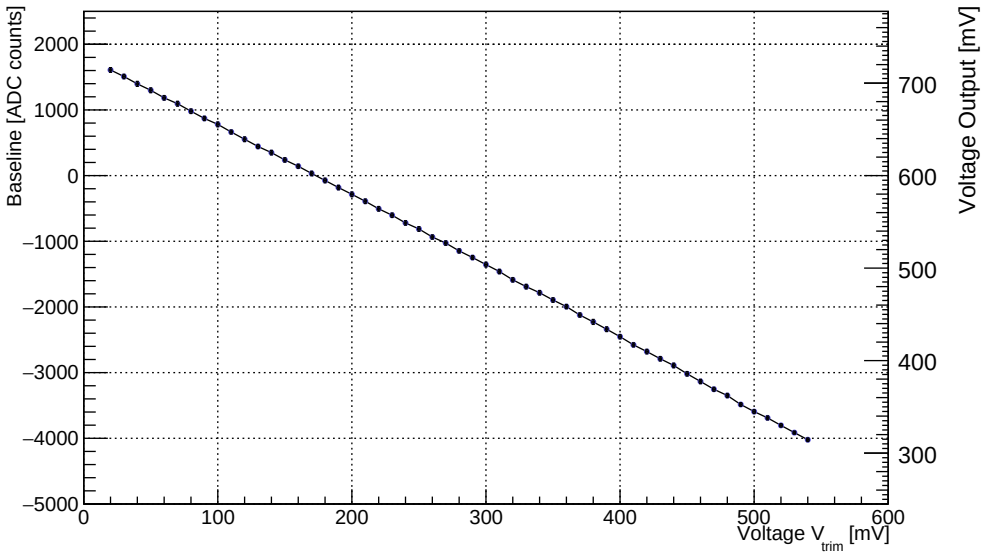


Figure 5.22: Baseline regulation plot.

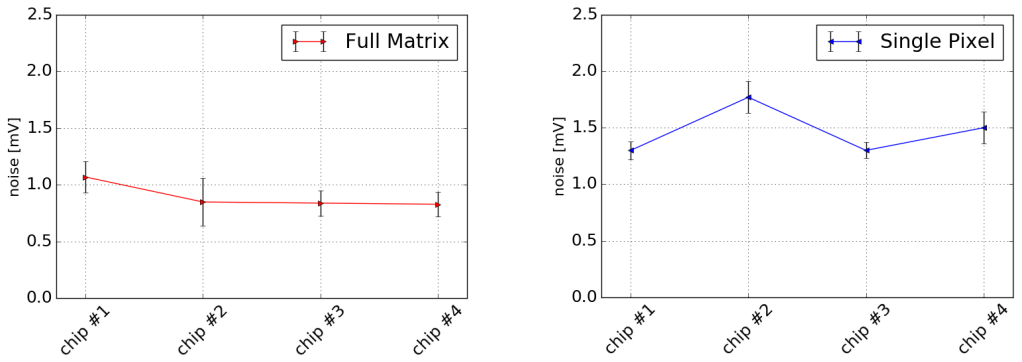
5.4.4 Noise measurements

Both the full matrix and the single (random) pixel have been tested for noise measurements. For both the cases, the sensor has been full depleted in order to reach the most realistic working configuration.
The full matrix test has been performed by mean of the DAQ automatic data acquisition feature [8]: after sensor full depletion, the DAQ is able to send a reset signal to all the 576 pixels, then is able to regulate the baseline and then to sample the output of the CSA. For each sample, the automatic DAQ allows to repeat the operation: in this specific case, this procedure has been iterated for four hundreds times.
Since the distribution of all the noise measurements have been assumed to be Gaussian, Figure 5.23(a) is consistent with the expected distribution; here, five different samples measurements are shown.

The measurements are in good agreement with the simulations expected values (≈900 μV); chip #2 show a more significant error bar with respect to the other samples, probably due to the depletion uniformities, observed in other cases as well. Error bars are obtained automatically from the DAQ itself, which provides, in addition to on-line data acquisition, the noise analysis too.
On the other hand, single pixel noise measurements has been performed on the same chip samples by mean of an oscilloscope selecting the test pulse mode and sampling the analog output (Figure 5.23(b)). In this case, the noise measurement is indirect and it is obtained from the slew rate and the jitter values in such a way (Eq. 5.1):

$$noise[mV] = SR\left[\frac{mV}{ns}\right] \times Jitter[ns] \tag{5.1}$$

The measured pixel, as said before, has been choose randomly. Error bars are obtained from the scope sensitivity. Here, measurement results appear pretty higher than the full matrix ones, but still compatible in the error range.



(a) (b)

Figure 5.23: Jitter measurements by mean of the automatic data acquisition with DAQ[8] (Fig. 5.23(a)) and by mean of the oscilloscope (Fig. 5.23(b))

5.4.5 ^{55}Fe irradiation tests

In order to perform a calibration test on MATISSE chip, an irradiation test with a radioactive source (isotope ^{55}Fe) has been performed at the Physics Department of Padova, with the INFN Padova Group. The ^{55}Fe emission spectrum is characterized by a main energy peak at 5.9 keV (equivalent to ≈1650 electrons).
In Fig. 5.25 the distribution of the four matrix sensors (from 0 to 3) separately are

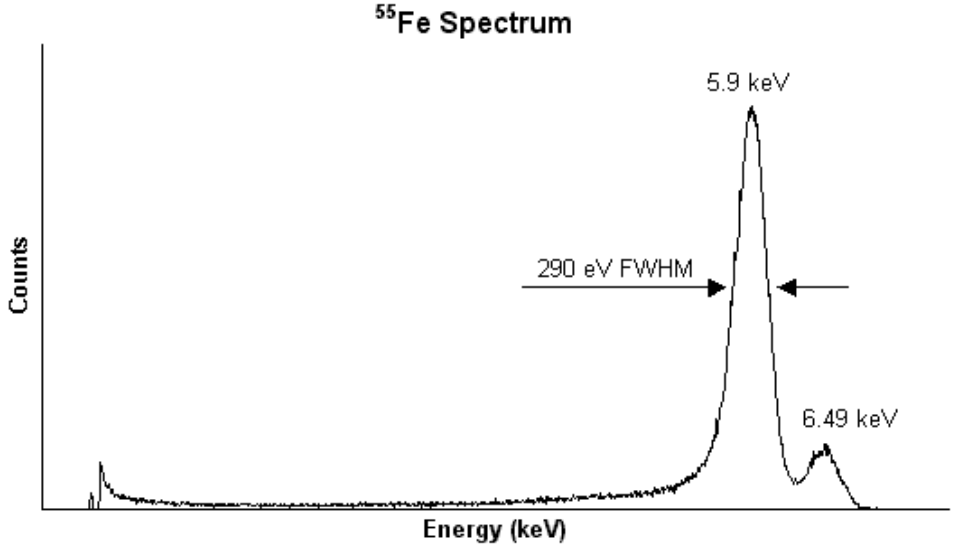


Figure 5.24: ^{55}Fe peak.

shown with a selected V_{bias} = -160 V. All the clusters are identified by considering a 5×5 matrix around an hit pixel, called *seed*. Seed's SNR (Signal-to-Noise Ratio) is 5, while for the pixel in its neighborhood is set to 2. The measured energy spectrum shows a main peak between 430-450 ADC counts for all the four sectors and this allows to derivate the analog gain value, which is of 117 mV/fC, in good agreement with simulations.
Noise of a single pixel can be determined with this calibration measurement. This test has been performed in dark conditions, at room temperature performing a 1600 events run. The rms of the gaussian distribution of all these events is hold as the noise value (expressed in ADC counts) for each pixel. The distribution (in electron value) of these noise values is depicted in Fig. 5.26; ≈40 electrons is the average value.

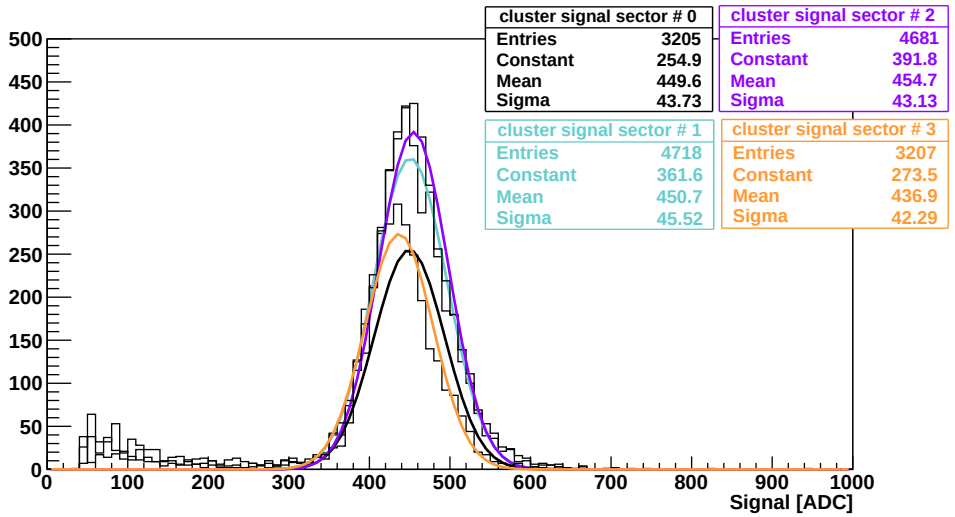


Figure 5.25: Irradiation test of the MATISSE using a ^{55}Fe source. Each plot corresponds to the results of a matrix sector (plot via [7]).

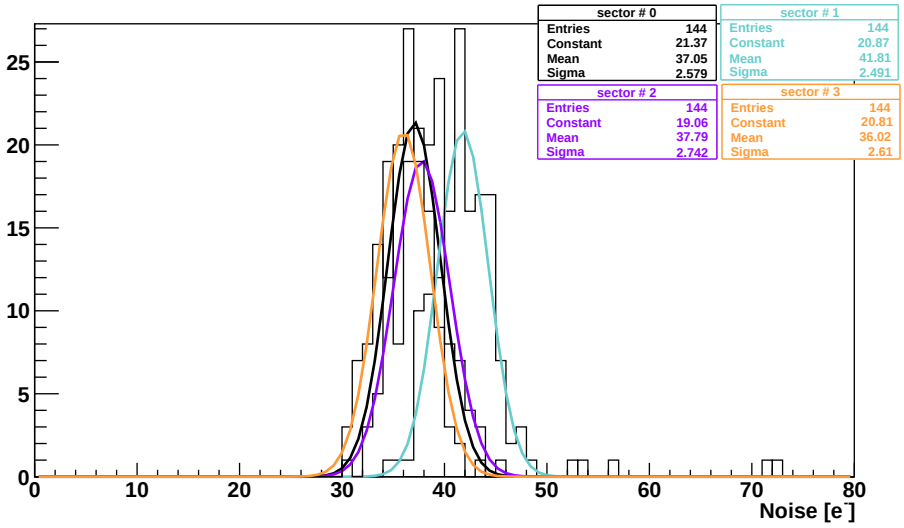


Figure 5.26: Irradiation test of the MATISSE using a ^{55}Fe source. Each plot corresponds to the results of a matrix sector (plot via [7]).

5.4.6 Storage time

Signal degradation vs readout time estimation allows to estimate the loss of information inside the device and the negative effect of leakage current. This measurement involves two different voltages, called *Sample A* and *Sample B*; they are stored in two memories and their readout is continually repeated for 10 ms. Figure 5.27 shows the different trend between the two: this effect is due to different leakage current effect depending on the voltage (the higher is the voltage, the more marked is the leakage). This measurement, then, permits the estimation of the drop voltage through the capacitor provoked by leakage and then the loss of information related to this.
Readout time in the real procedure is evaluated to be $\approx$30 μs with a frequency clock

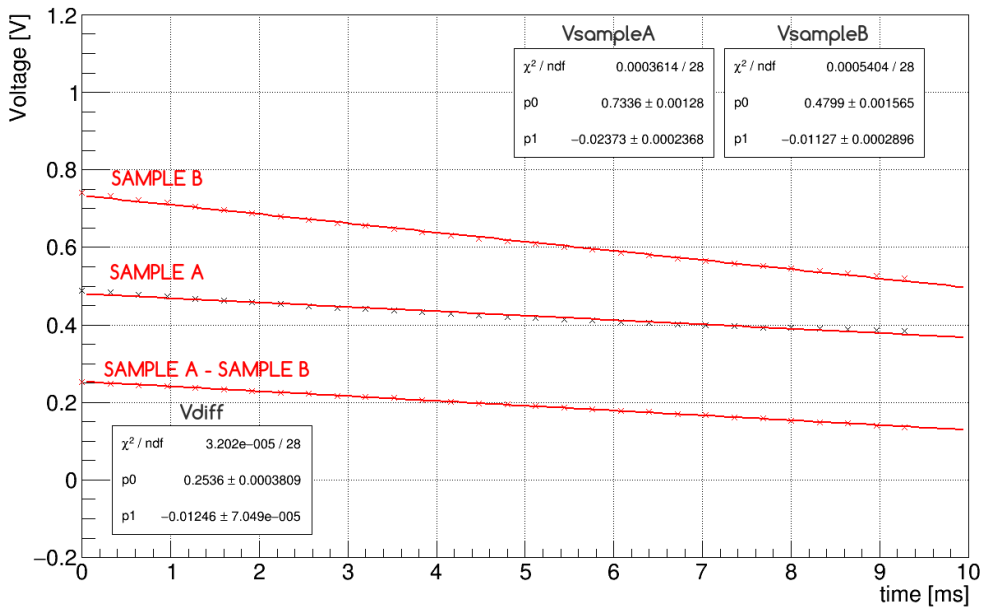


Figure 5.27: Storage time results (plot via [7]).

of 5 MHz; here, a minimum drop voltage of 350 μV (which corresponds to a charge of 3×10^{-3} fC) is estimated, which can be considered negligible. In addition to that, in the real application the useful information correspond to the difference between the two voltages, which is less sensitive than the single signal.

5.5 Conclusions

MATISSE ASIC is a low-power readout chip developed in a 110 nm CMOS process for fully depleted MAPS applications conceived for particle detectors for High Energy Physics experiments. Designed by Torino and Padova INFN groups and Università di Trento/TIFPA, it is based on double-side 300 μm thick sensors with collection by drift. A 24×24 matrix with a die size of 2×2 mm^2 constitutes the front-end electronics. The pixel cell contains both the collection node and the readout electronics and it is 50×50 μm^2 large. First prototypes have been received from the foundry in April 2017 and following measurements on the front end electronics have been performed. Test results show power consumption (6 mW in idle mode and 13.2 mW in data transmission mode) and noise measurements (for the full matrix and the single pixel) in good agreement with simulations. Irradiation tests (perfomed using a ^{55}Fe source) provide a 117 mV/fC analog gain with noise values of approximately 40 e$^-$/sector.

Conclusions

During my Ph.D. period I have directly participated to the development activities for what concerns some architectural parts of the prototype of MATISSE: in detail, some starting all-digital design for the sensor readout during the very initial part of the SEED project and, later, the architecture of the final prototype. Successively, I contributed to its readout electronics and sensor tests. Results of these tests have been presented during a poster session of IEEE MIC-NSS conference in Atlanta (USA) in October 2017. Past experiences on another monolithic sensor project (ALPIDE in ALICE Collaboration at CERN) helped me to have a synoptic view on their application in HEP.

In parallel, I managed all the configuration and the process-specific setting up of Scientific Linux workareas for the foundry process design kit: I also managed the relations with the techno department of the foundry and I developed scripts and updated on need the PDK versions. This helped me to understand better the full path of the ASIC design, from the basic tool configuration to the final physical prototype to test.

For what concerns CHIPIX65 project, I have participated to the laboratory and irradiation tests in Turin and in Padua: I presented these test results with a talk during IEEE MIC-NSS in Strasbourg (France) in November 2016.

The same for the 65 nm PLL, tested in Turin and in Padua for a TID irradiation test. Test results are going to be published in the next months in a full-paper dedicated [1].

[1] "*A Compact, Low Jitter, CMOS 65 nm 4.8-6 GHz Phase-Locked Loop for Applications in HEP Experiments Front-End Electronics*", Giovanni Mazza and Serena Panati, IEEE Transaction on Nuclear Science (TNS), TNS-00182-2018.

Appendix A

Radiation effects on silicon devices

A.1 Dose units

- **Absorbed Dose**: energy locally absorbed per unit mass due to ionization.

  the gray is the SI unit for the absorbed dose;

  the rad (Radiation Absorbed Dose) is commonly used.

  1 gray = 1 joule/kilogram (SI units) = 100 rad

  The dose needs to be referred to the absorbing material (e.g. Si, SiO_2 , GaAs)

- **Equivalent Dose** H_T: it is the measure of the transferred energy weighted with the W_R factor (type and energy of the incident particle)

  $H_T = W_R \cdot Dose$

  It is expressed in Sievert (Sv)

  it shows a measure of the damage of the incident particle on the selected target.

- **Effective Dose**: it is a measure of the biological risk

  It is weighted with a factor W_T depending on the type of tissue (skin, gonad, thyroid...)

A.2 Total Dose Effects

Ionization processes consist in adding or removing charged particles (such as electrons) from atoms. The electron-holes pair creation in the device oxide may cause long term effects (charge trapping): its consequence is a alteration of the electrical characteristics such as failures and degradation. Typically, two mechanism give their contribute:

- hole traps generation (V_{ot})
- interface states (V_{it})

both of them contribute, in the case of MOS technologies, to shifting of the transistor threshold voltage V_{th}. Under a TID (Total ionization Dose) exposure, come effects may be seen:

- first-order effects in the thick field isolation region;
- second-order effects: in the transistor gate region.

Hole traps accumulation cause primarily increasing of leakage and failures in MOS devices which are, on the other hand, less sensitive to the creation of interface traps. However, the combination of these two mechanisms can modify intensely the device behavior. Furthermore, their effect is strongly dependent to the process and the structure. In addition, recombination rates are deeply subject to the activation energy [108][109][110].

A.3 Heavy-Ion Effects

A.3.1 Types of Single Event Effects

Definition of the SEE by the European Aviation Safety Agency (EASA)[111]

> *A Single Event Effect (SEE) is a basic hardware issue as it occurs when a bit is flipped in hardware due to, among other causes, the effects of radiation on microelectronic circuits. SEEs may be non-destructive (typically transient errors that cause a temporary change of combinational logic, called Single Event Transients or SETs, or permanent errors that cause for example a change of a memory cell value, called Single Bit Upsets, Multiple Bit Upsets, Single Event Functional Interruptions or Single Event Latchups) or destructive (Single Event Burnouts, Single Event Gate Ruptures or Stuck Bits). Due to their potential impact on the behavior of airborne electronic hardware, it is necessary to address the impact of these effects (transient or permanent) on airborne electronic hardware and the potential safety impact at the Aircraft/Engine level.*

SEE could be of two different types:

- **destructive**: their effect is permanent
- **non-destructive**: their effect can be either temporary or permanent.

A.3.1.1 SEU

It generates a change of state in a memory storage cell (latches, RAM, μP cache memory/registers, FPGA). The SEU affects latches, registers, sequential logic and memory devices. A single event can produce upsets in more than one cell of the storage (i.e. multiple transistors' charge collected) depending on the amount of charge deposited and the size of the region in which it is deposited. This effect is called MCU (Multiple Cell Upset).

A.3.1.2 MBU

An Multiple Bit Upset is a single event which upsets more than one bit in the same logical word during a single measurement. When a MBU occurs, both multiple bit errors in a single word can be generated and single bit upset in multiple adjacent words.

A.3.1.3 SEFI

A Single Event Functional Interrupt is defined as a long duration loss of functionality or a interruption of the normal operation (like a burst of errors) in complex IC due caused by a perturbation of clocks or control registers. Usually it is not followed by an high current condition combined with a single event snap-back (SESB) or a single event latch-up (SEL). It is possible to recover the full functionality by reloading a configuration register, reloading the system or by cycling the power.

A.3.1.4 SET

A Single Event Transient (SET) is a pulse or a voltage propagation through a circuit during a single clock cycle. This causes a wrong logic state which could propagate if it happen during the active clock edge. Eventually this spurious signal may be latched in a memory cell. In order to mitigate this issue, three kind of masking techniques may limit its turning into an error:

- timing masking or latch window (in the case of elements outside their latching time window affected by SET)
- electrical masking (SET attenuation due to subsequent logic gates which can filter it)
- logic masking (non-sensitized path affected by SET)

A.3.1.5 SED

A Single Event Disturb describes the transient unstable state of a static random access memory (SRAM) which eventually may reach a stable state and, in that case,

the SED may be considered belonging to the SEU type. Since the unstable state of the cell may be quite long for performing read instructions and, consequently, generate soft errors, SEDs are defined separately.

A.3.1.6 SHE

A Single Event Hard Error (SHE) describes the condition when a particle-induced upset is not retrievable; e.g., when a particle hit, in addition to a bit-flip, damages the device substrate.

A.3.1.7 SEL

A Single Event Latchup happens in four layer semiconductor devices when one of a pair of parasitic transistor are activated by an energized particle; this may cause a short across the circuit until the power is cycled or the device burns. This effect may be destructive when it causes overheating and metal fusion.

A.3.1.8 SESB

A Single Event Snap-Back is a subtype of SEL and it shows exhibit a high current consuming condition inside the circuit. An energized particle, hitting near the drain may cause an avalanche multiplication of the charge carrier. For this reason the transistor becomes open and remains until a new cycling of the power.

A.3.1.9 SEB

A Single Event Burnout (SEB) may be destructive (with a permanent resulting failure) for the device because of a high current state in a power transistor. Typically SEB susceptibility decreases when teh temperature increases. With the definition of SEB some others effect are described: gate rupture, noise in charge-coupled devices, frozen bits, high voltage MOSFET burnout.

A.3.1.10 SEGR

A particle bombardment may cause a Single Event Gate Rupture, by creating a damage due to ionization between the drain and the gate oxide in power components. It normally produce some exeeding leakage current at the drain and the gate It could have destroy the device.

A.3.1.11 SEDR

The Single Event Dielectric Rupture causes a small permanent jump in the core power supply current.

A.3.2 Mitigation Techniques

It is possible to classify the most common mitigation techniques into three distinct groups:

1. Layout level techniques (require the manufacturing processes control)
    - guard-ring insertion
    - trench isolation design
    - transistor layout modification
2. Circuit level techniques
    - margins design (usually used for destructive SEE)
    - hardened cell design
    - design by using ECCs
    - spatial or temporal redundancy
3. Transistor layout level techniques
    - semiconductor materials improvements

SEE TYPE	AFFECTED ELECTRONICS	VISIBLE EFFECT
SEU	memories, latches	information stored in a memory cell corrupted
MBU	memories, latches	information stored in more than one memory cell corrupted
SEFI	built-in state or control section devices	normal operativity lost
SET	analog and mixed-signal electronics, photonics	unexpected impulse response into the circuitry
SED	latches, combinational logic	information stored in a bit temporarily corrupted
SHE	memories, latches	unmodifiable change of state in a memory cell
SEL	BiCMOS; CMOS	high-current conditions
SESB	MOSFET (n-channel)	high-current conditions
SEB	BJT, power MOSFET (n-channel)	burnout with destructive consequences
SEGR	power MOSFET	gate-dielectric rupture
SEDR	FPGA, non-volatile nMOS structures	dielectric rupture

Table A.1: SEE overview

	Hard SEE						Soft SEE					
	SEU	**MBU**	**MCU**	**SEFI**	**SET**	**SED**	**SHE**	**SEL**	**SESB**	**SEB**	**SEGR**	**SEDR**
Memories	✓	✓	✓	✓	✓	✓	✓					
Logic (Latches)	✓	✓	✓			✓	✓					
Logic (Combinational)				✓	✓	✓		✓				
Microprocessors	✓											
State Controller	✓	✓	✓	✓			✓					
Analog and mixed circuits				✓					✓			
Photonics				✓								
FPGA	✓	✓	✓	✓			✓	✓				✓
ASIC	✓	✓	✓	✓			✓	✓				
Power MOSFET									✓	✓	✓	✓
Power Devices					✓			✓				
Converters	✓				✓			✓		✓	✓	

Table A.2: Applicability of SEE to circuit types.

	Hard SEE						Soft SEE				
	SEU	**MBU**	**MCU**	**SEFI**	**SET**	**SED**	**SHE**	**SEL**	**SESB**	**SEB**	**SEGR**	**SEDR**
Board-level/Current protection								✓	✓			
Horizontal mitigation	✓	✓						✓	✓			
Vertical mitigation								✓	✓			
Spatial redundancy	✓				✓	✓	✓					
Temporal redundancy	✓				✓	✓						
Parity	✓	✓				✓						
ECCs	✓	✓				✓						
Scrubbing	✓	✓				✓						
Interleaving			✓									
Reset/cycling				✓				✓	✓			
External circuit protection										✓	✓	✓
Design margins										✓	✓	✓

Table A.3: Common mitigation techniques for SEE.

Appendix B

Process Design Kit (PDK) installation and maintenance

In order to design integrated circuits or tailor fabrication silicon processes, a Process Design Kit (PDK) is provided by the foundry.
The PDK is indispensable to design, draw, simulate and verify the circuit before producing it. Each PDK is thus a collection of scripts an data files specific to the foundry and to the chosen silicon process. Accuracy into PDK development guarantee more successful first-pass silicon production.
Based on the tool utilized for the design, PDK may provide different format for the input files and libraries. Usually an NdA (Non-Disclosure Agreement) is required; however there are also some open source projects [112].
Generally [113] a Process Design Kit may contain:
Some technology files:

- Layers, layers purposes and names
- Display attributes, fillers and colors
- Electrical rules
- Process constrains

Primitive devices library:

- Symbols

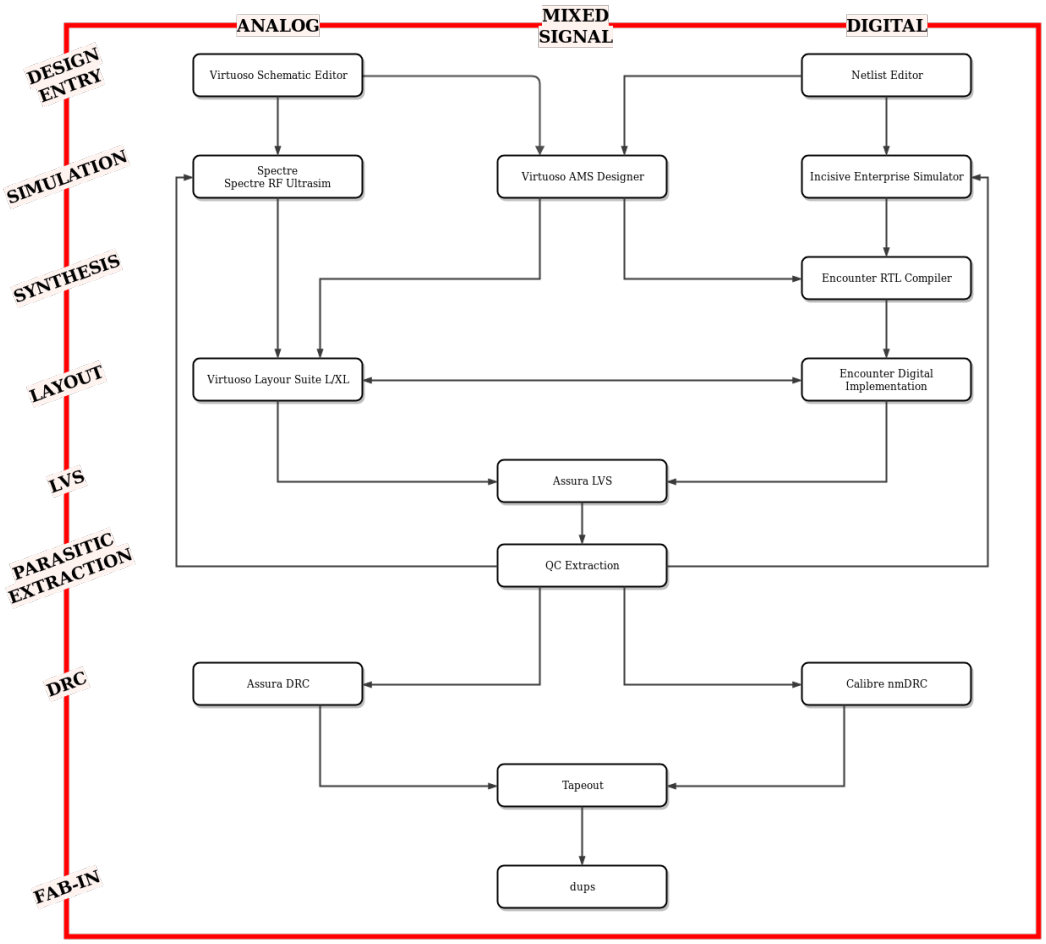


Figure B.1: EDA design flow example for Cadence© tools.

- parameterized cells (PCells)
- Devices parameters

Rule files:

- Library Exchange Format (LEF)
- Design Exchange Format (DEF)
- other tool-proprietary format files

Simulation models for primitives:

- SPICE models (or SPICE derivatives) for transistors
- SPICE models (or SPICE derivatives) for resistors

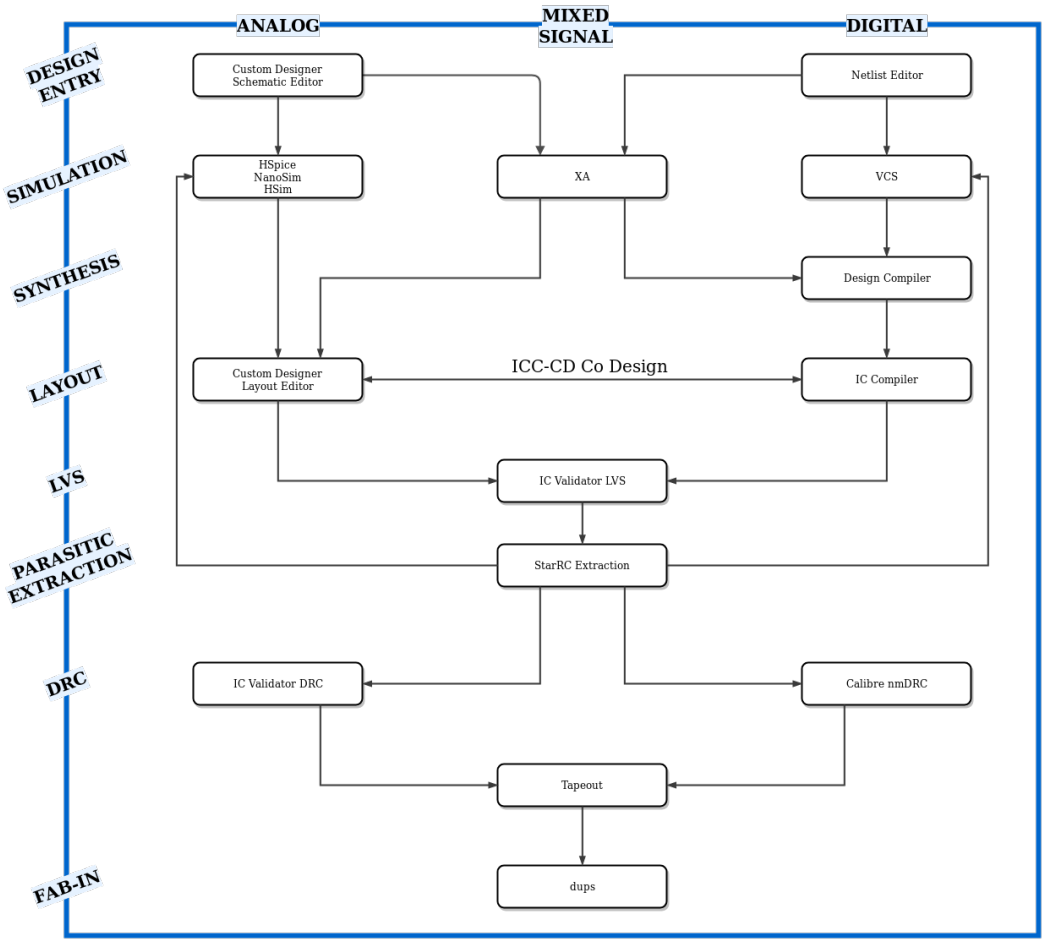


Figure B.2: EDA design flow example for Synopsys© tools.

- SPICE models (or SPICE derivatives) for capacitors
- SPICE models (or SPICE derivatives) for inductors

Verification decks:

- Layout Versus Schematic (LVS)
- Design Rule Check (DRC)
- Antenna Check
- Electrical Rule Check
- Physical Extraction

- Parasitics Extraction

Standard cell libraries for digital development:

- Gates symbols
- Library Exchange Format (LEF) of abstracted layouts
- Liberty files (.lib)
- Graphic Database System (GDSII) or Open Artwork System Interchange Standard (OASIS) stream data

In addition to that, some configuration between EDA tools, PDK and operative system are needed. Development of Perl scripts [114] or shell scripts[115] may be useful on need in order to make comfortable digital and analog workareas making and setting [116] and general PDK maintenance and updating.

Appendix C

Phase noise

C.0.1 Oscillator phase noise: general theory

Oscillators' phase and frequency has been the subject of a lot of studies likewise the number of models for different typologies of oscillators. Most of them are based on linear time invariant (LTI) model systems that does not take into account the internal mechanism which let device noise becoming phase noise. Furthermore the reduced order of these models does not allow to make precise prediction about the phase noise in long ring oscillator or circuits which contains essential singularities.

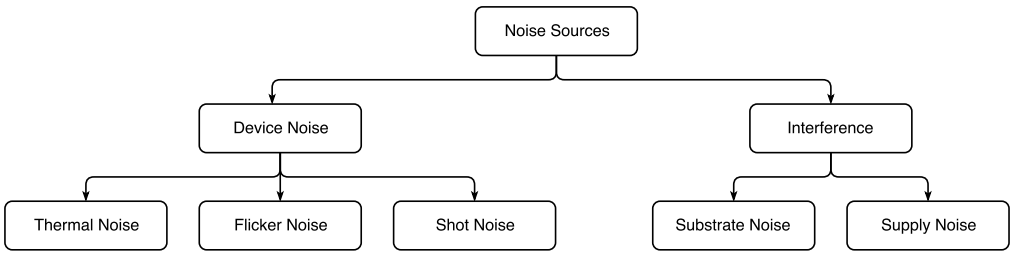


Figure C.1: Noise sources.

An accurate modeling of phase noise needs to consider oscillators as linear time-varying (LTV) systems, which shows stationary and cyclostationary noise source, differently from LTI systems.
As it is possible to see in Fig. C.1, sources can be divided in two branches: such as *device noise* and *interference*. Thermal, flicker and shot noise belong to the first group, substrate and supply noise to the second. The time-varying model allows

to include into the systems all those mechanisms (random or deterministic noise and spurious sources) which are converted in amplitude or phase noise inside the circuit. In this context, LTI models can be considered as special cases of time-varying systems.

C.0.1.1 Background and definitions

Let us consider an ideal sinusoidal oscillator. Its output voltage can be written as

$$V_{out}(t) = A\cos\left[\omega_0 t + \phi\right] \tag{C.1}$$

where A is the signal amplitude (in Volts), ω_0 is the angular frequency (in rad/s) and ϕ is the arbitrary fixed phase (in Volts). If an ideal oscillator which does not fluctuate randomly is considered, the spectrum shows only two pulses corresponding to the values $\pm\omega_0$.
Now let us consider a real oscillator:

$$V_{out}(t) = A(t)\cdot f[\omega_0 t + \phi(t)] \tag{C.2}$$

the time amplitude and phase are both function of the time and f is a periodic function with a period of 2π. For this reason, amplitude and phase shows fluctuations and the real oscillator spectrum has sidebands around the carrier frequency ω_0. How to quantify them? There are many methods but, usually, a signal's short term fluctuation is defined in terms of single sideband noise density and expressed in dBc/Hz (decibel below the carrier frequency per hertz) and they are such that calculated (including the effect of $A(t)$ and $\phi(t)$):

$$\mathscr{L}_{total}\left\{\Delta\omega\right\} = 10\cdot log\left[\frac{\mathscr{P}_{sideband}(\omega_0+\Delta\omega_0, 1Hz)}{\mathscr{P}_{carrier}}\right] \tag{C.3}$$

where $\mathscr{P}_{sideband}(\omega_0+\Delta\omega_0, 1Hz)$is the single sideband power calculated at the angular frequency offset $\Delta\omega$ from the carrier with a bandwidth of 1 Hz. Easy to calculate, this parameter shows the drawback of including in itself the sum of both phase and amplitude variation, disallowing the knowledge of them separately. However, in the majority of applications, the phase noise part is dominating on the amplitude one, so we can say that

$$\mathscr{L}_{total}\{\Delta\omega\} \approx \mathscr{L}_{phase}\{\Delta\omega\} \tag{C.4}$$

The semi-empirical model (Leeson-Cutler phase noise model [117]) for tuned tank oscillator, is based on a LTI assumption and it is described by the following relation:

$$\mathscr{L}\{\Delta\omega\} = 10 \cdot log\left\{\frac{2FkT}{P_s} \cdot \left[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \tag{C.5}$$

where F is the *device excess noise number* (empirical),k is the Boltzmann's constant, T the absolute temperature, ω_0 is the angular frequency, P_s is the average power dissipated in the resistive part of the considered tank, $Q_L$is the quality factor of the tank , $\Delta\omega$ is the offset from the carrier and $\Delta\omega_{1/f^3}$ is the frequency of the corner between $1/f^3$ and $1/f^2$.

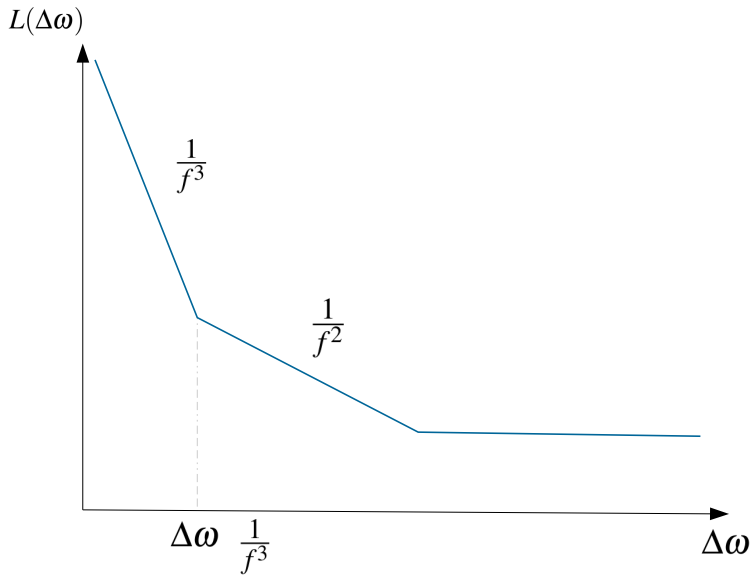


Figure C.2: Phase noise vs frequency offset of the carrier.

The analysis of $1/f^2$ region can be performed by calculating the transfer function,

which can be modeled for a parallel RLC with $\Delta\omega << \omega_0$ starting from its impedance

$$Z(\omega_0+\Delta\omega) \approx \frac{1}{G_L}\frac{1}{1+j2Q_L\frac{\Delta\omega}{\omega_0}} \tag{C.6}$$

where G_L is the parallel parasitic conductance of the tank; $G_m R_L = 1$ for steady-state oscillations.
The closed-loop transfer function of a RLC oscillator can be written ad the imaginary part of the following equation

$$H(\Delta\omega) = \frac{v_{out}(\omega_0+\Delta\omega)}{i_{in}(\omega_0+\Delta\omega)} = -j\frac{1}{G_L}\frac{\omega_0}{2Q_L\Delta\omega} \tag{C.7}$$

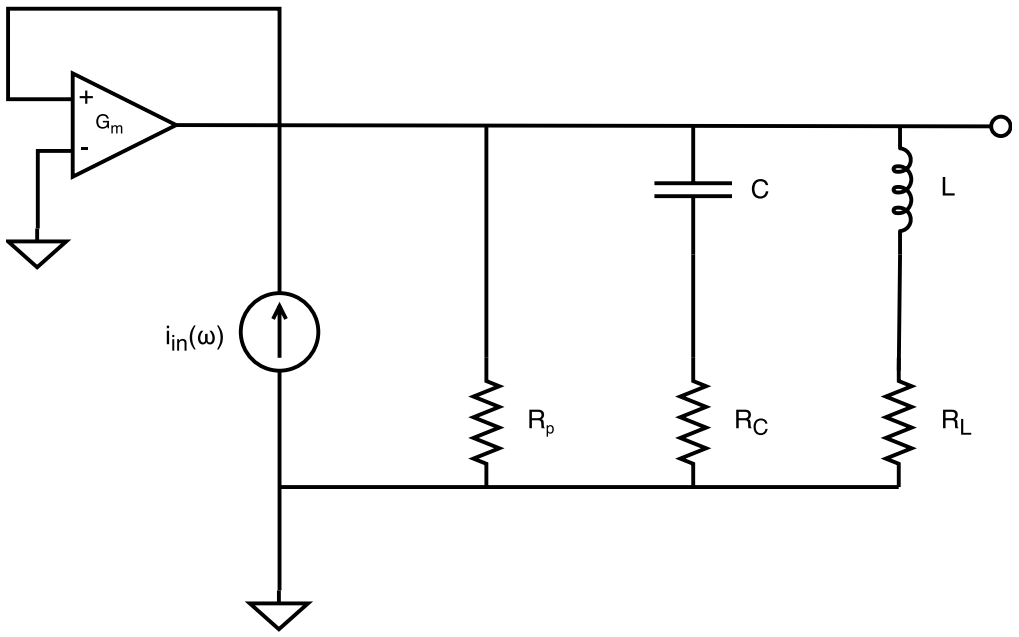


Figure C.3: A typical RLC oscillator scheme.

The equivalent mean square noise current density of the total equivalent resistance is equal to

$$\overline{i_n^2}/\Delta f = 4kTG_L \tag{C.8}$$

However, traditionally all noise sources are combined in one term given by the resistor noise and a F factor (”device excess noise number”), so the effective equivalent mean square noise current density can be written as

$$\overline{i_n^2}/\Delta f = 4FkTG_L \tag{C.9}$$

Unfortunately, since the noise of a real oscillator is cyclostationary, which means that it arises depending on various processes, F cannot be calculated a priori and, as $\omega_{1/f}^3$ parameter has to be considered as a posteriori fitting parameters.
By using the Eq.C.9, the phase noise in the $1/f^2$ spectrum worths:

$$\begin{aligned}\mathscr{L}\{\Delta\omega\} = 10\cdot\log\left(\frac{\overline{v_{noise}^2}}{v_{sig}^2}\right) &= 10\cdot\log\left[\frac{\frac{1}{2}\cdot|H(\Delta\omega)|^2\cdot\overline{i_n^2}/\Delta f}{\frac{1}{2}\cdot V_{max}^2}\right] \\ &= 10\cdot\log\left[\frac{2FkT}{P_s}\cdot\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\end{aligned} \tag{C.10}$$

$1/f^2$ region is the only portion of phase noise analytically achievable; the $1/f^3$ is usually treated as empirical. So, for the identification of the other individual noise sources of a tuned tank oscillator, the same approach can be employed, so for the RLC in Fig. C.3 the phase noise spectrum can ben written as

$$\mathscr{L}\{\Delta\omega\} = 10\cdot\log\left[\frac{kT\mathscr{R}_{eff}[1+\mathscr{A}]\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2}{\mathscr{V}_{max}^2/2}\right] \tag{C.11}$$

where $\mathscr{A}$ is an empirical fitting parameter and $\mathscr{R}_{eff}$ is the effective series resistance (Fig. C.3):

$$\mathscr{R}_{eff} = R_L + R_C + \frac{1}{R_p(C\omega_0)^2} \tag{C.12}$$

However, in order to improve the likeliness to reality, this approach does not represent a good method. For this reason some other methods are implemented [118, 119].

C.0.1.2 Excess phase impulse response model

Oscillator can be modeled as a black box with n different inputs and just two outputs: the instantaneous amplitude $A(t)$ and the excess phase noise $\phi(t)$. Noise inputs are represented by voltage sources (in series) with circuit branches and current sources

injecting into the circuit nodes. By studying frequency-domain fluctuation in these two systems (for each input, both systems are single-input and single-output systems), $A(t)$ and $\phi(t)$ can be determined. In general, given an arbitrary input current $i(t)$ injected in each node, excess phase noise can be determined by the equation

$$\phi(t) = \frac{1}{q_{max}} \left[\frac{c_0}{2} \int_{-\infty}^{t} i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau) \cos(n\omega_0 \tau) d\tau \right] \tag{C.13}$$

where q_{max} is the maximum charge displacement across a capacitor node, τ is the time during which the impulse is injected, c_n is the Fourier coefficient found for the *impulse sensitivity function* (ISF). The general case, for a current close to the multiple of the oscillation frequency ($i(t) = I_n \cos[(n\omega_0 + \Delta\omega)]$ can be defined as:

$$\phi(t) \approx \frac{I_n c_n \sin(\Delta\omega t)}{2 q_{max} \Delta\omega} \tag{C.14}$$

C.0.1.3 Transformation of phase to voltage

The previous method shows, given a current $i_n(t)$ how to calculate the excess phase noise. However the knowledge of how the output voltage is related to this excess phase fluctuations is needed to calculate power spectral density (PSD) of the output voltage $S_v(\omega)$ of the oscillator. The conversion in a voltage of the device noise current is made of two different terms: the non-linear phase modulation (PM) and the LTV current-to-phase conversion. In this context, a current injected at $n\omega_0 + \Delta\omega$ generates two equal sidebands at $\omega_0 \pm \Delta\omega$ and the carrier sideband power is equal to

$$P_{SBC}(\Delta\omega) = 10 \cdot \log \left(\frac{I_n c_n}{4 q_{max} \Delta\omega} \right)^2 \tag{C.15}$$

C.0.1.4 Phase noise sideband power prediction

If the current source $i_n(t)$ is random with both a $1/f$ region and a flat region. It can be demonstrated that the phase noise spectrum equation for a the $1/f^2$ region, given an input noise current with a white power spectral density of $\bar{i}_n^2/Deltaf$ is given by

the following:

$$\mathscr{L}\{\Delta\omega\} = 10 \cdot \log\left(\frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{4 \cdot \Delta\omega^2}\right) \tag{C.16}$$

where Γ_{rms} is the rms value of $\Gamma^(x)$, meanwhile the following one descrive the phase noise in the $1/f^3$ corner, due to internal noise sources:

$$\omega_{1/f^3} = \omega_{1/f^2} \cdot \frac{c_0^2}{2\Gamma_{rms}^2} \approx \omega_{1/f} \cdot \left(\frac{c_0}{c_1}\right)^2 \tag{C.17}$$

c_0 depends on the waveform and can be reduced in the case of particular oscillation symmetry.

C.0.1.5 Sources of cyclostationary noise

Let us consider now the time-varying system which is affected by sources of random noise which fluctuate periodically (cyclostationary sources). A white cyclostationary noise current can be defined as:

$$i_n(t) = i_{n0}(t) \cdot \alpha(\omega_0 t) \tag{C.18}$$

where $i_{n0}(t)$ is the stationary process and $\alpha(\omega_0 t)$ is the deterministic function related to the amplitude modulation of noise. So the phase noise can be written as

$$\phi(t) = \int_{-\infty}^{t} i_n(t)\frac{\Gamma(\omega_0\tau)}{q_{max}}d\tau = \int_{-\infty}^{t} i_{n0}(t)\frac{\alpha(\omega_0\tau)\Gamma(\omega_0\tau)}{q_{max}}d\tau \tag{C.19}$$

so, the cyclostationary noise can be described as stationary noise applied to a system which shows an effective ISF such as

$$\Gamma_{eff}(x) = \Gamma(x) \cdot \alpha(x) \tag{C.20}$$

$\alpha(x)$ can be derived from operating point and noise characteristics.

C.0.1.6 Output phase noise with multiple noise source prediction

The previous section methodology can be extended to multiple noise sources and multiple nodes by mean of superposition combining all the contributions. In general, this method can be summarized like this:

- to find the equivalent voltage noise sources in series with each inductor and current noise sources in parallel with each capacitor;
- to check out which are correlated and uncorrelated noise sources;
- to find transfer functions to the output excess phase (which means, to find the ISF for each source and the Γ_{rms} and the coefficient c_0 of it);
- to find the phase noise power from each source by using Γ_{rms}, c_0 and the power spectrum of input noise sources (Eq.C.16);
- to sum the uncorrelated sources (individual output phase noise powers) e square sum the correlated ones;
- to obtain the total noise power below the carrier.

References

[1] B Abelev et al and The ALICE Collaboration. Technical design report for the upgrade of the alice inner tracking system. *Journal of Physics G: Nuclear and Particle Physics*, 41(8):087002, 2014.

[2] S. Panati, A. Paternò, E. Monteil, L. Pacher, N. Demaria, A. Rivetti, M. D. R. Rolo, R. Wheadon, F. Rotondo, G. Dellacasa, F. Licciulli, F. Loddo, F. Ciciriello, C. Marzocca, S. Mattiazzo, F. De Canio, L. Gaioni, V. Re, G. Traversi, L. Ratti, S. Marconi, G. Magazzù, A. Stabile, and P. Placidi. First measurements of a prototype of a new generation pixel readout ASIC in 65 nm CMOS for extreme rate hep detectors at HL-LHC. In *2016 IEEE Nuclear Science Symposium, Medical Imaging Conference and Room-Temperature Semiconductor Detector Workshop (NSS/MIC/RTSD)*, pages 1–7, Oct 2016.

[3] M. Mager. ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 824:434 – 438, 2016. Frontier Detectors for Frontier Physics: Proceedings of the 13th Pisa Meeting on Advanced Detectors.

[4] K. D. Stefanov, A. S. Clarke, and A. D. Holland. Fully depleted pinned photodiode cmos image sensor with reverse substrate bias. *IEEE Electron Device Letters*, 38(1):64–66, Jan 2017.

[5] Popp, Martin (Chur, CH), De Coi, Beat (Sargans, CH), Annese, Marco (Chur, CH). Semiconductor structure for photon detection, December 2014.

[6] J. D. Segal, C. J. Kenney, S. I. Parker, C. H. Aw, W. J. Snoeys, B. Wooley, and J. D. Plummer. Second generation monolithic full-depletion radiation sensor with integrated cmos circuitry. In *IEEE Nuclear Science Symposuim Medical Imaging Conference*, pages 1896–1900, Oct 2010.

[7] S.Panati, J.Olave, A. Rivetti, L.Pancheri, F.Cossio, P.Giubilato, D.Pantano, S.Mattiazzo, M.D.Da Rocha Rolo, and N.Demaria. Matisse: A versatile readout electronics for monolithic active pixel sensors characterization. In *IEEE MIC-NSS*, Oct 2017.

[8] M. Battaglia, D. Bisello, D. Contarato, P. Giubilato, D. Pantano, T. Tanabe, and M. Tessaro. Flexible daq system for pixel detectors. In *2008 IEEE Nuclear Science Symposium Conference Record*, pages 2159–2163, Oct 2008.

[9] Meroli, Stefano. *Silicon pixel detectors for high precision measurements*. PhD thesis, Perugia U., 2012.

[10] C. Bower P. Garrou and P. Ramm. *Handbook of 3D Integration*. Wiley-VCH, 2008.

[11] D. Jain and J. Nuwad and N. Manoj and V. Sudarsan. Chapter 19 - Diamond-Based Radiation Detectors for Applications in Highly Corrosive Solutions and High-Radiation Fields . In Tyagi, A.K. and , and Banerjee, S. , editor, *Materials Under Extreme Conditions* , pages 683 – 715. Elsevier, Amsterdam, edition, 2017.

[12] Zhuqing Zhang and C. P. Wong. Recent advances in flip-chip underfill: materials, process, and reliability. *IEEE Transactions on Advanced Packaging*, 27(3):515–524, Aug 2004.

[13] Erik H.M. Heijne. Semiconductor micropattern pixel detectors: a review of the beginnings. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 465(1):1 – 26, 2001. SPD2000.

[14] V. A. Wright, W. D. Davidson, J. J. Melone, V. O'Shea, K. M. Smith, L. Donohue, L. Lea, K. Robb, S. Nenonen, and H. Sipila. Three-dimensional medipix-a new generation of x-ray detectors. *IEEE Transactions on Nuclear Science*, 52(5):1873–1876, Oct 2005.

[15] Christian, D. C. and Appel, J. A. and Chiodini, G. and Hoff, J. and Kwan, S. and Mekkaoui, A. and Yarema, R. FPIX2, the BTeV pixel readout chip. *Nucl. Instrum. Meth.*, A549:165–170, 2005.

[16] J.N. Butler. BTEV — A Dedicated B physics detector at the Fermilab Tevatron Collider. *Nuclear Physics B - Proceedings Supplements*, 55(1):251 – 259, 1997.

[17] Stephen Holmes, Ronald S Moore, and Vladimir Shiltsev. Overview of the tevatron collider complex: goals, operations and performance. *Journal of Instrumentation*, 6(08):T08001, 2011.

[18] Christian, D C. The architecture of the BTeV pixel readout chip. Technical Report FERMILAB-CONF-2002-319-E, FERMILAB, Batavia, IL, 2002.

[19] M. Destefanis. The PANDA experiment at FAIR. *Nuclear Physics B - Proceedings Supplements*, 245:199 – 206, 2013. The Proceedings of the 7th Joint International Hadron Structure'13 Conference.

[20] G. Mazza, D. Calvo, P. De Remigis, M. Mignone, J. Olave, A. Rivetti, R. Wheadon, and L. Zotti. The topix v4 prototype for the triggerless readout of the panda silicon pixel detector. *Journal of Instrumentation*, 10(01):C01042, 2015.

[21] M De Gaspari, J Alozy, R Ballabriga, M Campbell, E Fröjdh, J Idarraga, S Kulis, X Llopart, T Poikela, P Valerio, and W Wong. Design of the analog front-end for the timepix3 and smallpix hybrid pixel detectors in 130 nm cmos technology. *Journal of Instrumentation*, 9(01):C01037, 2014.

[22] T. Poikela, J. Plosila, T. Westerlund, M. Campbell, M. De Gaspari, X. Llopart, V. Gromov, R. Kluit, M. van Beuzekom, F. Zappon, V. Zivkovic, C. Brezina, K. Desch, Y. Fu, and A. Kruth. Timepix3: a 65k channel hybrid pixel readout chip with simultaneous toa/tot and sparse readout. *Journal of Instrumentation*, 9(05):C05013, 2014.

[23] X. Llopart and R. Ballabriga and M. Campbell and L. Tlustos and W. Wong. Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 581(1):485 – 494, 2007. VCI 2007.

[24] T. Poikela, M. De Gaspari, J. Plosila, T. Westerlund, R. Ballabriga, J. Buytaert, M. Campbell, X. Llopart, K. Wyllie, V. Gromov, M. van Beuzekom, and V. Zivkovic. Velopix: the pixel ASIC for the LHCb upgrade. *Journal of Instrumentation*, 10(01):C01057, 2015.

[25] Karol Hennessy. LHCb VELO upgrade. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 845:97 – 100, 2017. Proceedings of the Vienna Conference on Instrumentation 2016.

[26] T Poikela, J Plosila, T Westerlund, J Buytaert, M Campbell, M De Gaspari, X Llopart, K Wyllie, V Gromov, R Kluit, M van Beuzekom, F Zappon, V Zivkovic, C Brezina, K Desch, Y Fu, and A Kruth. Digital column readout architectures for hybrid pixel detector readout chips. *Journal of Instrumentation*, 9(01):C01007, 2014.

[27] R Turchetta. Cmos monolithic active pixel sensors (maps) for future vertex detectors. *Journal of Instrumentation*, 1(08):P08004, 2006.

[28] R. Turchetta et al. Cmos active pixel sensors: design for scientific applications. *Rutherford Appleton Laboratory, Chilton, Didcot, Oxfordshire, OX11 0QX;United Kingdom*, 2005.

[29] B. Pain, S. K. Mendis, R. C. Schober, R. H. Nixon, and E.R. Fossum. Low-power, low-noise analog circuits for on-focal-plane signal processing of infrared sensors. *Proceedings of SPIE*, 1946:365–374, 1993.

[30] D. Scheffer B. Dierickx, G. Meynants. Near 100% fillfactor cmos active pixels. *Advanced Image Sensors Workshop, Brugge, Belgium*, 1997.

[31] Enrico Giulio Villania and R. Turchetta and M. Tyndel. Analysis and simulation of charge collection in monolithic active pixel sensors (MAPS). *Nuclear*

Physics B - Proceedings Supplements, 125:184 – 188, 2003. Innovative Particle and Radiation Detectors.

[32] E. G. Villani, P. P. Allport, G. Casse, A. Evans, M. Tyndel, R. Turchetta, and J. J. Velthuis. Design and characterization of a novel, radiation-resistant active pixel sensor in a standard 0.25 mu;m cmos technology. In *IEEE Symposium Conference Record Nuclear Science 2004.*, volume 2, pages 1222–1226 Vol. 2, Oct 2004.

[33] G. Rizzo, C. Avanzini, G. Batignani, S. Bettarini, F. Bosi, G. Calderini, M. Ceccanti, R. Cenci, A. Cervelli, F. Crescioli, M. Dell'Orso, F. Forti, P. Giannetti, M. A. Giorgi, A. Lusiani, S. Gregucci, P. Mammini, G. Marchiori, M. Massa, F. Morsani, N. Neri, E. Paoloni, M. Piendibene, L. Sartori, J. Walsh, E. Yurtsev, M. Manghisoni, V. Re, G. Traversi, M. Bruschi, R. Di Sipio, B. Giacobbe, A. Gabrielli, F. Giorgi, G. Pellegrini, C. Sbarra, N. Semprini, R. Spighi, S. Valentinetti, M. Villa, A. Zoccoli, C. Andreoli, L. Gaioni, E. Pozzati, L. Ratti, V. Speziali, D. Gamba, G. Giraudo, P. Mereu, G. F. Dalla Betta, G. Soncini, G. Fontana, M. Bomben, L. Bosisio, P. Cristaudo, G. Giacomini, D. Jugovaz, L. Lanceri, I. Rashevskaya, L. Vitale, and G. Venier. Development of deep n-well maps in a 130 nm cmos technology and beam test results on a 4k-pixel matrix with digital sparsified readout. In *2008 IEEE Nuclear Science Symposium Conference Record*, pages 3242–3247, Oct 2008.

[34] L. Ratti, M. Manghisoni, V. Re, G. Traversi, S. Zucca, S. Bettarini, F. Morsani, and G. Rizzo. Front-end performance and charge collection properties of heavily irradiated dnw maps. *IEEE Transactions on Nuclear Science*, 57(4):1781–1789, Aug 2010.

[35] G. Rizzo, G. Batignani, S. Bettarini, F. Bosi, G. Calderini, R. Cenci, A. Cervelli, M. Dell'Orso, F. Forti, P. Giannetti, M. A. Giorgi, A. Lusiani, G. Marchiori, M. Massa, F. Morsani, N. Neri, E. Paoloni, J. Walsh, C. Andreoli, L. Gaioni, E. Pozzati, L. Ratti, V. Speziali, M. Manghisoni, V. Re, G. Traversi, M. Bomben, L. Bosisio, G. Giacomini, L. Lanceri, I. Rachevskaia, L. Vitale, G. F. Dalla Betta, G. Soncini, G. Fontana, L. Pancheri, G. Verzellesi, D. Gamba, G. Giraudo, P. Mereu, M. Bruschi, A. Gabrielli, B. Giacobbe, N. Semprini, R. Spighi, M. Villa, and A. Zoccoli. Recent development on triple well 130 nm cmos maps with in-pixel signal processing and data sparsification capability. In *2007 IEEE Nuclear Science Symposium Conference Record*, volume 2, pages 927–930, Oct 2007.

[36] Deptuch, G. and Winter, M. and Dulinski, W. and Husson, D. and Turchetta, R. and Riester, J. L. Simulation and measurements of charge collection in monolithic active pixel sensors. *Nucl. Instrum. Meth.*, A465:92–100, 2000.

[37] G. Deptuch, J. D. Berst, G. Claus, C. Colledani, W. Dulinski, Y. Gornushkin, D. Husson, J. L. Riester, and M. Winter. Design and testing of monolithic active pixel sensors for charged particle tracking. *IEEE Transactions on Nuclear Science*, 49(2):601–610, Apr 2002.

[38] J. J. Velthuis, P. P. Allport, G. Casse, A. Evans, R. Turchetta, M. Tyndel, and G. Villani. Characterization of active pixel sensors in 0.25 mu;m cmos technology. *IEEE Transactions on Nuclear Science*, 52(5):1887–1891, Oct 2005.

[39] Chen Xu, Shen Chao, and Mansun Chan. A new correlated double sampling (cds) technique for low voltage design environment in advanced cmos technology. In *Proceedings of the 28th European Solid-State Circuits Conference*, pages 117–120, Sept 2002.

[40] C. Virmontois, C. Durnez, M. Estribeau, P. Cervantes, B. Avon, V. Goiffon, P. Magnan, A. Materne, and A. Bardoux. Radiation effects in pinned photodiode cmos image sensors: Variation of epitaxial layer thickness. *IEEE Transactions on Nuclear Science*, 64(1):38–44, Jan 2017.

[41] V. Goiffon, M. Estribeau, P. Cervantes, R. Molina, M. Gaillardin, and P. Magnan. Influence of transfer gate design and bias on the radiation hardness of pinned photodiode cmos image sensors. *IEEE Transactions on Nuclear Science*, 61(6):3290–3301, Dec 2014.

[42] W. Snoeys. Monolithic pixel detectors for high energy physics. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 731:125 – 130, 2013. PIXEL 2012.

[43] P. Giubilato and D. Bisello and P. Chalmet and P. Denes and K. Kloukinas and S. Mattiazzo and A. Marchioro and H. Mugnier and D. Pantano and A. Potenza and A. Rivetti and J. Rousset and W. Snoeys and C. Tindall. LePix—A high resistivity, fully depleted monolithic pixel detector. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 732:91 – 94, 2013. Vienna Conference on Instrumentation 2013.

[44] P. Giubilato and M. Battaglia and D. Bisello and M. Caselle and P. Chalmet and L. Demaria and Y. Ikemoto and K. Kloukinas and S.C. Mansuy and S. Mattiazzo and A. Marchioro and H. Mugnier and D. Pantano and A. Potenza and A. Rivetti and J. Rousset and L. Silvestrin and W. Snoeys. Monolithic pixels on moderate resistivity substrate and sparsifying readout architecture. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 731:146 – 153, 2013. PIXEL 2012.

[45] A. Potenza and D. Bisello and M. Caselle and M. Costa and N. Demaria and P. Giubilato and Y. Ikemoto and C. Mansuy and A. Marchioro and S. Mattiazzo and M. Moll and L. Pacher and N. Pacifico and D. Pantano and A. Rivetti and L. Silvestrin and W. Snoeys. Radiation tolerance of a moderate resistivity substrate in a modern CMOS process. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and*

Associated Equipment, 718:347 – 349, 2013. Proceedings of the 12th Pisa Meeting on Advanced Detectors.

[46] A. Rivetti and M. Battaglia and D. Bisello and M. Caselle and P. Chalmet and M. Costa and N. Demaria and P. Giubilato and Y. Ikemoto and K. Kloukinas and C. Mansuy and A. Marchioro and H. Mugnier and D. Pantano and A. Potenza and J. Rousset and L. Silvestrin and J. Wyss. CMOS sensors in 90nm fabricated on high resistivity wafers: Design concept and irradiation results. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 730:119 – 123, 2013. Proceedings of the 9th International Conference on Radiation Effects on Semiconductor Materials Detectors and Devices.

[47] S. Mattiazzo and M. Battaglia and D. Bisello and M. Caselle and P. Chalmet and N. Demaria and P. Giubilato and Y. Ikemoto and K. Kloukinas and C. Mansuy and A. Marchioro and H. Mugnier and D. Pantano and A. Potenza and A. Rivetti and J. Rousset and L. Silvestrin and W. Snoeys and J. Wyss. LePIX: First results from a novel monolithic pixel sensor. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 718:288 – 291, 2013. Proceedings of the 12th Pisa Meeting on Advanced Detectors.

[48] P. Riedler. Upgrade of the ALICE Inner Tracking System. *Nuclear Physics A*, 956:866 – 869, 2016. The XXV International Conference on Ultrarelativistic Nucleus-Nucleus Collisions: Quark Matter 2015.

[49] Sabyasachi Siddhanta. The upgrade of the Inner Tracking System of ALICE. *Nuclear Physics A*, 931:1147 – 1151, 2014. QUARK MATTER 2014.

[50] Serhiy Senyukov. The upgrade of the ALICE Inner Tracking System. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 732:164 – 167, 2013. Vienna Conference on Instrumentation 2013.

[51] P. Martinengo. The new Inner Tracking System of the ALICE experiment. *Nuclear Physics A*, 967:900 – 903, 2017. The 26th International Conference on Ultra-relativistic Nucleus-Nucleus Collisions: Quark Matter 2017.

[52] W. Snoeys and G. Aglieri Rinella and H. Hillemanns and T. Kugathasan and M. Mager and L. Musa and P. Riedler and F. Reidt and J. Van Hoorne and A. Fenigstein and T. Leitner. A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 871:90 – 96, 2017.

[53] G Aglieri, C Cavicchioli, P L Chalmet, N Chanlek, A Collu, P Giubilato, H Hillemanns, A Junique, M Keil, D Kim, J Kim, T Kugathasan, A Lattuca, M Mager, C A Marin Tobon, D Marras, P Martinengo, S Mattiazzo, G Mazza,

H Mugnier, L Musa, D Pantano, C Puggioni, J Rousset, F Reidt, P Riedler, S Siddhanta, W Snoeys, G Usai, J W van Hoorne, P Yang, and J Yi. Monolithic active pixel sensor development for the upgrade of the alice inner tracking system. *Journal of Instrumentation*, 8(12):C12041, 2013.

[54] C. Cavicchioli and P.L. Chalmet and P. Giubilato and H. Hillemanns and A. Junique and T. Kugathasan and M. Mager and C.A. Marin Tobon and P. Martinengo and S. Mattiazzo and H. Mugnier and L. Musa and D. Pantano and J. Rousset and F. Reidt and P. Riedler and W. Snoeys and J.W. Van Hoorne and P. Yang. Design and characterization of novel monolithic pixel sensors for the ALICE ITS upgrade. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 765:177 – 182, 2014. HSTD-9 2013 - Proceedings of the 9th International "Hiroshima" Symposium on Development and Application of Semiconductor Tracking Detectors.

[55] Gianluca Aglieri Rinella. The ALPIDE pixel sensor chip for the upgrade of the ALICE Inner Tracking System. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 845:583 – 587, 2017. Proceedings of the Vienna Conference on Instrumentation 2016.

[56] A. Szczepankiewicz. Readout of the upgraded ALICE-ITS. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 824:465 – 469, 2016. Frontier Detectors for Frontier Physics: Proceedings of the 13th Pisa Meeting on Advanced Detectors.

[57] CERN. The high luminosity lhc.

[58] Bejar Alonso, I. and Rossi, L. HiLumi LHC Technical Design Report. 2015.

[59] CERN. 7^{th} framework programme, european research and innovation funding, 2014-2020.

[60] ATLAS-CMS 65 nm pixel ASIC meeting, (2012).

[61] Demaria, Natale and others. RD53 Collaboration and CHIPIX65 Project for the development of an innovative Pixel Front End Chip for HL-LHC. In *Proceedings, INFN Workshop on Future Detectors for HL-LHC (IFD2014): Povo, Italy, March 11-13, 2014*, volume IFD2014, page 010, 2015.

[62] RD53 Collaboration. RD53 collaboration web site.

[63] M. Garcia-Sciveres and J. Christainsen. Rd collaboration proposal: Development of pixel readout integrated circuits for extreme rate and radiation. *CERN-LHCC-2013-008*.

[64] Garcia-Sciveres, Mauricio. RD53A Integrated Circuit Specifications. Technical Report CERN-RD53-PUB-15-001, CERN, Geneva, Dec 2015.

[65] Marconi, S. and Conti, E. and Placidi, P. and Christiansen, J. and Hemperek, T. The RD53 Collaboration's SystemVerilog-UVM Simulation Framework and its General Applicability to Design of Advanced Pixel Readout Chips. *JINST*, 9(CERN-RD53-PUB-14-001):P10005. 15 p, Aug 2014. Comments: 15 pages, 10 figures (11 figure files), submitted to Journal of Instrumentation.

[66] Garcia-Sciveres, Maurice. The RD53A Integrated Circuit. Technical Report CERN-RD53-PUB-17-001, CERN, Geneva, Oct 2017.

[67] CHIPIX65 project. CHIPIX65 project web site.

[68] Capeans, M and Darbo, G and Einsweiller, K and Elsing, M and Flick, T and Garcia-Sciveres, M and Gemme, C and Pernegger, H and Rohne, O and Vuillermet, R. ATLAS Insertable B-Layer Technical Design Report. Technical Report CERN-LHCC-2010-013. ATLAS-TDR-19, Sep 2010.

[69] M. Garcia-Sciveres, D. Arutinov, M. Barbero, R. Beccherle, S. Dube, D. Elledge, J. Fleury, D. Fougeron, F. Gensolen, D. Gnani, V. Gromov, T. Hemperek, M. Karagounis, R. Kluit, A. Kruth, A. Mekkaoui, M. Menouni, and J.-D. Schipper. The fe-i4 pixel readout integrated circuit. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 636(1, Supplement):S155 – S159, 2011. 7th International ""Hiroshima"" Symposium on the Development and Application of Semiconductor Tracking Detectors.

[70] Dominguez, A and Abbaneo, D and Arndt, K and Bacchetta, N and Ball, A and Bartz, E and Bertl, W and Bilei, G M and Bolla, G and Cheung, H W K and Chertok, M and Costa, S and Demaria, N and Daniel Dominguez Vazquez and Ecklund, K and Erdmann, W and Gill, K and Hall, G and Harder, K and Hartmann, F and Horisberger, R and Johns, W and Kaestli, H C and Klein, K and Kotlinski, D and Kwan, S and Pesaresi, M and Postema, H and Rohe, T and Schäfer, C and Starodumov, A and Streuli, S and Tricomi, A and Tropea, P and Troska, J and Vasey, F and Zeuner, W. CMS Technical Design Report for the Pixel Detector Upgrade. Technical Report CERN-LHCC-2012-016. CMS-TDR-11, Sep 2012. Additional contacts: Jeffrey Spalding, Fermilab, Didier Contardo, Universite Claude Bernard-Lyon I.

[71] Matzner Dominguez, David Aaron and Abbaneo, D. and Arndt, K. and Bacchetta, N. and Ball, A. and Bartz, E. and Bertl, W. and Bilei, G. M. and Bolla, G. and Cheung, H. W. K. and others . CMS Technical Design Report for the Pixel Detector Upgrade. 2012.

[72] N. Demaria. Recent ASICs developments in 65nm CMOS technology for high energy physics experiments. In *2015 IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, pages 380–383, Dec 2015.

[73] N. Demaria, G. Dellacasa, G. Mazza, A. Rivetti, M. D. Da Rocha Rolo, E. Monteil, L. Pacher, F. Ciciriello, F. Corsi, C. Marzocca, G. De Roberts, F. Loddo, C. Tamma, M. Bagatin, D. Bisello, S. Gerardin, S. Mattiazzo,

L. Ding, P. Giubilato, A. Paccagnella, F. De Canio, L. Gaioni, M. Manghisoni, V. Re, G. Traversi, E. Riceputi, L. Ratti, C. Vacchi, R. Beccherle, G. Magazzu, M. Minuti, F. Morsani, F. Palla, V. Liberali, S. Shojaii, A. Stabile, G. M. Bilei, M. Menichelli, E. Conti, S. Marconi, D. Passen, and P. Placidi. CHIPIX65: Developments on a new generation pixel readout ASIC in CMOS 65 nm for hep experiments. In *2015 6th International Workshop on Advances in Sensors and Interfaces (IWASI)*, pages 49–54, June 2015.

[74] E. Monteil, L. Pacher, A. Paternò, N. Demaria, A. Rivetti, M. Da Rocha Rolo, F. Rotondo, C. Leng, and J. Chai. A synchronous analogue very front-end in 65nm CMOS with local fast tot encoding for pixel detectors at HL-LHC. *JINST*, 2016.

[75] L. Ratti, F. De Canio, L. Gaioni, M. Manghisoni, V. Re, and G. Traversi. An asynchronous front-end channel for pixel detectors at the HL-LHC experiment upgrades. In *2015 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, pages 1–5, Oct 2015.

[76] A. Paternò, L. Pacher, N. Demaria, A. Rivetti, G. Dellacasa, S. Marconi, and P. Placidi. New development on digital architecture for efficient pixel readout ASIC at extreme hit rate for hep detectors at HL-LHC. In *2016 IEEE Nuclear Science Symposium, Medical Imaging Conference and Room-Temperature Semiconductor Detector Workshop (NSS/MIC/RTSD)*, pages 1–5, Oct 2016.

[77] G. De Robertis, F. Loddo, S. Mattiazzo, L. Pacher, D. Pantano, and C. Tamma. Design of a 10-bit segmented current-steering digital-to-analog converter in CMOS 65 nm technology for the bias of new generation readout chips in high radiation environment. *Journal of Instrumentation*, 11(01):C01027, 2016.

[78] G. Traversi, F. De Canio, L. Gaioni, M. Manghisoni, L. Ratti, and V. Re. Design of bandgap reference circuits in a 65 nm CMOS technology for HL-LHC applications. *Journal of Instrumentation*, 10(02):C02004, 2015.

[79] L. Pacher, E. Monteil, A. Rivetti, N. Demaria, and M. Da Rocha Rolo. A low-power low-noise synchronous pixel front-end chain in 65 nm CMOS technology with local fast tot encoding and autozeroing for extreme rate and radiation at HL-LHC. In *2015 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, pages 1–4, Oct 2015.

[80] E. Monteil, L. Pacher, A. Paternò, F. Loddo, N. Demaria, L. Gaioni, F. De Canio, G. Traversi, V. Re, L.Ratti, A. Rivetti, M. Da Rocha Rolo, G. Dellacasa, G. Mazza, C. Marzocca, F. Licciulli, F. Ciciriello, S.Marconi, P. Placidi, G. Magazzù, A. Stabile, S. Mattiazzo, and C. Veri. A prototype of a new generation readout asic in 65nm cmos for pixel detectors at hl-lhc. *Journal of Instrumentation*, 11(12):C12044, 2016.

[81] S. Marconi, E. Conti, P. Placidi, J. Christiansen, and T. Hemperek. The RD53 collaboration's systemverilog-uvm simulation framework and its general applicability to design of advanced pixel readout chips. *Journal of Instrumentation*, 9(10):P10005, 2014.

[82] E. Conti, S. Marconi, J. Christiansen, P. Placidi, and T. Hemperek. Simulation of digital pixel readout chip architectures with the RD53 systemverilog-uvm verification environment using monte carlo physics data. *Journal of Instrumentation*, 11(01):C01069, 2016.

[83] S. Marconi, E. Conti, J. Christiansen, and P. Placidi. Reusable systemverilog-uvm design framework with constrained stimuli modeling for high energy physics applications. In *2015 IEEE International Symposium on Systems Engineering (ISSE)*, pages 391–397, Sept 2015.

[84] A. Hsu and Y.C. Wang. 8b/10b encoder, August 1993. EP Patent App. EP19,930,300,821.

[85] L. Pacher et al. Results from CHIPIX-FE0, a small scale prototype of a new generation pixel readout ASIC in 65nm CMOS for HL-LHCs. In *TWEPP 2017 Topical Workshop on Electronics for Particle Physics*, 2017.

[86] R.E. Best. *Phase-Locked Loops*. Professional Engineering. Mcgraw-hill, 2003.

[87] F. Gardner. Charge-pump phase-lock loops. *IEEE Transactions on Communications*, 28(11):1849–1858, Nov 1980.

[88] Textronix. Understanding and characterizing timing jitter, primer, 2005.

[89] Kishishita, T and Krüger, H and Hemperek, T and Lemarenko, M and Koch, M and Gronewald, M and Wermes, N. Prototype of a gigabit data transmitter in 65 nm CMOS for DEPFET pixel detectors at Belle-II. *Nucl. Instrum. Methods Phys. Res., A*, 718(AIDA-PUB-2013-017):168–172, Aug 2013.

[90] P. Leitao, R. Francisco, X. Llopart, F. Tavernier, S. Baron, S. Bonacini, and P. Moreira. The ecdr-PLL, a radiation-tolerant ASIC for clock and data recovery and deterministic phase clock synthesis. *Journal of Instrumentation*, 10(03):C03024, 2015.

[91] G Mazza, Gianluca Aglieri Rinella, F Benotto, Y Corrales Morales, T Kugathasan, Alessandra Lattuca, M Lupi, and I Ravasenga. A 1.2 gb/s data transmission unit in CMOS 0.18 m technology for the ALICE Inner Tracking System front-end ASIC. 12:C02009–C02009, 02 2017.

[92] A. Rao, M. Mansour, G. Singh, C. H. Lim, R. Ahmed, and D. R. Johnson. A 4-6.4 GHz lc PLL with adaptive bandwidth control for a forwarded clock link. *IEEE Journal of Solid-State Circuits*, 43(9):2099–2108, Sept 2008.

[93] J. Prinzie, J. Christiansen, P. Moreira, M. Steyaert, and P. Leroux. Comparison of a 65 nm CMOS ring- and lc-oscillator based PLL in terms of tid and seu sensitivity. *IEEE Transactions on Nuclear Science*, 64(1):245–252, Jan 2017.

[94] J. Craninckx and M. Steyaert. Low-noise voltage-controlled oscillators using enhanced lc-tanks. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 42(12):794–804, Dec 1995.

[95] R. Nonis, N. Da Dalt, P. Palestri, and L. Selmi. Modeling, design and characterization of a new low-jitter analog dual tuning LC-VCO PLL architecture. *IEEE Journal of Solid-State Circuits*, 40(6):1303–1309, June 2005.

[96] M. Kossel, T. Morf, J. Weiss, P. Buchmann, C. Menolfi, T. Toifl, and M. L. Schmatz. Lc PLL with 1.2-octave locking range based on mutual-inductance switching in 45-nm soi CMOS. *IEEE Journal of Solid-State Circuits*, 44(2):436–449, Feb 2009.

[97] S. Voinigescu. *High-Frequency Integrated Circuits*. 2013.

[98] S. S. Mohan, M. del Mar Hershenson, S. P. Boyd, and T. H. Lee. Simple accurate expressions for planar spiral inductances. *IEEE Journal of Solid-State Circuits*, 34(10):1419–1424, Oct 1999.

[99] K. K. Patel et al. Charge pump, loop filter and VCO for phase lock loop using 0.18 um CMOS technology. *IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)*, 2(4):21–25, May-Jun 2013.

[100] M. M. Green and U. Singh. Design of cmos cml circuits for high-speed broadband communications. In *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium*, volume 2, pages II–204–II–207 vol.2, May 2003.

[101] S. Guo, J. Li, P. Gui, Y. Ren, L. Chen, and B. L. Bhuva. Single-event transient effect on a self-biased ring-oscillator PLL and an lc PLL fabricated in sos technology. *IEEE Transactions on Nuclear Science*, 60(6):4668–4672, Dec 2013.

[102] J. Prinzie, M. Steyaert, P. Leroux, J. Christiansen, and P. Moreira. A single-event upset robust, 2.2 GHz to 3.2 GHz, 345 fs jitter PLL with triple-modular redundant phase detector in 65 nm CMOS. In *2016 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pages 285–288, Nov 2016.

[103] Federico Faccio et al. Influence of LDD spacers and h+ transport on the total-ionizing-dose response of 65 nm MOSfets irradiated to ultra-high doses. *IEEE Trans. Nucl. Science accepted for publication*, 2017.

[104] M. Innocent. General introduction to cmos image sensors. *Cypress Semiconductor, Belgium*, 2010.

[105] Peric, Ivan. A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology. *Nucl. Instrum. Meth.*, A582:876–885, 2007.

[106] W. Snoeys, J. D. Plummer, S. Parker, and C. Kenney. Pin detector arrays and integrated readout circuitry on high-resistivity float-zone silicon. *IEEE Transactions on Electron Devices*, 41(6):903–912, Jun 1994.

[107] J.Olave, S.Panati, A. Rivetti, L.Pancheri, F.Cossio, P.Giubilato, D.Pantano, S.Mattiazzo, M.D.Da Rocha Rolo, and N.Demaria. MATISSE: a low power front-end electronics for maps characterization. In *TWEPP*, Sept 2017.

[108] Marc Poizat. Total ionizing dose mechanisms and effects, 2009. EPFL Space Center.

[109] James F. Salzman. Total ionizing dose (tid) and single event effects (see) test report, 2013. Texas Instruments.

[110] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet, and V. Ferlet-Cavrois. Radiation effects in MOS oxides. *IEEE Transactions on Nuclear Science*, 55(4):1833–1853, Aug 2008.

[111] EASA (European Aviation Safety Agency). Certification memorandum: Development assurance of airborne electronic hardware. EASA CM No.: EASA CM -SWCEH - 001 Issue No.: 01 Issue Date: 11 of August 2011.

[112] Open Standards. Openpdk project: Openpdk coalition introduction, 2010.

[113] Silvaco. Silvaco process design kit, 2015.

[114] Perl. Perl 5, 2010.

[115] Shell Scripting. Bourne shell scripting tutorial, 2017.

[116] Open Cores Coding Guidelines. Bourne shell scripting tutorial, 2009.

[117] D. B. Leeson. A simple model of feedback oscillator noises spectrum. In *Proceeding IEEE*, volume 54, pages 329–330, 1966.

[118] A. Hajimiri and T. H. Lee. A general theory of phase noise in electrical oscillators. *IEEE Journal of Solid-State Circuits*, 33(2):179–194, Feb 1998.

[119] T. H. Lee and A. Hajimiri. Oscillator phase noise: a tutorial. *IEEE Journal of Solid-State Circuits*, 35(3):326–336, March 2000.