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(Article begins on next page)

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A Sub-Leakage pW-Power Hz-Range Relaxation Oscillator Operating with 0.3V-1.8V Unregulated Supply

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Abstract

A pW-power versatile relaxation oscillator operating from sub-threshold (0.3V) to nominal voltage (1.8V) is presented, having Hz-range frequency under sub-pF capacitor. The wide voltage and low sensitivity of frequency/absorbed current to the supply allow the suppression of the voltage regulator, and direct powering from harvesters (e.g., solar cell, thermal from machines) or 1.2-1.5V batteries. A 180nm testchip exhibits a frequency of 4 Hz, 10%/V supply sensitivity at 0.3-1.8V, 8-18pA current, 4%/°C thermal drift from -20°C to 40°C.

Introduction

Slow oscillators are key building blocks used to periodically wake up sensor nodes with low duty cycle [1]. The energy source voltage V_{DD} is typically highly variable, due to the large fluctuations in the harvested power and/or battery charge (Fig. 1). Being always on, the oscillator power consumption needs to be as low as possible, reaching the sub-nW range down to pWs in recent relaxation oscillators [1]-[6].

Oscillators in prior art usually have a strict requirement on voltage regulation to mitigate frequency variations and rapid power consumption increase at the cost of additional regulator power, which is invariably not accounted for in the oscillator evaluation [1]-[6]. Such oscillators operate either at near- or above-threshold voltages [4]-[6], and in a narrow voltage range (e.g., 50-100mV wide [1]-[3], [6]). For applications that impose accuracy over large temperature fluctuations, temperature compensation is introduced at the cost of additional power [2]-[4], which can be saved whenever the temperature is naturally restricted to a limited range (e.g., in indoor sensing, biomedical/implantable devices).

In this work, the first relaxation oscillator able to operate from sub-threshold to nominal voltage at pW power and Hz-range frequency is presented. The low sensitivity of frequency and supply current to V_{DD} permits to eliminate the voltage regulator, powering the oscillator directly with the harvester or battery (or drastically relaxing its design), while maintaining similar frequency and power consumption.

Proposed Relaxation Oscillator

The proposed oscillator is based on the novel digital architecture in Fig. 2a, with cells designed in dynamic leakage suppression (DLS) logic style (Fig. 3) [7]. DLS gates enable operation down to 0.3V, nearly-independent of V_{DD} and very low average transistor ON current I_{DLS} (~3pA/gate in 180nm), and thus slow operation with small capacitance *C*, sub-leakage overall power consumption, due to super-cutoff transistor operation [7]. DLS exhibits hysteretic behavior, with low (high) input threshold $V_{DLS,L}$ ($V_{DLS,H}$) equal to 75mV (250mV) at V_{DD}=0.4V, which is weakly dependent on V_{DD} [7] (Fig. 3).

The A and B terminals of the capacitor *C* in Fig. 2a drive the DLS inverters with hysteresis G1a-b, and are driven by the outputs $\bar{Q}$ and Q of the latch G3a-b, which is loaded by the gates G4a-b with short-circuited input/output (which act like inverters, once $ENABLE$ is asserted in Fig. 2b). The size ratio of G3a-b and G4a-b sets the high (low) DC voltage $V_{AB,H}$ ($V_{AB,L}$) of v_A and v_B, which is equal to 275mV (32mV) under minimum-sized gates and V_{DD}=0.4V (see Fig. 4).

Assuming that $\bar{Q}$ is high (Q is low) at the beginning of a period (t_0 in Fig. 2b), $v_A = V_{AB,H}$ since G3a is pulling $\bar{Q}$ high and is loaded by G4a (see above), whereas $v_B = V_{MAX} > V_{AB,H}$ from the end of the previous period (see evaluation below). Since the output Q of G3b is low, v_B is pulled down by the DLS gate G3b, which draws a small (~3pA) and nearly supply-independent current I_{DLS} that discharges *C*. During this transient, v_B drops down until it crosses the switching threshold $V_{DLS,L}$ of G1b (t_1 in Fig. 2b). At this point, the capacitor voltage is $v_C = v_A - v_B = V_{AB,H} - V_{DLS,L}$. When v_B crosses $V_{DLS,L}$, the inverting behavior of G1b, G2b and G3b pulls Q high, raising v_B to $V_{AB,H}$ (t_2 in Fig. 2b). As *C* maintains the same voltage $v_C = V_{AB,H} - V_{DLS,L}$ before/after the transition, $v_A = v_B + v_C$ is pulled up from $V_{AB,H}$ to $V_{MAX} = V_{AB,H} + (V_{AB,H} - V_{DLS,L}) > V_{AB,H}$. At this point, a semi-period *T*/2 is completed, and a new semi-period with inverted signals starts (same as above, swapping Q and $\bar{Q}$, v_A and v_B).

Full-swing output OUT is generated by the G2a-b latch, and is a square wave with nearly 50% duty cycle and period $T \approx 4C(V_{AB,H} - V_{DLS,L})/I_{DLS}$ (constant-current discharge of *C*, see Fig. 2b). *T* has low sensitivity to the supply voltage since $V_{AB,H}$, $V_{DLS,L}$ and I_{DLS} are weakly supply-dependent in DLS logic [7] (see also Figs. 3-4). The power consumption is dominated by the static sub-leakage current drawn by transistors, which is again rather insensitive to V_{DD} in DLS logic [7].

Testchip and Measurement Results

The oscillator was demonstrated with a 180nm testchip (Fig. 5a). The area of 10,000 μm^2 is the second smallest among [1]-[6]. Not being temperature-compensated, the frequency shows a mean thermal drift of 4%/°C from -20°C to 40°C (Fig. 5b), which is comparable to [5] and expectedly higher than temperature-compensated oscillators [2]-[4].

Measurements of five dice showed that the proposed oscillator is the only one that can operate from deep sub-threshold (0.3V) to nominal voltage (1.8V) from Figs. 5-6. Across five dice, the frequency ranges from 3.36Hz to 4.28Hz (average 4Hz) at 25°C and 0.4V, the supply current ranges from 7.3pA to 9.5pA, and the power ranges from 2.9pW to 3.7pW (average 3.32pW, Fig. 5c), which is the lowest reported to date (Fig. 6).

Further power advantage over [1]-[6] is achieved when the power required by the voltage regulator is fairly taken into account in [1]-[6], considering that no voltage regulation is instead needed in the proposed oscillator. This is because the latter operates from 1.8V down to 0.3V, with a low frequency sensitivity to supply voltage of 10%/V (Fig. 5d). This is the second best voltage sensitivity after [4], which instead requires an additional regulated supply and a current reference. Also, the supply current (Fig. 5c) has minor increase from 8pA to 18pA, when varying V_{DD} from 0.3V to 1.8V (Fig. 5c).

Thanks to its pW power, Hz-range, frequency/power insensitivity to V_{DD} in a wide range, and low area, the proposed oscillator is well suited for low-cost low-power sensor nodes.

Acknowledgements

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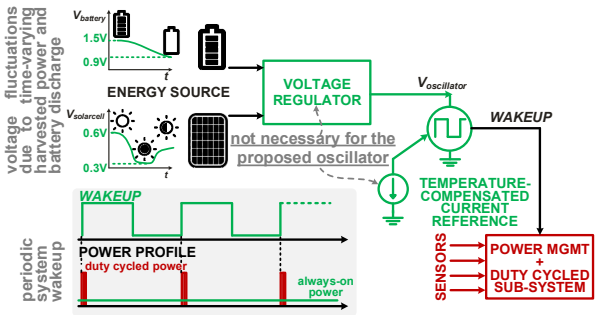


Fig. 1. Duty-cycled sensor node with slow oscillator for system wake-up.

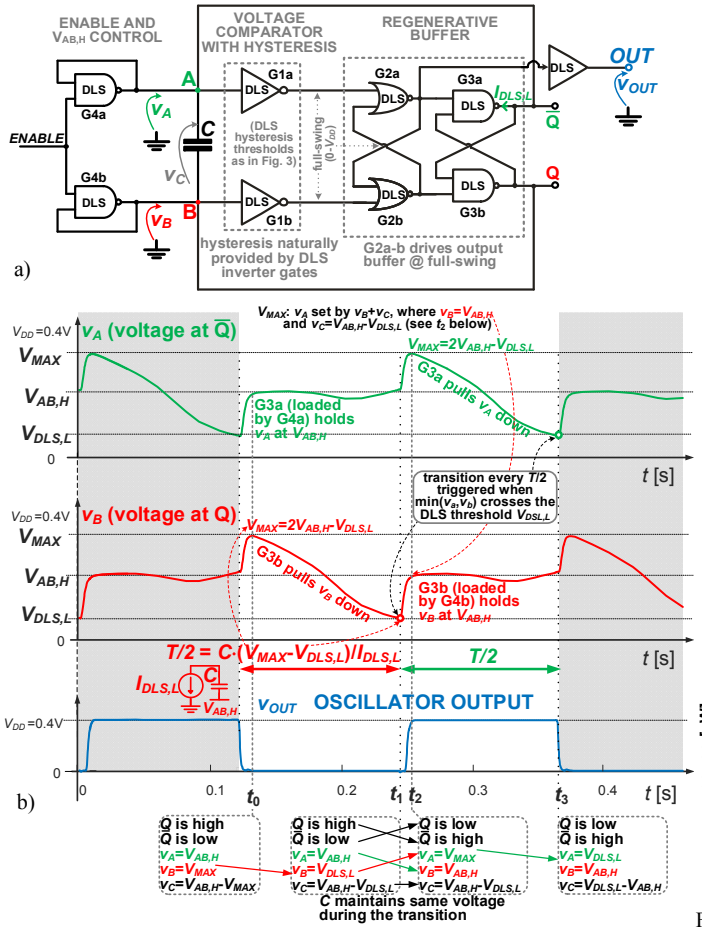


Fig. 2. a) Proposed oscillator architecture based on DLS logic in Fig. 3 (all minimum-sized transistors), b) waveforms and period evaluation.

References

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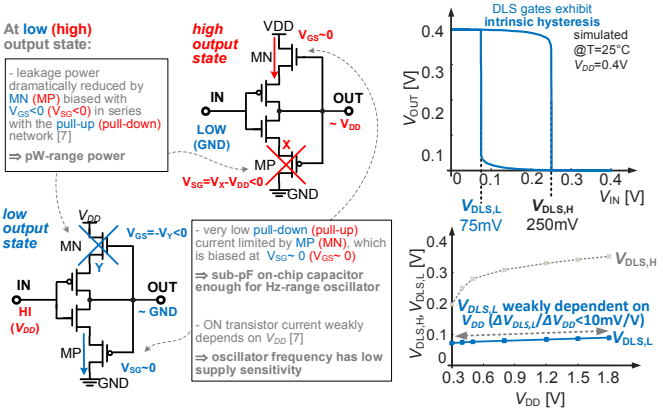


Fig. 3. Inverter in Dynamic Leakage Suppression (DLS) logic style used in all standard cells in Fig. 2a, and properties exploited in the proposed oscillator.

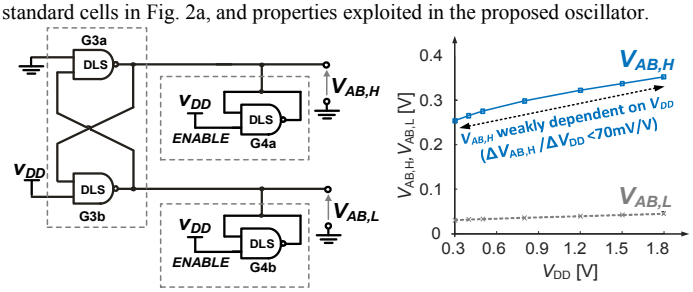


Fig. 4. a) DLS latch G3a-b loaded with gates G4a-b having short-circuited input/output, b) resulting $V_{AB,H}$ and $V_{AB,L}$ vs. V_{DD} (showing weak dependence).

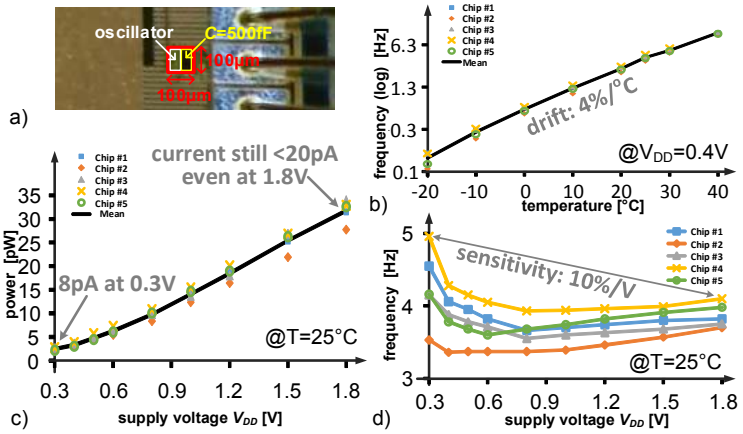


Fig. 5. Measurements of five samples of the proposed oscillator: a) testchip micrograph, b) output frequency vs. temperature @V_{DD}=0.4V, c) power consumption vs. V_{DD} @T=25°C, d) output frequency vs. V_{DD} @T=25°C.

	Lin CICC07 [1]	Lin ISSCC09 [2]	Lee JSSCC13 [3]	Jeong JSSC15 [4]	Nadeau JSSC16 [5]	Wang JSSC16 [6]	this work
oscillator principle	gate leakage	program & hold	gate leakage	relaxation	program & hold	capacitor discharge	DLS logic
technology	130nm	130nm	130nm	180nm	180nm	65nm	180nm
area (µm²)	**480**	19,000	15,300	240,000	N/A	25,500	10,000
supply voltage [V]	0.45	0.6	0.7 (1.2 for VDDH)	1.2	0.6	0.5	**0.4**
frequency [Hz]	0.09	11.11	0.37	11	18	2.8	4
power [pW]	120	150	660	5,800	4.2	44.4	**3.32**
frequency variability (process)	28%	N/A	N/A	N/A	N/A	11.8%	8.9%
voltage range [V]	0.4 to 0.5	0.55 to 0.65	0.65 to 0.75	1.2 to 2.2	NA	0.48 to 0.52	**0.3 to 1.8**
supply sensitivity [%/V]	150	60	420	**1**	240	160	10
temperature range [°C]	0 to 80	0 to 90	-20 to 60	-10 to 90	-30 to 60	-40 to 60	-20 to 40
thermal drift [%/°C]	0.16	0.049	**0.0031**	0.0045	2	0.126	4
frequency shift due to 10% voltage, 5°C temperature change	7.55%	3.85%	29.42%	**0.14%**	24.4%	8.63%	21%
voltage regulator (current reference) requirement	YES (NO)	YES (YES)	YES (NO)	YES (YES)	YES (YES)	YES (NO)	**NO (NO)**

Fig. 6. Relaxation Hz-range oscillator performance comparison (best performance in bold).