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Application of spread-spectrum techniques to class-E DC/DC converters: some preliminary results

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***Abstract*—Spread spectrum clocking (SSC) has recently emerged as a very effective solution to mitigate electromagnetic interference (EMI) issues. In last years it has been widely used in switching dc/dc converters, in particular in class-D ones, i.e., that based on pulse-width modulation. Conversely, it finds no application in resonant ones. Within this paper we investigate the effects of applying SSC techniques to a recently introduced resonant class-E converter. Intensive SPICE simulations using both basic and advanced SSC techniques show not only that SSC is effective in mitigating EMI issues in this class of converters, but also that the most important circuit figures of merit such as conversion efficiency are not affected.**

I. Introduction

The electromagnetic interferences (EMI) reduction in clocked circuit such as switching power converters is of great practical concern. In particular, *design-time* solutions have to be adopted [1] whenever *a-posteriori* methodologies, such as filtering or shielding, cannot be employed since they may not ensure the required reduction, or simply since they may be not economically convenient. The basic idea in the former solutions is to introduce an intentional *jitter* in the reference clock by slightly *delaying* or *anticipating* clock edges, in this way a perfect periodicity is avoided, thus reshaping the power spectrum from a delta-like function to a wide-band spectrum, and reducing the power spectrum peak level. This technique is known as *spread-spectrum* clocking (SSC), and is perfectly coherent with international regulations [2], [3], which link compliance with the ability of fitting the interfering power spectrum within a prescribed mask. Classical spread-spectrum techniques exploit triangular [4], [5] or periodic [1] waveforms, while most advanced techniques [6] may rely on random sequences [7] with good statistical properties [8].

In recent years, SSC techniques have been found of particular interest for switching dc/dc converter circuits, that are a preeminent source of EMI due to their high-power commutations that generate a large-amplitude interfering spectrum. In particular many literature works [4], [6], as well as many commercial solutions [9], [10], propose to apply SSC techniques to class-D switching dc/dc converters, i.e., that based on pulse-width modulation (PWM) control signal, with remarkable advantages from the point of view of EMI reduction and almost no disadvantages in terms of converter performance reduction [6].

However, only a very few works [5, and references therein] propose to apply these techniques for EMI reduction in high-frequency resonant converters. The main reason is that here, differently from the PWM case, the switching frequency f_c is a fundamental design parameter, since all circuit elements are resonating at f_c. Avoiding perfect periodicity by introducing intentional jitter results in a deviation of the instantaneous converter oscillation frequency with respect to its nominal value. The converter is not operating anymore in its optimum working point, and this increases circuit loss or even prevents the correct converter behavior.

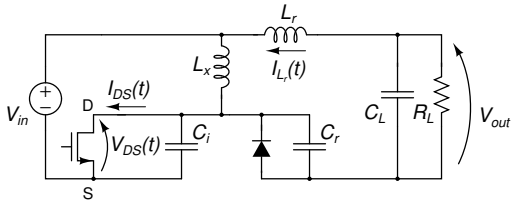

Fig. 1. Schematic of the analyzed class-E resonant dc-dc converter taken from [11].

In this paper, by means of intensive SPICE simulations, we investigate the effect of applying SSC technique to a resonant converter recently introduced in [11]. In detail, we focus on the class-E converter whose schematic is depicted in Fig. 1. This circuit exploits the so called *soft-switching* technique in order to reduce the switching losses. Conversely from class-D switching converters characterized by rectangular waveforms, class-E ones embed a resonant circuit that, roughly speaking, shapes the drain/source voltage $V_{DS}(t)$ and the drain current $I_{DS}(t)$ of the MOS switch in a sinusoidal-like way, synchronizing the zero-crossing instants of $V_{DS}(t)$ and $I_{DS}(t)$ with the turn-on instant of the MOS switch. These approaches are known, respectively, as zero-voltage switching (ZVS) and zero-current switching (ZCS), and they are used to reduce the voltage-current product of the MOS at the switching instants, thus lowering (ideally, down to zero) the energy-loss-per-cycle, reducing the device stress and relaxing the constraints on the switch turn-on and turn-off response times. This allows to increase the switching frequency up to the the VHF range (30-300 MHz) [12]; however, the operation point is extremely sensitive to the oscillation frequency, and the application of SSC techniques may results in an unpredictable outcome.

By exploiting the innovative design procedure described in [11], we have designed a $1\,\mathrm{W}$ class-E converter with $V_{in} = V_{out} = 5\,\mathrm{V}$ as case study. At the nominal frequency $f_c = 1\,\mathrm{MHz}$ the converter has a 0.835 efficiency, while the observed output ripple normalized by the output voltage is equal to the $8 \cdot 10^{-4}$. Then, we have investigated the converter behavior when driving the main MOS switch using both classical (i.e., triangular-based) and advanced (chaos-based) SSC techniques. Results show that EMI are effectively reduced, while all most

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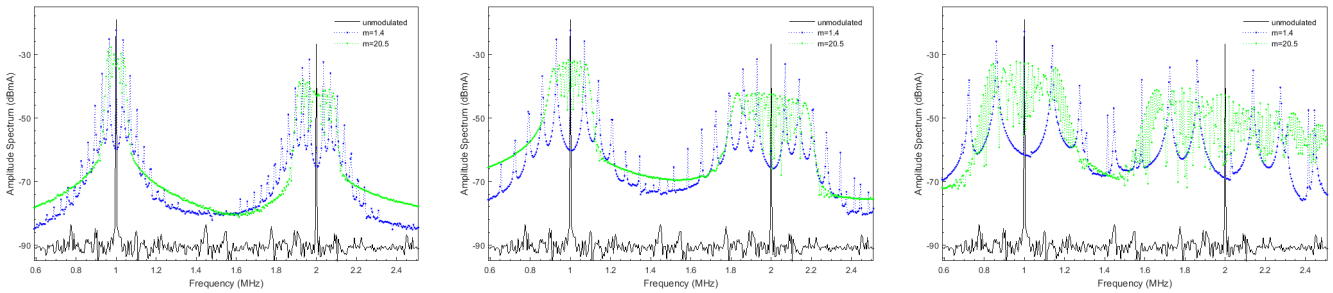

(a) (b) (c)

Fig. 2. Output power spectra of the converter of Fig. 1 when applying triangular-based SSC for three different values of Δf. (a): $\Delta f/f_c = 0.05$; (b): $\Delta f/f_c = 0.1$; (c): $\Delta f/f_c = 0.2$.

important converter figures of merit are almost not affected.

The paper is organized as follows. In Section II we investigate the converter behavior when a standard triangular-based SSC is used. Then, in Section III we use the more advanced chaos-based SSC proposed in [6] to see if converter performance can be increased. Finally, we draw the conclusion.

II. Basic SSC Techniques

SSC is usually achieved by means of a frequency modulation of the reference clock signal. More formally, and limiting ourselves to the first harmonic $s(t)$ of the clock, one has

$$s(t) = A_0 \cos\left(2\pi f_c t + 2\pi\Delta f \int_{-\infty}^{t} \xi(\tau)d\tau\right) \qquad (1)$$

where Δf is known as frequency deviation and $-1 \leq \xi(t) \leq 1$ is the (normalized) driving signal. For higher harmonics the model is similar, with the only difference that the nth harmonic is spread within a bandwidth that is n-times larger.

Despite the fact that many different solutions have been proposed, the most common one is given by generating $\xi(t)$ as a triangular waveform with period T. The advantage of this approach is that, assuming that the modulation index $m = \Delta f\, T$ is large enough, the spectrum of (1), despite being actually discrete, looks like continuous and approximately flat in $[f_c - \Delta f, f_c + \Delta f]$. Higher harmonics have similar behavior, and this represents the optimum in terms of EMI reduction since no peaks in the power spectrum are present.

In order to apply this technique to the class-E converter of Fig. 1, it is enough to drive the MOS switch with the modulated clock signal instead of using the reference one. By means of SPICE simulations, we can show in Fig. 2 the output power spectrum of the current I_{L_r} when the converter is working in this configuration, for different values of m (i.e., of T) and of Δf. The spectrum in the figure has been computed by means of the periodogram technique using a 5 kHz frequency resolution. We have focused on the I_{L_r} current since inductors are expected to be the most prominent source of EMI in a switching converter [4], so the overall EMI spectrum will be strongly related to the I_{L_r} power spectrum. Yet, all other waveforms in the circuit presents a power spectrum very similar to the considered one.

The observed power spectra are aligned with the expected ones according to the SSC classical theory: they are discrete, but look like continuous for large m, i.e., in the *slow modulation* case. Furthermore, the peak reduction with respect to the unmodulated case is increasing with Δf, since the energy is spread over a larger bandwidth.

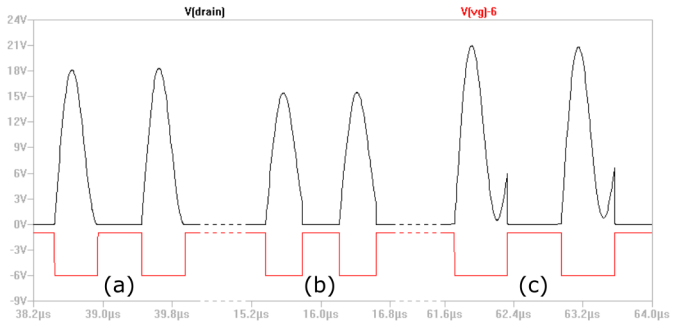

Fig. 3. When oscillating at the correct switching frequency f_c (a), the resonant converter features ZVS, i.e., the MOS is turned ON by its control clock signal (bottom plot) when $V_{DS}(t)$ (top plot) naturally reaches zero. When applying SSC, this does not happen, and the MOS may be turned ON too early (b) or too late (c).

Once that a correct behavior in terms of EMI reduction is established, many other converter figures of merit must be verified. As already anticipated, the main issue is given by the fact that resonant converters are designed to operate at a well defined switching frequency, and a small change in it may not ensure the optimal working point, or even prevent the correct converter behavior. As an example, the waveforms of Fig. 3 plots some chunks of the MOS switch drain/source voltage in a long simulation with $\Delta f/f_c = 0.2$. When the instantaneous switching frequency is the correct one as in case (a), the converter features ZVS, i.e., the MOS is turned ON when $V_{DS}(t)$ voltage (top plot in the figure) naturally reaches zero. However, when applying SSC, the instantaneous switching frequency is continuously changed by $\xi(t)$, and ZVS may be not always ensured. The MOS may be turned ON too early as in case (b), or too late as in case (c). Even if a non-perfect ZVS is usually tolerated, this reduces converter performance.

In order to evaluate the effect of SSC on the class-E converter, we focus on four (normalized) converter figures of merit:

- EMI reduction, defined as the peak level of the SSC power spectrum normalized by the peak level of the unmodulated one. The lower the observed peak level, the higher the EMI reduction. Note that in the large majority of cases, both peak levels are generated by the

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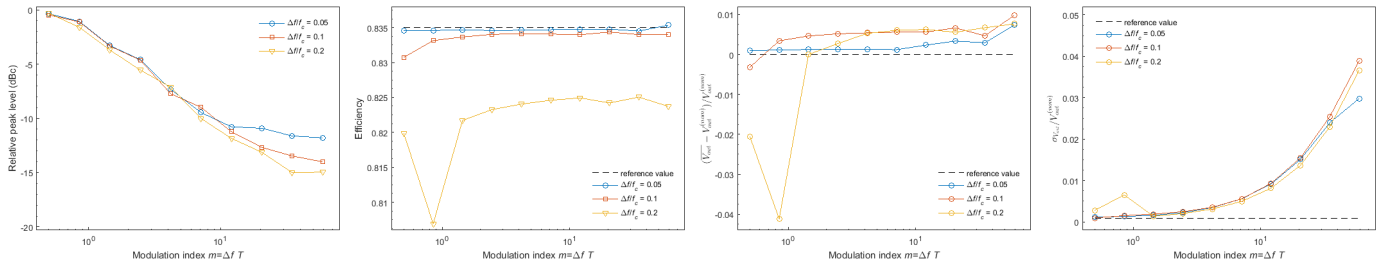

(a) (b) (c) (d)

Fig. 4. Figures of merit for the class-E converter when applying triangular-based SSC for different values of Δf and m. (a): EMI reduction; (b): efficiency; (c): output voltage deviation; (d): output voltage ripple.

first harmonic;

- the converter efficiency, defined as the ratio between the average output power and the average total input power;
- the deviation of the mean value $\overline{V_{out}}$ of the output voltage with respect to the nominal value $V_{out}^{(nom)} = 5\,\mathrm{V}$, defined as $\left(\overline{V_{out}} - V_{out}^{(nom)}\right)/V_{out}^{(nom)}$;
- the normalized converter output ripple, defined as the output voltage standard deviation $\sigma_{V_{out}}$ divided by $\overline{V_{out}}$.

These figures of merits for different values of Δf and m have been plotted in Fig. 4 and can be commented as follows.

The EMI reduction, plotted in (a), is increasing with m, up to a saturation value for large m indexes. Furthermore, this saturation level is increasing with Δf. This is actually the behavior predicted and observed in [4] when applying classic SSC to PWM converters. Note that Fig. 4(a) is the same as [4, Fig. 4]

Conversely, the converter efficiency, plotted in (b), is almost independent of m, but it is strongly dependent on Δf. With $\Delta f/f_c = 0.05$ or $\Delta f/f_c = 0.1$, there are no remarkable differences with the efficiency of the unmodulated converter (dashed line), but for $\Delta f/f_c = 0.2$, the converter efficiency is strongly reduced. This is due to the large changes in the instantaneous switching frequency, as observed in the example of Fig. 3. Efficiency is also reduced when m is small, i.e. for *fast* modulations.

Surprisingly, the effect on the average output voltage is very limited, as shown in plot (c), and the normalized deviation from the nominal output level (dashed line in the figure) is always limited, except for small values of m. As for previous figures of merit, also here slow modulations are preferred.

Finally, the output ripple shown in (d) is almost independent of Δf, but strongly increasing with m. From the output ripple point of view, the converter suffers slow modulations. This can be explained with the fact that, for large m, the converter have enough time to settle to a new stable operating point, significantly altering the output voltage.

Based on the above observations, the standard SSC technique can be effectively applied to the considered resonant converter when intermediate values of m and of Δf are used, thus either allowing a good EMI reduction without altering the overall converter performance.

III. Advanced SSCG Techniques

With the aim of improving converter performance, we apply the more advanced SSC technique suggested in [6]. In more details, i.e., we replace the triangular driving signal with the pulse amplitude modulated (PAM) signal

$$\xi(t) = \sum_k x_k g(t - kT_s) \tag{2}$$

where $g(t)$ is a rectangular pulse of duration T, and the sequence $\{x_k\}$ comes from a chaotic map, that is a 1D discrete-time autonomous systems, whose evolution is described by:

$$x_{k+1} = M(x_k), \quad M : \{-1, 1\} \mapsto \{-1, 1\} \tag{3}$$

where M is properly designed a non-linear function [13]. The main property of chaotic maps is their strong dependence on the initial condition: two trajectories starting from two very close initial conditions appear, after few steps, as completely uncorrelated. This guarantees unpredictability in true-implemented systems, where the system state x_k is known only with finite precision. The property which makes these system suitable for EMI reduction is to generate non periodic trajectories, which ensure a *continuous* power spectrum of $s(t)$ and of all the clock harmonics.

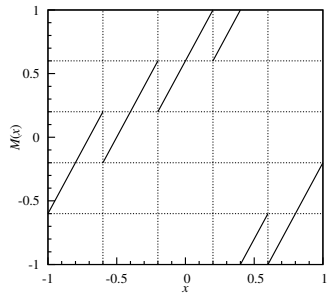

Fig. 5. M function of the chaotic map proposed in [6].

In particular, following [6], we use the update function M depicted in Fig. 5. The statistical properties of the $\{x_k\}$ sequences generated by this map ensure high performance in terms of EMI reduction in many different measurement conditions.

A few examples of the output power spectra of the inductor current I_{L_r} are depicted in Fig. 6. The advantage of a continuous spectrum is clear, since no peaks are present at all. Indeed, this is the optimal condition for EMI reduction purposes.

When computing the four converter figures of merit as in the previous case, we get the four plots of Fig. 7. The behavior of the converter is almost the same as in the standard triangular based SSC case, with the only remarkable difference that EMI

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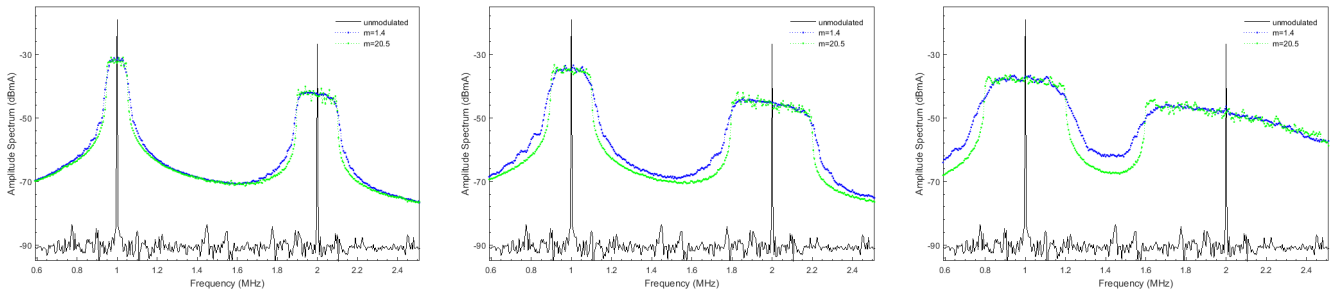
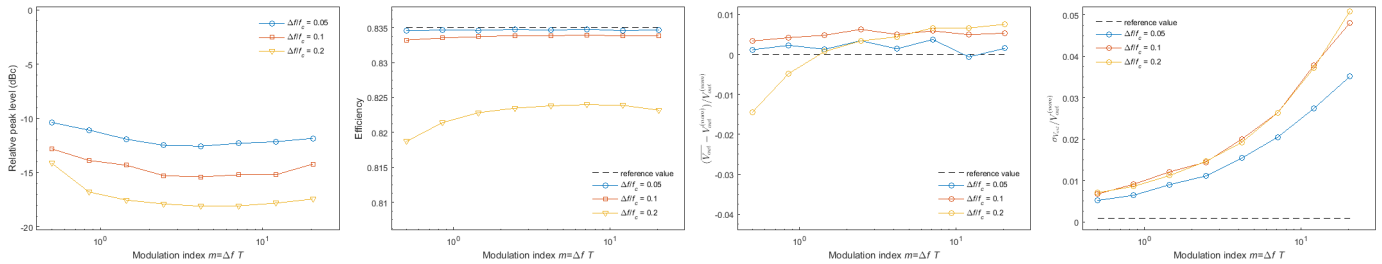


(a) (b) (c)

Fig. 6. Output power spectra of the converter of Fig. 1 when applying chaos-based SSC for three different values of Δf. (a): $\Delta f/f_c = 0.05$; (b): $\Delta f/f_c = 0.1$; (c): $\Delta f/f_c = 0.2$.



(a) (b) (c) (d)

Fig. 7. Figures of merit for the class-E converter when applying chaos-based SSC for different values of Δf and m. (a): EMI reduction; (b): efficiency; (c): output voltage deviation; (d): ripple.

reduction is much higher and almost independent on m, as can be seen in Fig. 7(a). It is known, in fact, that EMI reduction in SSC systems based on chaos, for sufficiently large m (that usually means $m > 1$, see [6] and references therein), depends only on the ratio between Δf and the frequency resolution of the spectral analysis. The higher the Δf, the higher the EMI reduction.

The conclusion is that also the considered advanced SSC technique can be conveniently applied to the resonant class-E converter of Fig. 1. In order to achieve the best performance, an intermediate values of both m and Δf are recommended as in the previously considered triangular based case. In this way, it is possible to get a high EMI reduction (by using Δf not too low) and a limited ripple (by using m not too low), with negligible effects on output voltage deviation and output voltage ripple. In the case considered in this paper, the values that appear to be the the optimal ones are $\Delta f/f_c = 0.1$ and m equal to a few units.

IV. Conclusion

In this paper, the effects of applying SSC techniques to a resonant class-E converter have been investigated. The interest is motivated by the fact that, even though SSC techniques are quite commonly applied to PWM based class-D converters, they are not used in resonant converters. By means of intensive SPICE simulations we can show that using the standard triangular based approach with intermediate values for Δf and m, SSC can be successfully applied to the converter, ensuring the same converter performance as in the unmodulated case, and offering EMI reduction. When using a more advanced SSC technique based on chaos, we can even increase EMI reduction without additional costs in terms of converter performance degradation.

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