A pNML Compact Model Enabling the Exploration of 3D Architectures

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G. Turvani, F. Riente, E. Plozner, M. Vacca, M. Graziano and S. Breitkreutz-v. Gamm

***Abstract*—In Nano Magnetic Logic (NML), single-domain nanomagnets enable logic operations. Binary information can be encoded thanks to its bistable magnetization. Many implementations are currently discussed in literature, among them one promising candidate is perpendicular-Nano Magnetic Logic (pNML). It features several advantages like the controllability of the switching mechanism, the simplicity of design and the natural predisposition of being integrated in 3D architectures.**

Here we show how this technology can be adopted in the design of 3D logic architectures. Physical equations and quantities have been gathered from experimental demonstrations of pNML devices; formulas have then been fitted and implemented in VHDL (VHSIC Hardware Description Language). In this paper we present an analysis of pNML circuits: initially a Multiplexer has been manufactured and characterized, then our compact model has been tested through simulations. Moreover, the MUX has adopted to design a generic n-bit accumulator.

Our results demonstrate that the compact model makes it possible to perform fast simulations, while maintaining a fine level of accuracy. Thanks to its flexibility, novel materials, geometric variations and other technological improvements can be easily integrated in order to be tested at circuit level. We anticipate our essay to be a starting point for the exploration of large 3D digital circuits.

***Index Terms*—perpendicular Nano Magnets Logic, pNML, 3D Architecturs, Innovative Technology**

I. Introduction

According to the International Technology Roadmap of Semiconductors [1], CMOS technology is rapidly reaching its technological end economical limits. Among emerging technologies currently under investigation, Nano Magnetic Logic (NML) [2] based devices seem to be very promising [3]. NML belongs to the so-called beyond-CMOS technologies, where information transportation is accomplished through magneto-dynamic interactions among devices. Different implementations have been studied in recent years, two of the most interesting being in-plane Nano Magnetic Logic (iNML) [4] [5] and perpendicular Nano Magnetic Logic (pNML) [6].

The main characteristics of this technology are the non-volatility of stored information, the possibility to store binary information, the absence of interconnections and the possibility of being integrated with standard CMOS technology. iNML rectangular-shaped nanomagnets (depicted in Fig. 1.A), with typical dimensions of (50x100)nm, are placed side-by-side creating wires and logic devices [7] [8] . Indeed, the coupling-field acting among neighboring cells makes it possible to transfer a magnetic charge according to the ferromagnetic and antiferromagnetic interaction. The maximum limit of iNML elements which can be cascaded is limited to 4/5 because of physical non-idealities like thermal noise etc For this reason, logic circuits must be divided into clock zones, in which the maximum number of cells is limited. Furthermore, information is propagated among different clock zones according to a multiphase clocking system [9].

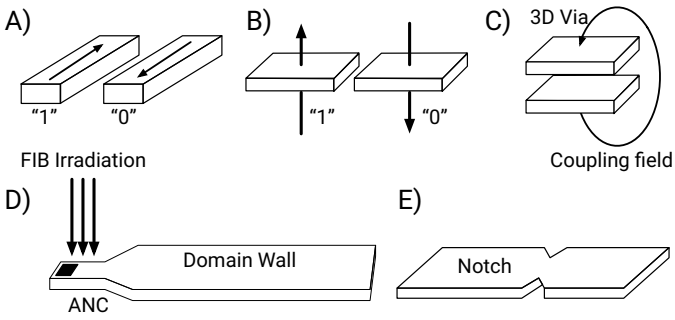

Figure 1. A) iNML cells. Logic status is encoded in the planar magnetization B) pNML cells. Logic status is encoded in the perpendicular magnetization C) 3D Via for vertical interconnections D) ANC creation through spotted FIB irradiation. This definies a univocal propagation directionality. E) Memory element.

pNML (Fig. 1.B) overcomes this limitation thanks to its intrinsic physical properties. Here, only one clock signal is applied to the whole circuit [10] [11]. This has a remarkable impact in terms of circuit compactness and also simplifies the design process. There are several improvements introduced by this implementation: the switching mechanism is tunable through the manufacturing process, the propagation direction of signals is controllable and it can be adopted in monolithic 3D structures [12] (Fig. 1.C). In pNML technology, single domain nanomagnets with perpendicular magnetic anisotropy are used. Two stable magnetization states are possible, which encode the binary values 1 and 0.

However, to guarantee the signal flow directionality, one side of the magnet should be more sensitive to magnetic field changes. This highly-sensitive region is called artificial nucleation center (ANC) and it is obtained by a partial Focus-Ion-Beam (FIB) irradiation as shown in Fig. 1.D, [6]. Hence, signal propagation is achieved in two steps: i) the domain wall nucleation in the ANC and ii) its subsequent motion. As shown in Fig. 1.D, the magnet is partially irradiated on the left side entailing a reduction of the switching field. Only a magnet placed nearby the ANC can influence the

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magnetization defining a univocal propagation direction [13].

Logic computation is performed by means of basic pNML gates inverters and majority voters as experimentally demonstrated in [10]. Signal synchronization can be achieved by controlling domain wall (DW) propagation. Geometrical deformations (Fig. 1.E) in the magnetic nanowire (notches) make it possible to block the propagating information. However, to restore the information flow, short in-plane field pulses can be used [14]. Usually, they are generated by a buried wire placed just below the magnetic notch. In addition, this technology enables the fabrication of monolithically 3D-integrated devices, as demonstrated in [12]. The first structures have been already experimentally demonstrated [6], then, several micromagnetic simulations have been performed in order to study the physical and logic behavior of such devices. Nevertheless, micromagnetic simulators require very high computational costs and consequently, a lot of time is required to simulate larger circuits. Different models have been presented to perform lighter simulations. One of the most interesting has been presented in [15] and it is implemented in Verilog-A. This model enables the reduction of the simulation time but has a lack of flexibility when considering the description of complex architectures. Here, we present our physical compact model entirely developed in VHDL (VHSIC Hardware Description Language) and able to perform very fast simulations of logic architectures, while preserving a fine level of accuracy. From a methodological point of view, several experiments have been carried out in order to characterize pNML devices. Initially, a complete study of characterization has been pursued, then, physical data has been extracted and fitted into equations. A detailed description of this model will be given in Sec. II. The novelty of this model lies in the ability to enable fast simulations of complex logic architectures.

With this paper we validate our compact model by presenting how the physical equations have been fitted from experiments. As benchmarks, we choose to report the simulation results obtained with the architectures of a Multiplexer and an Accumulator. Both circuits have been described completely in VHDL with a generic bit parallelism. These circuits must be understood as samples aiming to verify the validity of the presented model. Notwithstanding, exactly the same approach can be applied to circuits of any complexity.

Experiments on 3D integration of pNML devices are currently carried on; with our approach it is possible to test multilayered circuits with very low computational costs. Furthermore, since the model is organized in libraries containing technological quantities and physical equations, it is possible to test circuits by changing any parameter (like geometry, materials).

II. The Model

To characterize complex architectures, a compact model has been implemented using the hardware description language VHDL. It gives a full characterization of the analyzed circuit mixing the description of the switching behavior and all the physical and technological features which characterize pNML technology. From an implementation point of view, with this new model, pNML devices are divided into a few elementary blocks characterized by different functionalities. In this way, circuits of any complexity can be composed using a library of elementary components.

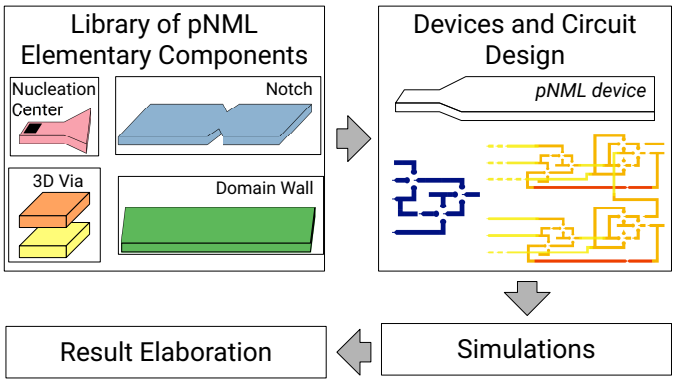

Figure 2. Proposed methodology: the model of basic pNML elements is implemented into a VHDL library. The combination of those components is used to design pNML devices, and then architectures. Circuits can be tested through standard VHDL simulators.

In order to implement the compact model, several physical parameters must be taken into account: geometry, material chosen for the realization of the magnetic layers and delay parameters such as the nucleation time and the propagation time. Indeed, the focus is on the nucleation time and thus also on the probability of being nucleated the current domain wall, and on the propagation time, both of which are used to define the duration of the clocking pulse. In order to implement the model, two packages have been created. The first one includes the main physical quantities which characterize pNML devices. Beyond that, different formulas have been conceived in order to recreate the switching behavior of the ANC and the propagation along the DW. The second package defines the specific functionality of each elementary block needed to realize circuits.

The flexibility of this model resides in its intrinsic ability to be adapted by simply modifying the library parameters. This represents a key point in the study of complex logic architectures. Now it is possible to obtain fast simulations of pNML circuits exploring how small modifications of physical quantities (like geometry) can have a remarkable impact on the performance of pNML circuits. Furthermore, the investigation of geometric deformations such as notches, is always becoming always more attractive since they can be used to design innovative memories. Herein the description of each elementary block follows.

A. Nucleation Center

The creation of a Domain Wall (DW) starts with the nucleation of the magnetic structure in correspondence with the ANC. This irradiated spot enables the control of the switching properties of pNML devices [16]. The propagation is supported by applying an external clock field called H_{clock}. The nucleation and the propagation of the new domain define the basis for the signal transmission in this technology. The propagation can be planar, so through neighboring magnets in

the same plane, or perpendicular, so through overlapping magnets belonging to different layers interconnected by magnetic vias [12]. Hence, signal transmission can take place among different layers making it possible to realize 3D structures. In order to guarantee a correct propagation, the switching process should be completed during the clock field pulse time t_{clock}. As a consequence, all the operations required to switch the magnet, like the nucleation of the domain wall and the propagation of the new magnetization, must be completed before the end of the clock period [16]. This defines a constraint on the pulse time t_{clock}:

$$t_{clock} > t_{nuc} + t_{prop}. \tag{1}$$

Here, t_{nuc} represents the time required to nucleate the structure, while t_{prop} is the time required to propagate the magnetization through the entire structure.

To nucleate a nanomagnetic structure means to reverse the current state of magnetization in the ANC. The field required to do this can be extracted considering the anisotropy field, modelled by the Stoner-Wohlfarth model [16] [15]:

$$H_{ani} = \frac{2K_{eff,ANC}}{\mu_0 M_S}, \tag{2}$$

where, M_S is the saturation magnetization of the magnet and $K_{eff,ANC}$ is the effective anisotropy in the ANC. In fact, each nanomagnet is characterized by a unique anisotropy term (called effective anisotropy K_{eff}) which depends on the crystal structure, the geometry and the material. H_{nuc}, the nucleation field required to switch the DW, is equal to the H_{ani} (eq. 2). The main role of the nucleation field is to reduce the energy barrier $E_{barrier}$ of the structure.

The nucleation field required to nucleate a device is influenced by the superposition the coupling fields of the neighboring cells.

$$H_{eff} = H_{clock} - C_{eff}. \tag{3}$$

Where C_{eff} is:

$$C_{eff} = \sum_{i=1}^{N} C_i M_i. \tag{4}$$

Here, C_i represents the coupling fields from the inputs with magnetization $M_i \in \{-1; 1\}$ [16]. M_i influences the energy barrier which increases or decreases according to the parallel or antiparallel state of input magnetization with respect to the current state. Whether nucleation occurs or not can be estimated by exploiting the probability of nucleation P_{nuc}, expressed in terms of applied field H_z and of the duration time of the field t by using the Arrhenius model [16]. To nucleate the ANC of the nanomagnet, the clock field pulse of amplitude H_{pulse} and its effective pulse time t_{eff} are considered:

$$P_{nuc}(t_{eff}, H_{pulse}) = 1 - \exp\left(-\frac{t_{eff}}{\tau(H_{pulse})}\right) \tag{5}$$

$$\tau(H_{pulse}) = f_0^{-1} \cdot \exp\left(\frac{E_0\left(1 - \frac{H_{pulse}}{H_0}\right)^2}{K_B T}\right) \tag{6}$$

Two constraints on the nucleation probability can be expressed:

$$P_{nuc,support} = P_{nuc}(t_{nuc}, H_{clock} + C) \to 1, \tag{7}$$

$$P_{nuc,prevent} = P_{nuc}(t_{clock}, H_{clock} - C) \to 0. \tag{8}$$

Eq. (7) supports the nucleation, while eq. (8) prevents it. The error rate of a device during one clock cycle is given by:

$$E_{device} = 1 - P_{nuc,support} \cdot [1 - P_{nuc,prevent}] \tag{9}$$

The nucleation probability, and therefore the reliability of the whole pNML circuit, strongly depends on the nucleation time t_{nuc}, the clocking pulse time t_{clock} , the field amplitude H_{clock} and the coupling fields C [16]. The time required to nucleate a DW can be expressed in terms of the desired probability of nucleating it:

$$t_{nuc} = -\tau(H_{eff}) \cdot \ln(1 - P_{nuc}). \tag{10}$$

B. Domain Wall

Once the nanowire is nucleated, the magnetic charge is propagated through the entire structure. The propagation is characterized by a speed of motion, the DW velocity v_{DW}, which depends on the applied field [16]. Three main regimes can be identified in the propagation of the new state, in thin multilayer structures. These regimes are modelled according to the external field H_z applied to the magnetic structure [16]. In the first two regimes, where the H_z less or comparable to the intrinsic pinning field, v_{DW} strictly depends on the temperature with an exponential relation. In the flow regime ($H_z \gg H_{int}$) instead, the velocity depends linearly on the applied field and can be modelled according to the following equation:

$$v_{DW}(H_z \gg H_{int}) = v_0 + \mu_w(H_z - H_{int}) \tag{11}$$

where v_0 is a numerical prefactor and μ_w is the domain wall mobility. From a theoretical point of view, the velocity has a linear dependency on the applied field and consequently the adopted working regime is the flow regime. The propagation time t_{prop} can be defined as follows:

$$t_{prop} = \frac{l_{mag}}{v_{DW}(H_{clock})} \tag{12}$$

where l_{mag} is the length of the magnet.

C. Notch

The propagation of DWs can be controlled by a geometric modification [14]. With notches it is possible to pin the magnetization propagation. Here, the pinning and the depinning operations play a fundamental role. In other words, a notch defines an energy barrier able to block a magnetic transmission. The depinning field H_{dep}, which is required to depin a DW, is [14]:

$$H_{dep} = H_{int} + \frac{\sigma_w sin\alpha}{2M_s(h + \frac{1}{2}\delta_w sin\alpha)}, \tag{13}$$

where α is the notch apex angle and h the notch width.

The depinning time (t_{dep}) is the time required to depin a DW from and it is described by the following equation:

$$t_{dep} = \tau_0 \cdot e^{\frac{M_s V_a (H_{dep} - H)}{K_B T}}. \quad (14)$$

Here, V_a is the activation volume and τ_0 is the inverse of the attempted frequency f_0.

In order to depin the magnetic domain from the notch, an external in-plane field is applied. In fact, the out of plane clock field applied externally, which is required to switch correctly the domain wall and propagate the new domain, has an amplitude which is not high enough to depin the notch. For this reason, an additional in-plane field is used to depin it since this reduces the required depinning field. Since temperature plays an important role, and can help to overcome the energy barrier of the notch, it is important to define the probability of depinning [14]:

$$P_{dep} = 1 - e^{\frac{t}{\tau(H_{eff})}}, \quad (15)$$

where H_{eff} represents the applied effective magnetic field, which is a combination of the in-plane and out-of-plane fields. t instead, represents its duration, while $\tau(H_{eff})$ is the time constant which describes the switching of the magnetization [14].

D. Vias

Vertical interconnections (vias) represent the key element for the realization of signal crossings. This element enables the design of 3D architectures with pNML. In these novel structures, information is carried among different layers by using such magnetic vias [12]. It acts as an ANC, but since the nucleation occurs within vertically aligned magnets the coupling is ferromagnetic. This defines a new constraint in the clock pulse duration. Indeed, t_{clock} should be long enough to guarantee both the nucleation of all vias and the propagation of the domain walls, in all layers.

E. VHDL Implementation Hints

All the equations here reported are implemented in VHDL by using the *math* and *numeric* libraries. The idea behind this compact model is to have a single entity for each basic component. For example, the interconnection of a *Nucleation Center* and a *Domain Wall* entities defines the structure of the device represented in Fig. 1.D. Hence, similar devices can be arranged and connected together composing logic and finally circuits. The model is structured in two parts: I) a library containing the implementation of physical equations and all parameters (like constants, geometrical information etc) and II) the entity declaration of each component with the implementation of its physical behavior. An example of the parameter contained in the library file is given in the following paragraph in table I and II. Here, all the geometrical and fields parameters are listed and together with the corresponding value. Designers are free to modify all these quantities according to their specific needs, in this way it is possibly to verify of the performance of pNML devices vary in order to refine the peculiarity of this technology. Equations are implemented through several procedures. The main implemented functions are:

- Evaluation of the propagation time t_{prop}
- Evaluation of the nucleation time t_{nuc}
- Evaluation of the DW velocity
- Computation of the nucleation probability
- Extraction of the critical path
- Evaluation of the minimum nucleation time

All the procedures are invoked by the components' entities. For example, the implementation of the Nucleation Center sees a list of several calls to the needed procedures. In this case, the first function invoked is *Computation of the nucleation probability*. Here the effective field H_{eff}, the switching time τ_{eff} etc... are evaluated by the use of the equation reported in the previous paragraphs. At last, the nucleation probability is returned and then the magnetization status can be evaluated according to the clock signals and the status of the neighboring magnets.

III. Circuit Analysis

The compact model presented here makes it possible to simulate logic architectures while preserving technological information needed to study the behavior of pNML circuits. Different experiments have been conducted on a Full Adder (FA) [10] circuit in order to extract the physical quantities and fit the equations which must be inserted within the implemented libraries. The following circuits have been tested by using the technological parameters listed in Tab. I and II.

Table I
Geometrical parameters set according to [16], [10].

Geometrical parameter	Value
Length of the basic block DW	$3.5 \cdot 10^{-7}$ m
Width of the domain wall	$2.0 \cdot 10^{-7}$ m
Thickness of the Co	$3.2 \cdot 10^{-9}$ m
Thickness of the stack	$6.2 \cdot 10^{-9}$ m
ANC volume	$1.68 \cdot 10^{-23}$ m^3
Apex angle	51.5°
Notch height	$54.0 \cdot 10^{-9}$ m
Activation volume	$1.26 \cdot 10^{-23}$ m^3

Table II
Field parameters set for the simulation, according to [10], [16].

Field parameter	Value
Clock field amplitude	560 Oe
Intrinsic pinning field	190 Oe
Coupling field strength for the inverter	153 Oe
Coupling field strength for the majority voter	48 Oe
Coupling field strength for the magnetic via	75 Oe
Effective anisotropy	$2.0 \cdot 10^5$ J/m^3
Saturation magnetization of Co	$1.4 \cdot 10^6$ A/m
Depinning field	736.6 Oe

In this paper we present how the behavior of a multiplexer (MUX) realized experimentally has been mirrored by using our model. This circuit has then been adopted in order to

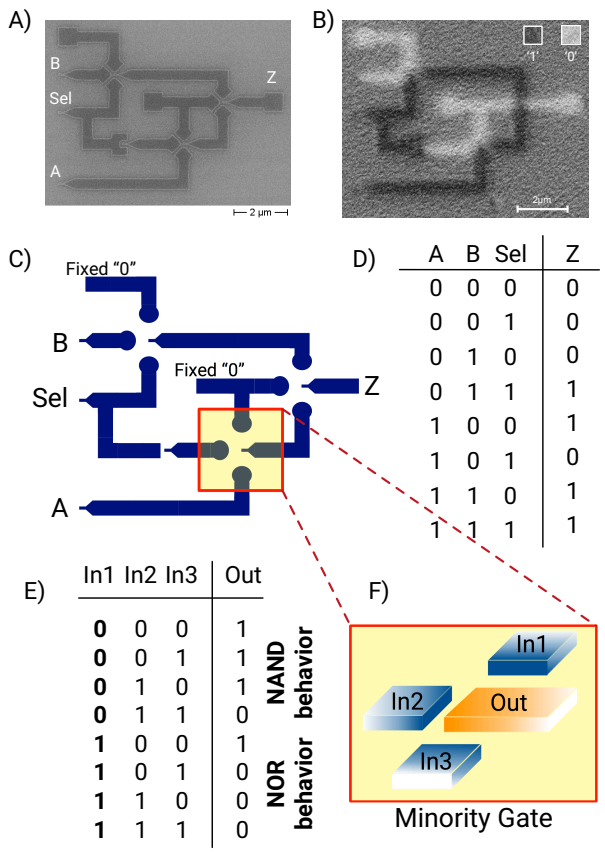

Figure 3. A) SEM image of the fabricated 2-to-1 1-bit multiplexer; B) Wide-field-MOKE image of the fabricated multiplexer when the input signals are equal to A=1, B=0 and Sel=1. C) Implemented 2-to-1 MUX with D) truth table. E) NAND and NOR behaviors can be programmed according to the input pattern of the F) Minority Gate.

realize an accumulator. Performance studies are here proposed, also considering a generic implementation which allows the investigation of the n-bit accumulator. Hence, this architecture combines the use of both the MUX and the FA, also exploiting the novel 3D topology.

A. Multiplexer

In general, the functionality of the considered 2-to-1 MUX can be described as:

$$Z = (A \cdot \overline{S}) + (B \cdot S) : \tag{16}$$

Eq. (16) is then modified as follows in order to be synthesized by using only NAND gates:

$$\begin{aligned} Z &= \overline{\overline{(A \cdot \overline{S}) + (B \cdot S)}} \\ Z &= \overline{\overline{(A \cdot \overline{S})} \cdot \overline{(B \cdot S)}} \end{aligned} \tag{17}$$

The NAND operation in realized by using the majority voter gate, with one input fixed to 0. The multiplexer needs three majority voter gates and one inverter. The realized structure is depicted in Fig. 3.E and F.

The fabrication process started from a cleaned silicon wafer. The multilayer stack, which enables the perpendicular magnetic anisotropy, has been obtained by RF magnetron sputtering. An ultra-thin film of $Ta_{1.7nm}Pt_{4nm}[Co_{0.75nm}Pt_{1.4nm}]_{x4}Pt_{2.75nm}$ has been deposited. The adhesion layer (Ta) and Pt have been sputtered at 2μbar, whereas Co was sputtered at 4μbar. After spin coating a thin layer of PMMA resist, the magnetic stack has been patterned by using Focus-Ion-Beam (FIB) lithography with a dose of $5 \cdot 10^{12}$ ions/cm^2. A computer-defined mask of the multiplexer has been used to pattern the multilayer stack. During the lithography, the ANCs are defined by increasing the Ga^+ dose to $5 \cdot 10^{13}$ ions/cm^2 over a specific spot of 30x30 nm^2. Afterwards, the exposed resist is developed for 15s. By electron beam physical vapor deposition, a thin layer of Ti is deposited on top to protect the magnetic stack. Then, the remaining resist is lifted off and the magnetic devices are structured by Ion Beam Etching.

Fig. 3.A shows the SEM image of the fabricated device. Here, magnetic nanowires are in the range of 400nm. Wide nanomagnets have been fabricated to get sharper images during the measurement phase at the Wide-field-MOKE. We have verified the logic behavior of the 2-to-1 multiplexer by using a Wide-field-MOKE microscope. The out-of-plane field was generated by an external electro-magnet placed just below the circuit. In Fig. 3.B we report the correct ordering of the magnetic circuit for the input combination: A=1, B=0 and Sel=1. The Wide-field-MOKE image shows that the proper input B is selected and transferred to the output (Z). The measured coupling field of the inverter gate is 10mT.

The functionality of the circuit depicted in Fig. 3.C and D is analyzed by using the VHDL model both in terms of switching behavior and of timing performance.

In the first instance, the simulation extracts the maximum clock frequency that can be achieved for the considered circuit. This value is strictly related to the critical propagation time, so the propagation delay introduced by the longest domain wall, and the minimum nucleation time required to nucleate the ANC. The extracted minimum nucleation time is 558 ns, while the longest propagation time is 73.7 ns. According to these values, the clock period is evaluated by setting in the VHDL package the values of $t_{nuc} = 600$ ns and $t_{prop} = 80$ ns. The resulting t_{clock} is 850 ns considering value rounding and the non-idealities introduced by H_{clock}; indeed, the rise time must be taken into account, and it is calculated as 20% of the pulse duration in the worst possible case. This timing analysis is related to the geometric characteristic of the examined sample. Indeed, in this example larger device sizes have been adopted in order to improve the testability during measurements. Nevertheless, smaller dimensions can lead to significantly higher performance.

Considering these parameters, the circuit latency can be extracted considering an exhaustive analysis of the input patterns. Results are reported in Tab. III. Generally, the output is valid during the second clock cycle. Only the input combination 1–0–0 has the longest delay, since it passes through all the chains (due to the fact that the majority voter that computes $A \cdot \overline{S}$) needs the reverse of the selector to discriminate the output. Moreover, this value is also needed by the last majority voter to compute the final result.

Table III
LATENCY FOR THE OUTPUT OF THE 2 TO 1 MULTIPLEXER.

A	B	Selector	Z	Z latency
0	0	0	0	3.172 μs
0	0	1	0	3.172 μs
0	1	0	0	3.172 μs
0	1	1	1	2.322 μs
1	0	0	1	4.022 μs
1	0	1	0	3.172 μs
1	1	0	1	2.322 μs
1	1	1	1	2.322 μs

B. 2-bit accumulator

The accumulator architecture considered here is depicted in Fig. 4. The arithmetic unit is an adder realized by using the FA presented in [10]. The MUX is used to select one of the inputs of the adder unit. The choice is made between the previous computed sum, and the current applied input. The storing of the information is accomplished by using the notch structures.

The structure is organized in a 3D topology. It is divided in three planes, exploiting the LIM (Logic In Memory) approach [17]: the memory plane, the logic plane and the routing plane. The pNML technology offers the possibility to be easily adopted in 3D organizations. since the different layers can communicate by ferromagnetic coupling. In this way no complex interconnections are needed, and moreover, area can be saved by overlapping different layers.

The logic plane contains the computational units: the 2-to1 MUX and the FA. FAs can be arranged in order to compose a Ripple Carry Adder (RCA). In this organization, each carry is passed to the next FA and only when the last terminates its computation the final result is valid.

The routing plane connects inputs with the logical plane. It is used also to connect the MUX with the FA and the carries. While designing the accumulator, paths must be balanced in order to guarantee a correct signal synchronization. Hence, two inverters in cascade must be added in order compensate the delay introduced by the MUX. This guarantees inputs to reach the full adder in the same clock cycle. Moreover, each FA belonging to the RCA introduces a delay. For this reason, more significant bits must be properly delayed.

Within the memory plane, notches have a twofold functionality: they can be used as memory element able to store the current state of magnetization, and they can be used as programmable inputs for majority/minority gates, in order to realize logic programmable architectures.

The logic plane communicates both with the routing plane and the memory plane. In this topology, external inputs are connected to logic through the routing plane. Indeed, partial results of the accumulator are stored thanks to the notches belonging to the memory plane.

Similarly to what is presented for the MUX, the accumulator has also been tested with our physical-compact model. Here t, $t_{nuc,min}$ is equal to 558 ns and the longest propagation time (t_{prop}) is 622 ns. This critical value comes from the feedback route. By adding the rise time, which is equal to the 20% of the t_{clock}, the final duration of the applied H_{clock} is 1.625 μs.

Table IV
RESULTS OF THE N-BIT ACCUMULATOR: $t_{nuc,min}$, t_{prop}, CRITICAL PATH (C.P.), t_{clk} AND LATENCY (IN TERMS OF CLOCK CYCLES).

	$t_{nuc,min}[ns]$	$t_{prop}[ns]$	C.P.[μs]	$t_{clk}[\mu s]$	Lat. [cc]
2 bit	558	622	1.22	1.625	6
4 bit	558	622	1.22	1.625	8
8 bit	558	622	1.22	1.625	12
16 bit	558	842	1.442	1.875	16
32 bit	558	1.314	1.914	2.5	32

For the 2-bit accumulator, the extracted critical path is: $t_{critical} = 1.22$ μs.

The various input combinations are tested. After the sixth clock cycle for any combination the outputs are ordered correctly. The critical output bit is the one that comes from the sum of the last full adder, so the second bit of the final result.

The selector is enabled at 26.0 us in order to guarantee that the first result is valid for any combination.

The in plane field that depin the notch structure in the memory layer is activated with two pulses of a duration of 50 ns. The first one is activated during the positive phase of the clock field, while the other in the negative phase. The couple of pulses is activated every 21.0 us. After six clock cycles the new computed result is valid.

C. Generic Accumulator

The design of the 2-bit accumulator wa intended to be flexible from the first steps of development. As a consequence, the layout has been developed considering the repeatability of the structure. The generic VHDL implementation of the architecture makes it possible to automatically scale the input parallelism. For each configuration, values of $t_{nuc,min}$, t_{prop} and t_{clock} are evaluated (Tab. IV).

It can be noticed that, for the 4-bit and 8-bit structures, the critical path is the same as for the 2-bit accumulator. For the other structures, the critical path is related to the routing of the inputs to the FA, which increases with the number of bits.

A summary of how the latency varies depending on number of bits, is reported in Tab. IV. The selector and the pulses of the in-plane field are enabled according to the number of bits of the tested architecture. As for the 2-bit case, the selector is set to one after the first activation of the two pulses of in-plane field.

IV. FUTURE DEVELOPMENTS AND CONCLUSIONS

The results reported have been obtained according to the physical quantities reported in in Tab. I and II. However, further technological improvement are currently under investigation [18].

As already discussed, dataflow directionality depends on FIB irradiation, which creates the artificial nucleation center. The size of the ANC would limit the scaling of pNML technology. However, we are trying to solve this limitation by tuning the tip geometry and simplifying the fabrication process. The idea is to remove the FIB irradiation within the fabrication process and avoid the ANC scaling limitation.

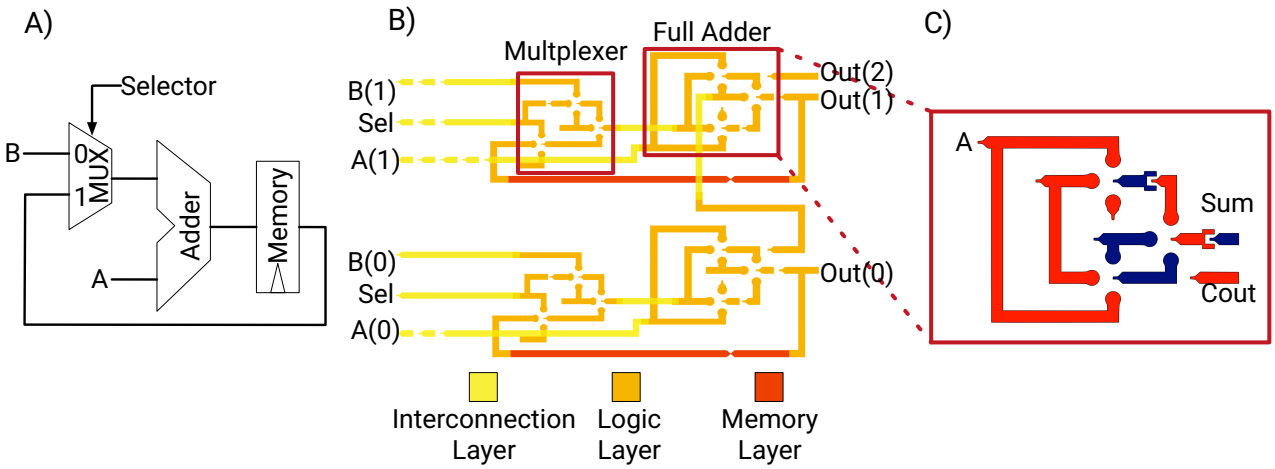

Figure 4. A) The Accumulator architecture is composed an adder and a multiplexer. The former is implemented as a chain of FAs. B) Accumulator layout C) FA layout already verified [10]

Usually our process starts from a cleaned and oxidized silicon wafer. On top of that, we sputter the multilayer of Co/Pt and we spin coat a thin layer of PMMA resist. During the lithography we pattern the magnet geometry and we define the ANC by FIB irradiation. Then, the exposed resist is developed and the thin layer of Ti is evaporated to protect the magnetic layer during the lift-off process. Finally, the magnets are structured by Ion Beam Etching.

As reported by Kimling in [19], modifying the process in the following way could lead to a 60% reduction of the nucleation field. In this process, on top of the cleaned silicon wafer a thin layer of PMMA is spin coated before doing the lithography. Afterwards, the irradiated resist is developed and the multilayer stack (Co/Pt) is sputtered. As a final step, the non-irradiated resist is lifted-off concluding the fabrication process.

This process exploits the undercut profile obtained after the development to have a non-homogenous thickness of the Co/Pt stack. In particular, the magnetic stack will be thinner on the side of the magnet and on the tip. When the multilayer stack is thinner, the magnetic anisotropy is locally reduced. Therefore, by shaping the tip (input) of the nanowire it is possible to define the ANC without the need of the FIB irradiation and the Ion Beam Etching steps.

With this paper, we have presented a physical compact model enabling fast simulations of complex logic architectures. The model has been proved through experiments; performance of a Multiplexer and a generic n-bit Accumulator are analyzed in order to be an example of how our model can be used for further investigations. Its flexibility offers the possibility to be easily adapted by simply modifying the technological parameters. As an example, to scaling the size of DomainWalls results in an improvement of timing performance. Moreover, it is possible to study how different fabrication processes might lead to more reliable circuits. In other words, with the presented compact-model it is possible to verify how physical can influence performance.

As a future step, we are now integrating the model presented here into our ToPoliNano suite. This will enable the automatic generation of the VHDL code making it possible to simply describe circuits through a graphical representation of a set of basic elements.

Investigation on logic architectures can be carried on also exploiting the novel concept of Logic In Memory which sees the integration of memory elements (notches) and logic onto the same device. Indeed, the introduction of notches and vias enables the design of 3D circuits.

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