A Physical-Aware Abstraction Flow for Efficient Design-Space Exploration of a Wireless Body Area Network Application

M. Crepaldi, P. Motto Ros, D. Demarchi
IIT@PoliTo/Politecnico di Torino (DET)
Corso Trento, Torino
Email: marco.crepaldi@iit.it

J. Buckley, B. O'Flynn
Tyndall National Institute
Lee Maltings, Dyke Parade, Cork
Email: john.buckley@tyndall.ie

D. Quaglia
EDALab s.r.l.
Cá Vignal 2, Strada Le Grazie, Verona
Email: davide.quaglia@edalab.it

***Abstract*—This paper presents abstraction techniques and modeling approaches to include physical-level antenna and receiver performance effects in a system-level network simulation for Wireless Body Area Networks (WBAN). The simulation platform is based on SystemC which can be used to model digital HW and SW aspects of an embedded application. By using the SystemC Network Simulation Library also a distributed network scenario can be simulated. Here, this platform has been extended to take into account the bit error rate and the path loss associated with antenna positioning in close proximity to the human body and with the design parameters of the wireless receiver. Antenna effects are modeled through a database of performance values based on physical measurements on a human phantom. Path loss information is fed in the SystemC simulator to model the received signal strength as a function of the position of nodes. The same information is used in the physical-level simulation of the receiver to extract bit error rate curves to be used by the SystemC simulator to build a statistical model of packet corruption. Instead of physical-level details, their effects are modeled in a parametric way into the system-level simulation thus combining speed and fidelity and allowing cross-domain design space exploration.**

***Keywords*-Network-level simulation, Abstraction, WBAN, Antenna modeling, Digital radio receiver, cross-domain design, joint design.**

I. Introduction

The design of a smart system is becoming increasingly complex in distributed applications where several embedded systems nodes with various hardware (HW) and software (SW) components wirelessly transmit over a network. A realistic example of this kind of application is the healthcare wireless body area network presented in Fig. 1. Each monitored person wears a number of wireless nodes that capture and process different kinds of body-related information; they exchange data and commands with a base station over a radio channel which is shared among different unrelated data flows.

To design such kind of application, several aspects belonging to *different domains* should be modeled: 1) **SW components:** they range from the application down to the operating system and drivers; 2) **HW components:** CPU which executes SW, memory, communication bus and transceiver; 3) **Antennas:** propagation and the reception of radio signals with performance depending on the positioning on the human body; 4) **Communication channel and non-ideality:** radio signal propagation between transmitter and receiver affected by signal path loss as a function of devices separation and interference with other radio devices.

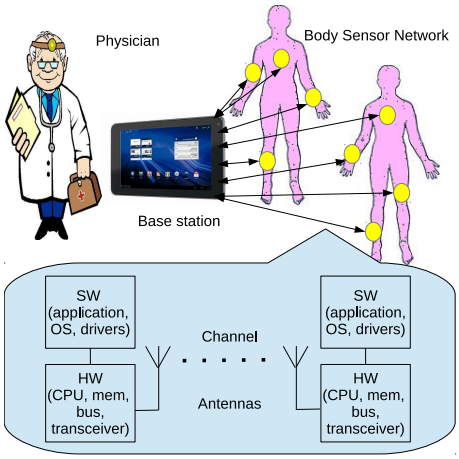

Figure 1. Wireless Body Area Network Scenario.

These different domains (SW, HW, radio frequency transmission) impact on the design especially when very efficient solutions are needed (i.e. cross-layer design [1] and joint design [2]). A *cross-domain design framework* should model and simulate all these aspects to allow the exploration of the corresponding design space dimensions and the verification that requirements are met.

Unfortunately, such aspects are modeled by very different tools with very different approaches. A comprehensive framework can be obtained through co-simulation, i.e., synchronized execution of different simulators exchanging information through open interfaces [3], [4]. The speed of co-simulation is limited by synchronization overhead and by the slowest tool in the chain (e.g., electromagnetic simulation and post-layout simulator). Moreover, it is hard to be implemented with proprietary tools.

Traditionally, the system-level [5], [6] or network-

level [7], [8] simulation of a complex distributed embedded application uses the full computational power of the host to reproduce data processing inside each node and protocols above physical layer for inter-node interaction. Therefore, such simulation lacks of low-level physical details. Design decisions are normally made based only on high-level functionality, but more interesting optimizations could be possible if low-level non-ideality are considered especially for applications requiring strict reliability, energy or resource constraints. However, increasing the complexity of a system-level model implies loosing the advantages of fast high-level simulation.

Therefore, the requirements of an efficient cross-domain simulation approach are: 1) Simulation speed close to system-level simulation for fast design-space exploration; 2) Modeling of as many design parameters as possible belonging to different domains to enrich design space; 3) Generation of executable models to be called by well-known tools for automatic design-space exploration [9].

This work aims at filling these gaps by *replacing co-simulation with abstraction*; system-level simulation is enriched with the high-level effect of physical-level details without simulating them in the same runtime session. The behavior of antennas is described in terms of a library of simulated and measured 1-Port Scattering (*S*) Parameters as a function of antenna positioning on the human body. The performance of the receiver are efficiently evaluated because its model is all-digital and, by-design, enables fast statistical measurement and characterization; the performance of the receiver is modeled as a look-up table which returns the bit error rate as a function of design parameters. Finally, the application-level simulator contains an abstract model of the transmission channel which takes into account path loss and bit error rate in the simulation of message exchanges with higher speed compared to standard co-simulation paradigms.

The paper is organized as follows. Sec. II details the adopted abstraction and modeling approach. Sec. III details the antenna modeling approach. Sec. IV describes the digital receiver and its modeling advantages. Sec. V details the path loss abstract modeling. Sec. VI presents the high-level network simulation library in which the abstract models are implemented. Sec. VII evaluates the effectiveness of our approach in terms of simulation time. Sec. VIII concludes the paper.

II. Abstraction and modeling approach

A recent trend in embedded system design consists uses *abstraction* to reduce simulation time by removing details (e.g., clock events) but not their effect (e.g., the timing properties) [10]. Our target is a methodology to abstract physical communications inside a wireless body area network to remove simulation details about physical models but not their effects on system performance.

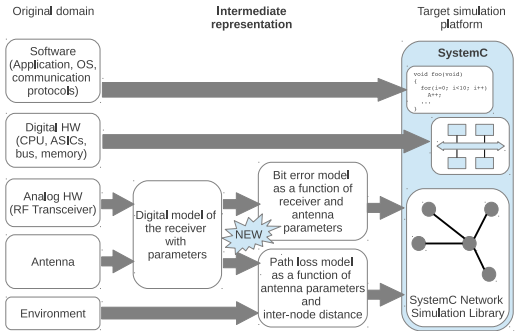

Figure 2. Summary of the overall approach for the abstraction of a WBAN system.

Fig. 2 summarizes the abstraction approach followed in this work. The left side of the figure shows the different components of the system belonging to different domains, i.e., SW, digital and analog HW, antenna and environment which propagates radio signal. SW part consists of the application, the operating system and all the communication protocols above the physical layer. Digital HW is represented by the platform which executes SW. Both SW and digital HW components can be described by discrete-time models focusing of data to elaborated. In other words their models can be functions taking input data and the discrete time (i.e., clock signal). Vice versa analog HW, antenna and environment are described by continuous-time models and usually frequency-domain functions are used. Therefore, this heterogeneous mix can be considered as a Cyber-Physical system.

While abstracting digital HW aspects mainly consists in merging low-level simulation events into coarse-grain events [11], issues arise for other domains. For example, let us consider the antenna sub-system. An antenna in an electrical transducer that converts a guided electromagnetic wave to a free-space wave (and vice versa), enabling wireless communication. As such, an antenna cannot be strictly identified with a discrete-time-domain function. In other words, the antenna gain, the antenna *S*-Parameters, the electrical matching, the resonance frequency and even the orientation are not directly usable at system-level because not straightforwardly linked to the information which is processed at high-level. Therefore, the only way to enable a high-level simulation to account for low-level antenna details is *making a data bit account for antenna effects*. In general, from a system-level perspective, the physical-level implementation details need to be included as far as they impact on a high-level figure of merit. The main keypoint of this cross-domain work is the possibility of grouping together a certain number of details and condense them in the form of a function f which maps design parameters onto performance values.

In this work, the block which bridges the frequency-

domain and the discrete-time-domain is the *digital model of the receiver*. To obtain an effective bridging the receiver shall be capable of parametric modeling to enable a design space exploration based on a variation of parameters directly related to its physical implementation. Moreover, the receiver shall be capable of parameterization and measurements covering the frequency domain specifications of the antenna. The most important parameter which is directly related to data link performance is bit error rate. The main activity to bridge the RF domain with the application domain is then addressing path loss and bit error rate performance figures of the receiver by using cumulative frequency parameters that can be extracted from antenna measurements.

The right side of Fig. 2 shows the simulation platform we adopted for the simulation of this system. SystemC [5] has been chosen for its modeling flexibility. SW and digital HW can be easily modeled in SystemC being its main target. In the last years an extension of SystemC has been created to model packet-based networks; the SystemC Network Simulation Library (SCNSL) [12] allows modeling network nodes exchanging packets over point-to-point and shared links. The contribution of this work is shown in the middle of the figure which represents the generation of components for SCNSL to model bit errors and path loss starting from parametric physical-level models of the receiver and the antenna as well as from the inter-node distance.

III. Antenna Interaction with the Human Body

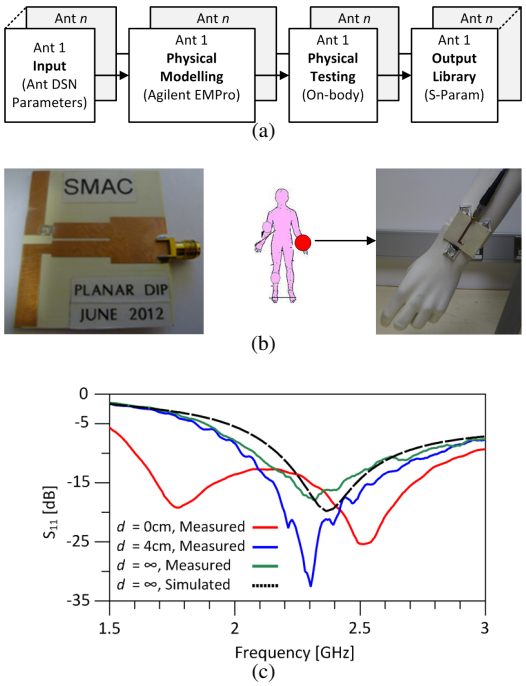

Figure 3. **(a)** Antenna modeling, measurement and library development methodology, **(b)** Prototype antenna and antenna testing on phantom arm, **(c)** Measured antenna return loss as a function of antenna-wrist distance d.

A. Antenna Detuning

Antenna radiation and propagation characteristics for WBAN applications can be significantly affected by human body effects [13]. One effect is antenna detuning where the resonant frequency of the antenna is detuned from its nominal value. This effect leads to a change in antenna impedance due to signal reflections from the antenna and leads to a waste in power delivery to the antenna. The human body can also introduce a $10-15$dB reduction in received WBAN signal strength at 2.45 GHz, due to absorptive effects [14]. This in turn has important implications for WBAN performance in terms of bit-error-rate and link quality as well as power consumption. WBAN applications in particular demand antenna structures of small physical size. This size limitation leads to inherently narrowband structures that are easily detuned by nearby objects. Because of the above effects, modeling of antenna behavior in proximity with the human body is challenging due to the changing environment in the vicinity of the antenna. In addition, it is difficult to predict (during early system-level modeling) what antenna topology works best with a particular radio transceiver and what other circuitry (e.g. matching network) may be required. It is also difficult to predict the potential bit-error-rate of a WBAN system when interfaced with a particular radio transceiver device and placed on the body.

B. Physical-Level Antenna Modeling

To accurately predict antenna behavior at a physical level (low-level), Electromagnetic (EM) modeling is required to analyze and optimize the impedance and radiation characteristics of antennas for a particular application. The Finite Element Method (FEM), Method of Moments (MoM) and Finite Difference Time Domain (FDTD) techniques are the most popular approaches used in antenna design. Once the main antenna specifications (such as center frequency f_c, Gain, Impedance, Bandwidth) are specified based on the application, choosing the most appropriate antenna topology is the next step. Antenna comparison and selection is an activity that requires a significant amount of time in terms of both model development and computation. It is difficult, therefore, at an early stage of the design cycle, to quickly evaluate and compare potential antenna performance without first having to complete lengthy modelling activities.

C. High-Level Antenna Modeling Approach

This section details the approach used to allow physical-level details of the antenna to be included in an application-level network simulation for WBAN. The methodology is illustrated in Fig. 3(a) with specified performance parameters such as resonant frequency f_0, bandwidth B, Return Loss RL and Gain G used as design constraints during modeling. The selected antenna types $(Ant1-n)$ are the most commonly used antennas used in WBAN including the Dipole, Monopole, Loop, Inverted-F antenna (IFA) etc.

In terms of analyzing the antenna model, a planar free-space model is first analyzed using Agilent's 2D and 3D EM simulation software (Agilent Momentum and EMPro [15]). Having optimized the design to meet the target specification, a hardware prototype is then fabricated. Fig. 3(b) shows an example of a planar dipole antenna with integrated Balanced-To-Unbalanced-Converter (BALUN) which is designed for 2.45 GHz ISM-band operation. All antennas are fabricated on a RO4350B low-loss substrate [16]. Model validation is then performed using physical measurements (for the free-space case) for each antenna type to verify model accuracy and robustness when compared to actual measured performance. In the case shown, the impedance characteristics of the planar dipole antenna are measured in the frequency domain using a Vector Network Analyzer (VNA) instrument with the antenna placed on a phantom human arm during testing.

Fig. 3(c) plots the measured antenna return loss as a function of the antenna-wrist distance (d). Some of the effects of the human body are observed in this case with antenna detuning effects leading to a decrease in f_c, a change in bandwidth as well as a reduction in power delivered to the antenna. It can also be seen that simulation and measured results are in good agreement for the free-space case ($d = \infty$). Once the wrist measurement is complete, the measured edited 1-port S-Parameters are saved to a library. The advantage of this method is that antenna simulation time can be greatly reduced. For example, a full-FEM simulation for the planar dipole antenna is very time consuming and requires approximately 10 minutes to compute whereas running a simulation directly from the library takes only seconds. The same procedure is carried out with the antenna placed on several areas of the body including wrist, forearm, upper arm, chest, thigh etc with all results added to the library. Low-level, measured antenna performance parameters can then be extracted from the above library and can be used as input for a radio receiver model as next described in Sec. IV. The path loss degradation due to the positioning of the human body is also used as input for the application-domain SystemC simulator presented in Sec. VI.

IV. Digital Receiver

Fig. 4 shows the generic architecture of the logic receiver. The receiver is based on the hypothesis that only logic gates are used for the design of the receiver to enable heavy digitizing [17]. The receiver is truly all-digital hence without requiring ad-hoc ADC and DAC for digitizing as normally required in digital radio solutions [18]–[20].

After antenna or matching filtering, in the block scheme H, $\mathrm{RF_{IN}}$ is processed by the front-end. It is a non-linear unit, based on CMOS inverters at the middle of the supply voltage V_{dd}, that amplifies the incoming pulses to saturation level and transforms $V_{dd}/2$ crossings $\mathrm{RF_{IN}}$ variations into high d/dt digital edges. Compared to standard receivers which require a signal level below a limit to ensure a sufficient linearity, here the output of the front-end needs to be saturated for a correct operation. Its operation is similar to a limiter in Frequency Modulation (FM) receivers, but without maintaining a sinusoidal nature, i.e. the wave phases of $\mathrm{RF_{IN}}$ saturate to rail-to-rail limits and edges become digital, maintaining a correct phase rotation compared to the small signal input. $\mathrm{D_{OUT}}$ feeds the baseband unit which comprises a delay line of duration ΔT. The receiver does not require an analog delay line as in Transmitted Reference receivers (TR) or pulsed Frequency Shift Keying (FSK) demodulators. The obtained delayed signal $\mathrm{D'_{OUT}}(t-\Delta T)$ with $\mathrm{D'_{OUT}}$ is processed by two logic `Edge/level combiners`, i.e. Serial-In-Parallel-Output (SIPO) asynchronous circuits. The `Edge/Level Combiners` compute the temporal event (hit) of receiving a pulse, implementing a specific temporal logic function based on signal edges and levels both for positive and negative edge transitions using flip-flops memory elements and combination logic. The correlators have a memory size of N, corresponding to the number of consecutive edge/levels transitions processed, and can have N different parallel outputs. Parallel outputs are '1' only when the edge/level functional output is true and *maintained* in time, zero otherwise. When both a negative and a positive edge correlator outputs are valid, a new pulse C_i is issued, for $i \in [0, N-1]$. The generated digital event P, self-synchronized at carrier level to the incoming RF signal oscillations, is processed by an additional `Edge/Level Combiner` with memory size K. This re-clocker block operates as a filter and removes glitches that may result from the asynchronous sequential combination of the preceding bi-phase `Edge/Level Combiners`. Signals S_C and S_F control the multiplexers that select the parallel output confidence level.

The pulse events E feed an asynchronous Synchronized-On/Off Keying (S-OOK) demodulator [21]. Besides the standard `DATA` and `CLK` nominal outputs, the demodulator provides two corresponding signals carrying the trigger events of the processed synch and data pulses (d and s) which feed a multiplexer controlled by a Duty-Cycling Controller (DCC), signal S_E. The DCC locks the incoming `DATA` and `CLK` events to generate a duty-cycling activation signal which precedes each transmitted symbol. During preamble search phase, the DCC periodically activates the receiver for T_{ON} and deactivates it for T_{OFF} with uncorrelated period compared to symbol period T_s (duty cycle $\frac{T_{ON}}{T_{ON}+T_{OFF}}$). When a pulse is received, the logic shuts down the front-end for T_{OFF} and reactivates it before a new symbol is received based on the last Fast-MPE event (preamble sequence), or the Last Slow-MPE event (locked condition, payload). S_E selects `Data` or `Synch` valid transitions, during preamble search and payload demodulation, respectively. With duty-cycling the receiver can decrease the energy consumption and gate other concurrent pulse transmissions for medium access control

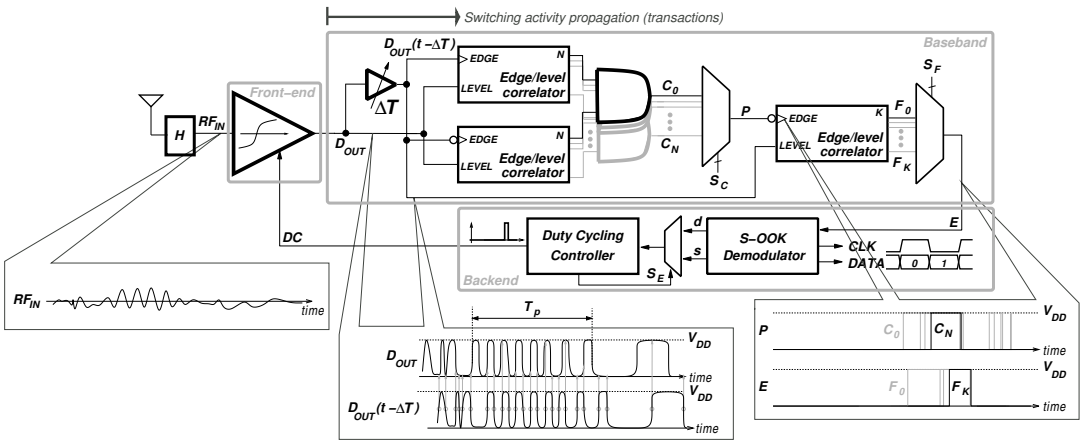

Figure 4. Asynchronous logic receiver architecture.

or multi-user simultaneous transmissions. Moreover it helps decreasing the receiver false alarm probability.

Both delay ΔT and the `Edge/Level Combiners` logic function can be designed based on signal type, the confidence level required to maximize detection probability or to filter out noise and interference. The number of memory elements N or K impacts on the receiver false alarm probability and on signal detection features.

The use of CMOS logic gates, hence an all-digital design enables: 1) **Modeling and simulation based on an event-driven model of computation**. The system can be described with VHDL (or SystemC) which in general enables faster computing time compared to mixed-signal standard co-simulations to explain statistical system operation. 2) **Portability**. The all-digital design can be easily ported and implemented in a different technology processes. 3) **Non-linear front-end amplification**. RF signal amplification is based on front-end saturation and a gain control unit can then be avoided and amplifiers can be designed disregarding typical linearity requirements, i.e. using simple CMOS inverters. 4) **Architectural flexibility and digital-enabled parameterization**. The baseband architecture can be parameterized at VHDL modeling level to enable high-level design space exploration using tools for digital systems design. Moreover, at implementation level statistical measurements can be parameterized, permitting design space exploration based on realistic data. 5) **Radio frequency scaling**. Since radio reception is now considered as a self-timed computing process, the same design, with the same logic elements, in a lower technology node can operate at higher pulses center frequency, with scaled timings. 6) **Process-Voltage-Temperature robustness**. Since pulses are now digitized to a series of digital edges and detection is based on mutually delayed edges sampling, detection can still occur given a propagation delay variation (robustness to center frequency variations).

A. Bit Error Rate Measurements

Fig. 5 shows statistical error-rate performance metric obtained for different pulses center frequency. The Total-Error-Rate (TER) is a statistical error-ratio quantity specific of S-OOK which indicates both synchronization and data errors. It includes both wrong received bits and missed synchronization data. Thanks to the logic receiver architecture the error-rate curves, can be addressed both by input signal power and both by input signal center frequency. The depicted VHDL model data demonstrates that the receiver model, i.e. the internal time constants, can be scaled and normalized, hence made technology independent as in digital circuits. These

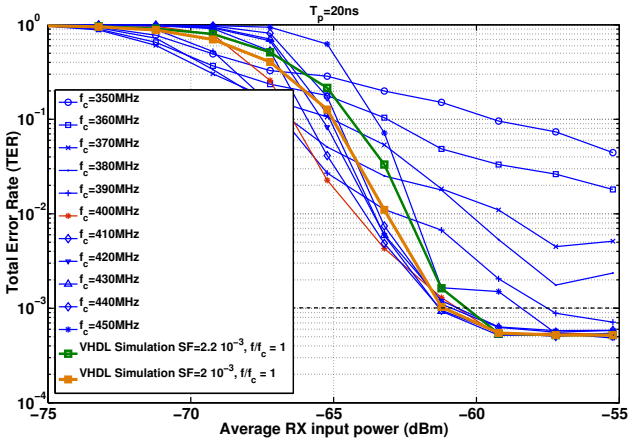

Figure 5. Error-rate measurements with superposed VHDL simulations obtained for different modeling parameters.

error-rate measurements table can be used by the SystemC simulator to implement a statistical model which account for physical bit-level transmission error details.

V. Abstraction Technique

The measured data of Fig. 5 needs to be bridged to antenna simulations including the low-level parameters and impacts on the human body depicted in Sec. III. We then need to extract an equivalent center frequency parameter from the antenna measurements depicted in Fig. 3(c), so that the error-rate figures of merit can be related to the antenna parameters. To account for antenna parameters in the modeling, the radio link needs to be revisited at pulse-level, the abstraction level where the concepts of frequency, received power and human body interactions with the antenna are typically *design entry points*. Fig. 6 schematizes this concept. An information bit needs to be revisited as a unitary *pulse-level token*, i.e. a modulated bit on the wireless channel, statistically independent to the previous. This feature suits perfectly an S-OOK data transmission in which the receiver self-synchronizes with the incoming symbol, independently from the previous.

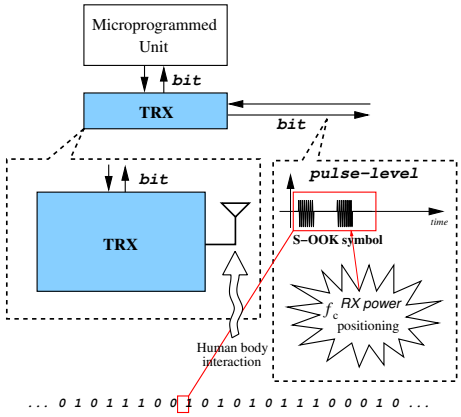

Figure 6. Pulse-level interaction with the statistical bit-level figures of merit.

Fig. 7 shows the additional path loss attenuation due to antenna detuning R as a function of phantom separation and pulses center frequency. This quantity needs to be added to the Friis path loss formula which in turn address the measured error-rate performance figures at RX power and center frequency level. The received signal power is then $P_{RX}(f_c,d,d_p) = P_{TX} + 10n\log_{10}(\frac{d}{d_0}) + R(d_p,f_c)$, where d_0 is 1 m, d is TX-RX separation and d_p is the phantom separation. The quantity $P_{RX}(f_c,d,d_p)$ which now accounts for human body-related physical parameters, can be used to address the statistical error-rate data of Fig. 5.

The quantity R is determined as follows: **For each center frequency** f_c: 1) The measured antenna parameters (Touchstone format) data of Fig. 3(c) is converted into a complex number representation; 2) The mismatch loss $1-|S_{11}|^2$ is calculated (radiated power is not considered because other antenna parameters such as efficiency are not taken into account); 3) Assuming a dumped sine wave hypothesis for the transmitted pulses, the pulses signal power $|U|^2$ is calculated; 3) The quantity $e(d_p) = \int_0^{+\infty}\left(1-|S_{11}(d_p)|^2\right)|U|^2 df$ is determined; 4) The additional path loss is computed as $R = \frac{e(d_p)}{e(\infty)}$, where $e(\infty)$ is the energy of the received pulses assuming free space propagation.

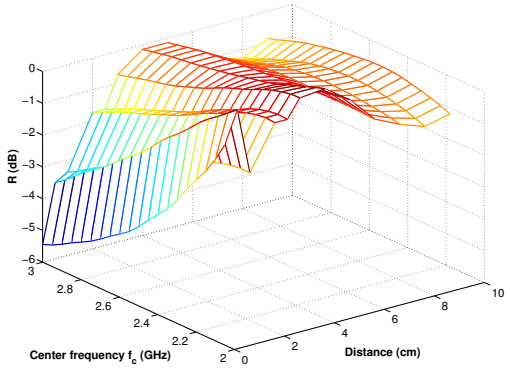

Figure 7. Additional path loss attenuation R resulting from the antenna interaction with the human body.

VI. SystemC Network Simulation Library

Bit error rate and path loss as a function of antenna and receiver design parameters are used to generate some components of the SystemC Network Simulation Library whose architecture is shown in Fig. 8.

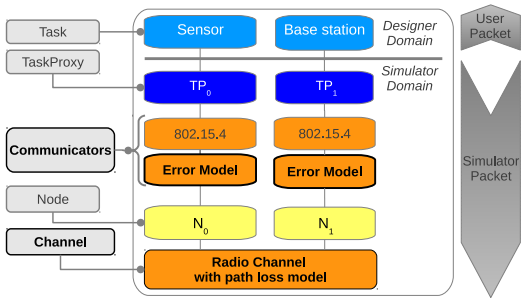

Figure 8. SCNSL internal architecture.

Tasks are used to model node functionality (e.g., sensor node or base station) provided by SW and digital HW components. Thus, tasks shall be implemented by designers either at register transfer or transaction level. From the point of view of the network simulator, a task is just the producer or consumer of packets and therefore its implementation is not important. However, for the system designer, task implementation is crucial and many operations are connected to its modeling, e.g., change of abstraction level, validation, fault injection, HW/SW partitioning, mapping to an available platform, synthesis, and so forth. For this reason the *TaskProxy* is introduced, which decouples task implementation from the backend which simulates the network. This solution ensures

a stable interface between the TaskProxy and the simulation kernel and, at the same time, provides complete freedom in the modeling style for the Task, e.g., as interconnections of basic blocks or behavioral.

Tasks are hosted by *Nodes*, which are the abstraction of physical devices. Thus, tasks deployed on different nodes shall communicate by using the API provided by SCNSL for the network communication, while tasks deployed on the same node shall communicate by using standard SystemC communication primitives (e.g., signals, FIFOs, TLM primitives).

The *Channel* represents the transmission medium, and SCNSL provides models for both wired (full-duplex, half-duplex and unidirectional) and wireless channels. In this work the wireless channel has been used; it simulates various communication aspects, like packet collisions and path loss. In this work the path loss analytical model can be replaced by the curves obtained by modeling the antenna interaction with human body as in the example shown in Fig. 7.

Packet manipulation is a key concept for network simulation. It can be used to implement packet-processing blocks (e.g., queues, tracing or filtering mechanisms) and protocols. The *Communicator* is a SCNSL component implementing a packet-processing interface. New capabilities and behaviors can be easily added by extending this class, i.e., implementing the `send()` and `receive()` methods. Communicators can be interconnected with each other to create packet-processing chains. Each valid chain has on one end a TaskProxy instance and on the other end a Node; hence transmitted packets will move from the source TaskProxy to the Node, traversing zero or more intermediate communicators, then they are transmitted by using a channel model, and cross the communicators between the destination node and the destination TaskProxy. This way, a modification of the transmission behavior is possible by creating a new communicator and placing it between task proxies and nodes. In this work, communicators can be used to implement a bit error injection mechanism according to the curves obtained by the VHDL simulation of the receiver as in the example shown in Fig. 5.

VII. Methodology Evaluation

To evaluate the speed-up of the proposed simulation approach, a WBAN for patient monitoring has been modeled. The star network topology used in this case study is shown in Fig. 1. The base station acts as collector for n sensor nodes. An SCNSL model of the IEEE 802.15.4 [22] wireless protocol has been used; it is configured to operate in unslotted CSMA/CA mode and 16 bit short addresses are used in data packets. Each sensor node performs the following actions every 17 ms: 1) sampling accelerometers, 2) building a 64-byte packet with the raw samples, 3) sending the packet to the base station. Experiments focus on the uplink communication of data packets from sensor nodes to the base station. The simulation is carried out for 10 seconds of simulated time (i.e., 600 packets) and considers up to 16 sensor nodes, which may be placed, for example, on different people in the same room. Fig. 9 shows the execution time of SCNSL simulation as a function of the number of sensor nodes. With 16 sensor nodes the simulation time is about 170 ms on Intel(R) Xeon(R) CPU E5520 @2.27GHz.

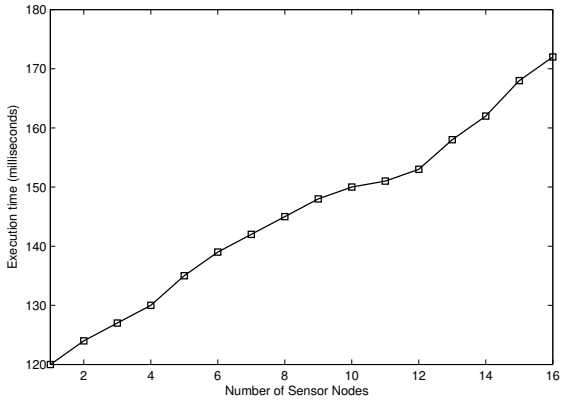

Figure 9. SystemC execution time as a function of the number of sensor nodes.

In case of a standard co-simulation, with very high detail on the digital receiver, simulation time would be very high. To simulate a 10 ns receiver activity with transistor-level detail, SPICE takes about 2 s on the same host platform. To simulate the reception of a packet in presence of channel noise only (disregarding other noise contributions given by the circuit itself), 512 bit, 10 μs symbol time, we would need to run a SPICE simulation lasting 5.12 ms, which would require $\frac{5.1210^{-3}}{10^{-8}} = 51200$ s. In case of the all-digital VHDL model, still requiring co-simulation with models of SW components, execution time is greatly reduced (183 ms per S-OOK symbol, which corresponds to 23.4 s) but still very high compared to the one provided by SCNSL. Both SPICE and VHDL simulations, *inter alia*, regard the transmission of one packet from one sensor node only.

VIII. Conclusion

We have presented a technique which enables the inclusion of physical-level effects in a system-level simulation of a Wireless Body Area Network. The inclusion of physical-level effects led to the organization and the processing of low-level details into the form of a function that links physical-level design parameters to performance figures like bit error rate and path loss. The use of an all-digital receiver for radio reception enables the use of low-level logic parameters directly at high abstraction level, as a result of digital-enabled flexibility. Thanks to intelligent measurement sessions on WBAN antennas, the positioning of the antennas

along the human body can be directly accounted for at system-level thus enabling the simulation of the impact of the antenna on a wireless link performance.

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