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Test and modeling of the hydraulic performance of high-efficiency cooling configurations for gyrotron resonance cavities

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Robust nonlinear models for CMOS buffers

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*Abstract*ô **For over a decade, buffer macromodeling has been a topic of great interest for the integrated circuit industry. The performance assessment of high-speed datalinks requires efficient means of simulating IC ports making compact and accurate behavioral models valuable instruments. In the present communication a new modeling technique, with several important advantages is described. The approach is purely õblack-boxö, relying exclusively on the observation of the external port voltages and currents safeguarding intellectual property. Unlike the standard algorithms currently used in EDA tools, the method described in this paper models the input-output behavior by means of a simple nonlinear system easy to identify and implement. Good model performance in overclocking conditions is an important advantage.**

*Keywords*ô *circuit simulation; integrated circuits; nonlinear circuits; behavioral modeling; IBIS*

I. Introduction

Intricate networks of interconnects exist in electronic systems at all levels. In this complex environment, where electromagnetic compatibility and signal integrity issues are crucial, integrated circuit (IC) buffers act as nonlinear dynamical terminations strongly influencing the shape of signals on the interconnects themselves. Simulating buffers for in-depth investigations is often problematic. Transistor-level descriptions are seldom available. They disclose the internal design and technology of the devices and are not normally released by designers. Even when provided by IC suppliers, in encrypted form, they lack portability, turn out to be computationally greedy and cannot effectively be used in a simulation environment. Owing to this, the best compromise is the development of behavioral models, that attempt to mimic the port electrical behavior of devices and that can be effectively estimated from the observation of the signals at the IC interfaces (see [1-4] and the references therein). The standard solution in IC buffer modelling is offered by the Input/Output Buffer Information Specification (IBIS). IBIS assumes simplified equivalent circuits of typical buffer structures and provides guidelines for collecting the key features of devices (e.g., the static characteristics of the output

port of a buffer, the equivalent capacitance of the silicon die, the parameters of the equivalent circuit of the package,...) [5-6]. A certain number of alternative approaches, complementing IBIS and providing improved accuracy for various device technologies are available in literature [7-14]. However, all the state-of-the-art approaches share common limitations. Some of the most common problems are related to the accurate reproduction of the switching behavior of devices particularly when dealing with overclocking operations or spurious transition events. In their attempt to solve these problems modelers have little space to maneuver. One cannot resort to complicated nonlinear structures that are costly in terms of processor cycles and maybe be difficult to implement on existing circuit simulators. Nor can one rely on cumbersome algorithms for parameter identification, flexibility is a central requirement.

II. A note on the state of the art

Buffer circuits, such as the single-ended example represented in Fig. 1a, basically act as I/O interfaces between the internal core circuitry to the external interconnects. Modeling the behavior of a CMOS device of this type boils down to implementing a nonlinear dynamic mathematical relation binding the input and output port voltages to the output current, e.g. $i_2 = F(v_1, v_2)$. However, most available models simplify the problem by first identifying a model of the output port, e.g. $i_2 = F(v_2)$. A system of weighting functions is then used to account for the influence of the input voltage. In IBIS models (or models generated by similar techniques such as [7-9]) the output current of the buffer writes:

$$i_2(t) = w_H(t)i_H(v_2) + w_L(t)i_L(v_2) \tag{1}$$

where $i_H(v_2)$ and $i_L(v_2)$ are the static characteristics of the output port of the buffer in the fixed high and low state, respectively, and $w_{H,L}(t)$ are weighting functions. The latter are computed numerically from the device responses on two standard loads by solving a least-squares problem (e.g., see [5]

or [6] for details). The models are designed for easy implementation in SPICE with the weighting functions simply embedded as tables. In order for arbitrary binary signals to be fed into the model the weighting functions are cropped and pasted as up-down and down-up transitions unfold.

The main advantage of this approach is simplicity. Model parameters are easily computed from both simulation and measured data (e.g., see [7] and [8]) and the implementation is robust. The main problem is related to inaccuracies, specifically in the case of overclocking-related phenomena. In the following sections we address this problem and suggest a different model topology that solves it, while remaining simple to implement and SPICE-friendly. The test device used throughout the paper is a Texas Instruments 8-bit bus transceiver (model name SN74ALVCH16973, nominal power supply voltage $VDD = 2.5$ V). Its SPICE transistor level description is available on the vendor's official website and was used to compute the reference waveforms. The power supply voltage is considered constant throughout the paper.

III. A NEW PARADIGM
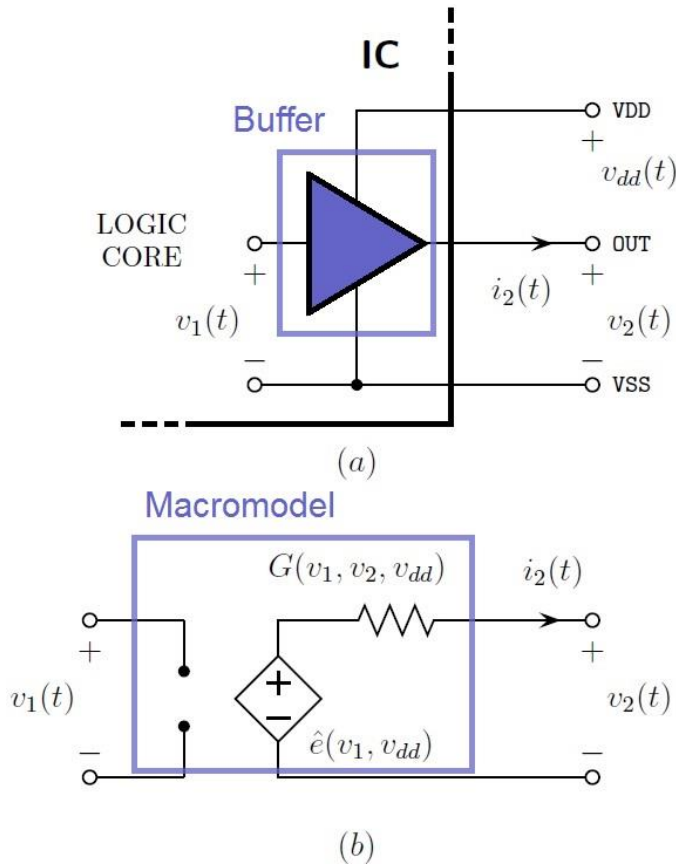
A. General theoretical framework

(a)

(b)

Fig. 1. a) General structure of an IC buffer; b) Macroodel topology

The method described in this paper is centered on the structure of Fig. 1b, where v_1 is the input voltage, v_2 is the output voltage, $\breve{e}(v_1)$ is the open circuit voltage response of

the device and $G(v_1, v_2)$ is a nonlinear conductance. The authors were inspired by the well-known Thevenin equivalent model of linear circuits and imagined a similar, nonlinear structure, adapted for approximating the behavior of CMOS buffers.

In order to simplify model extraction a reasonable assumption is made. Let the conductance $G(v_1, v_2)$ be written as a weighted sum given by equation (2).

$$G(v_1, v_2) = p_H(v_1)G_H(v_2) + p_L(v_1)G_L(v_2)$$
$$= \left(\frac{\breve{e}(v_1)}{VDD}\right)G_H(v_2) + \left(1 - \frac{\breve{e}(v_1)}{VDD}\right)G_L(v_2) \quad (2)$$

where $G_H(v_2)$ and $G_L(v_2)$ are the nonlinear conductances associated to the fixed high and low output state, respectively. The idea is to capture, by using a simple mathematical model, the change of the buffer's output impedance with respect to the variation of the input signal driving the buffer. Note that (2) uses $\breve{e}(v_1)$ as a weighting function in order to account for switching. This is consistent with the physics of CMOS circuits. The gate voltage intrinsically acts as a weighting function for the output current during switching events and is closely related to the open circuit-output voltage.

Now consider Fig. 1b and equation (2). In this case, the expression of the output current can be cast as follows.

$$i_2(t) = G(v_1, v_2)(\breve{e}(v_1) - v_2)$$
$$= p_H(t)(\breve{e}(v_1) - v_2)G_H(v_2) + p_L(t)(\breve{e}(v_1) - v_2)G_L(v_2) \quad (3)$$
$$= p_H(t)f_H(v_1, v_2) + p_L(t)f_L(v_1, v_2)$$

Note the similarity between equations (1) and (3). From a modeler's point of view it is reassuring to note that the top-down approach described here (from circuit theory to macromodel) finally leads to a paradigm similar to the IBIS one obtained by a bottom-up approach (from transistor model to macromodel). Note, however that the only explicit link to the input voltage in the two submodels i_H and i_L of (2) is the presence of the fixed high and low state nominal voltages, VDD and 0 respectively. In the case of (3) instead, the inclusion of $\breve{e}(v_1)$ in f_H and f_L provides a stronger link to the input port and leads to better accuracy during switching events.

With the general framework set, model parameters have to be determined in purely "black-box" manner.

B. Submodel identification

The first issue that needs to be addressed is the modeling of $\breve{e}(v_1)$. It may be tempting to use a technique similar to the one implemented in IBIS-based EDA tools, namely, concatenated, properly trimmed, pre-recorded voltage curves describing typical up-down and down-up transitions in order to simulate drivers for arbitrary input signals. However, this approach,

while being robust, is also responsible for the inaccurate behavior observed in IBIS models used in overclocking conditions and the authors discarded it. Instead a parametric non-linear model structure of the Hammerstein type was chosen. It is described in Fig. 2. The open circuit voltage $\breve{e}(v_1)$ is modelled as a cascade of three blocks. The first block is purely static and consists in a table-based model simply mapping the static open-circuit input-output characteristic of the buffer. The second block is a linear filter and the third block is an ideal delay line accounting for the measured delay of the device in open circuit.
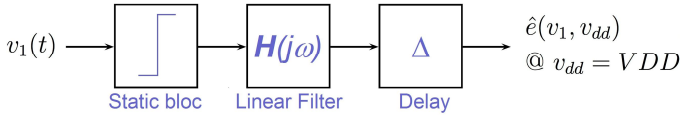

$v_1(t) \longrightarrow$ [Static bloc] $\longrightarrow$ [$\boldsymbol{H(j\omega)}$ Linear Filter] $\longrightarrow$ [Δ Delay] $\longrightarrow \begin{array}{l}\hat{e}(v_1, v_{dd}) \\ @ \ v_{dd} = VDD\end{array}$

Fig. 2. Submodel implementing $\breve{e}(v_1)$

The second issue concerns conductances $G_H(v_2)$ and $G_L(v_2)$ of (2). These are determined via a DC analysis with an ideal voltage source v_2 connected to the output port of the buffer. The buffer is locked in on or off state respectively, and the conductances are computed via Ohm's law according to $G_{H,L} = i_2 / (\breve{e}(v_1) - v_2)$. They are simply embedded in the SPICE netlist of the model as tables. It is relevant to remark that model parameters, i.e. $\breve{e}$ and $G_{H,L}$, can also be computed from actual measurements performed on a real device, with standard solutions for the test fixture.

C. Practical Implementation

The extraction and implementation of the Thevenin-like model is summarized below.

- Step 1. With the driver in open circuit, run a DC sweep of v_1 in order to extract the static input-output characteristic $v_2(v_1)$ and implement the first block in Fig. 2. This is a simple two column table that can be easily embedded in a SPICE sub-circuit.

- Step 2. Run a transient simulation of the driver, in open circuit, using a step stimulus for v_1. Measure the delay exhibited by the v_2 response and extract it. Compute the derivative of the un-delayed (shifted) step response and, subsequently, obtain the frequency response $H(j\omega)$ by simple FFT.

- Step 3. Use vector-fitting [15], [16] to obtain a rational fit of the frequency response $H(j\omega)$ of the filter and generate the equivalent SPICE model. Embed the delay by using an ideal transmission line. At the point $\breve{e}$ is completely modeled.

- Step 4. Run two DC sweeps on the driver output port with the device locked in on and off state respectively in order to extract the $i_2(v_2)$ characteristics.

- Step 5. Compute G_H, and G_L, from the $i_2(v_2)$ characteristics using Ohm's law, embed the results as tables in spice sub-circuit. At this point both elements of the Thevenin-like circuit are fully modeled.

It's worth noting that steps 2) and 3) could be modified to allow a direct identification in time domain using time-domain vector fitting [17].

IV. SIMULATION RESULTS

In this section, the Thevenin-like model is used to simulate a realistic interconnect structure consisting of the driver connected to a distributed load defined by a transmission line with a 60 Ohm characteristic impedance and 100 ps delay. The transmission line is terminated by a lumped equivalent of a receiver circuit represented by the shunt connection of a 7 pF capacitor.

The responses of the driver, of the Thevenin-like model and of an IBIS model are shown in Fig. 3. The stimulus is a typical binary sequence including one very fast up-down-up transition and one very fast down-up-down transition. There is a very good agreement between the Thevenin response and the reference while the IBIS response exhibits misalignment phenomena each time a spurious transition occurs.

This is not surprising, the crop-and-paste IBIS strategy has an intrinsic problem at high frequencies and this is precisely the issue that the Thevenin approach presented here addresses.

Statistically relevant tests record an average $10 \times$ speed-up was for the Thevenin-like model with respect to the reference. The user has some leverage on the speed vs. accuracy trade-off by adjusting the order of the linear filter in Fig. 2. or the resolution of the different static mappings. This further confirms the strength of the proposed method and it's worth noting that the speed-up is independent of the complexity of the original transistor model.
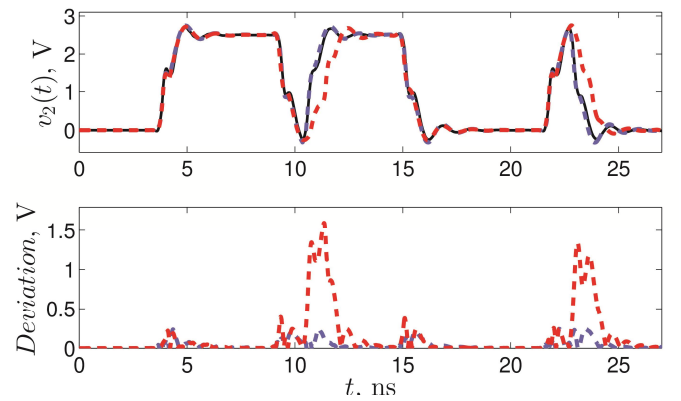

Fig. 3. Output port voltage response of the example buffer loading an transmission line with 60 Ohm characteristic impedance, 0.1 ns delay and a far end 7 pF capacitor. Solid black: reference response; dashed blue: Thevenin model prediction; dashed red: IBIS model prediction.

V. ADDITIONAL REFINEMENTS

The main purpose of this communication was to present an articulated proof of concept and it was the authors' intention to

keep the modeling framework as simple as possible. Several refinements and improvements may be considered in order to increase modeling accuracy. The first one concerns the passive element $G(v_1, v_2)$. Its definition could be in order to take into account the dynamic behavior of the output port, mainly the output capacity. A õcompensation capacityö may simply be added, for example, as in the case of IBIS models. A more daring approach would be to abandon the two-submodel hypothesis and attempt to identify $G(v_1, v_2)$ as a single nonlinear multiple-imput-single-output function. This strategy would not modify the general theoretical framework presented in this paper and may bring significant advantages in terms of accuracy. The main caveat concerns model complexity and robustness.

On a more general level, the Thevenin-like model in Fig. 1b. could be implemented in various ways. The identification of the $\check{e}(v_1)$ block, for example, is a classical single-input-single-output dynamic system identification problem and a plethora of methods is available in academic literature: neural networks, polynomial filters or various heuristics (e.g., see [18-20]). Note though that the Hammerstein structure has the advantage of being simple and robust.

Finally it would be interesting to include the variations of the power supply-voltage in the model. This could be achieved by including correction coefficients accounting for the variations of the power supply.

VI. CONCLUSION

The present communication addresses the subject of IC buffer macromodeling and provides both a new theoretical framework and the methodology required to implement it. Implementation is, indeed, a crucial issue. The approach is SPICE-friendly; it can be integrated in any EDA tool just as easily as current mainstream techniques. All the required system-identification tools are off-the shelf, no cumbersome or exotic algorithms are required. The results presented in section IV demonstrate the modeløs accuracy and the potential improvements discussed in section V should lead to further refinements of the technique in the near future.

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