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Original
First study of SEU in ToPix4 / Calvo, D., De Remigis, P., Mazza, G., Olave, E.J., Silvestrin, L., Wheadon, R., Zotti, L.. - In: LNL- ANNUAL REPORT. - ISSN 1828-8561. - ELETTRONICO. - LNL Annual Report 2014:107(2014), pp. 107-108.

Availability:
This version is available at: 11583/2642646 since: 2016-09-15T14:13:42Z

Publisher:
LNL Annual Reports

Published
DOI:

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28 November 2026

First study of SEU effects in ToPix4

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INTRODUCTION

ToPix4 is the 4th generation custom prototype developed for the readout of the silicon pixel devices for the Micro Vertex Detector [1] of the PANDA [2] experiment.

ToPix4 provides position, time information and energy measurement of the incoming particles and it is developed according to the trigger-less data acquisition system planned in the experiment. The ASIC is designed in a 130 nm CMOS technology and it includes 640 readout cells of 100 μm^2 x 100 μm^2 sizes. The Time over Threshold technique (ToT) is implemented to perform energy loss measurements. The 160 MHz master clock signal is used as a reference for event time measurement. Single Event Upset (SEU) protection techniques are applied for the digital parts.

THE PROTOTYPE

ToPix4 [3] features a die size of 6 mm x 3 mm and includes 4 double columns: two 2 x 32 cells external columns and two 2 x 128 cells central columns , folded in four 2 x 32 cell columns, thus obtaining a final matrix of 20 x 32 cells. Figure 1 shows the prototype wire bonded to its testing board.

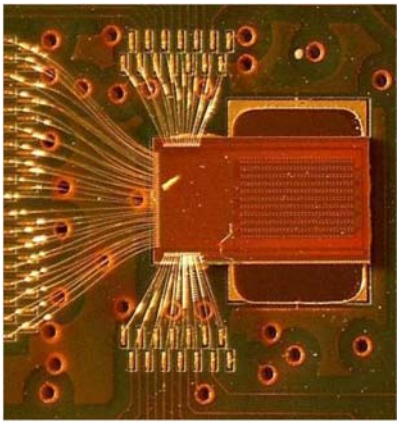

Fig. 1. ToPix4 on its testing board with the wire connections.

Each readout cell includes a preamplifier controlled by a baseline restorer and a constant current discharge circuit, followed by a comparator. A digital control unit detects the rising and falling edges of the comparator output and stores in two 12-bits registers the corresponding time stamp values. In particular the common time information to all the cells is provided by a timestamp bus driven by a counter. The timestamp bus is also used to upload the 8-bit pixel configuration register value during the chip configuration phase.

The comparator rising edge gives the event time stamp, meanwhile the duration of the comparator output is a linear measurement of the integrated charge and therefore the difference between the trailing and leading edges time stamps provides the ToT measurement.

Each double column is connected to a 32-words FIFO via sense preamplifiers. Then the 4 FIFOs are readout by the control chip unit that send out data using a 320 Mb/s serial link based on the SLVS standard.

To mitigate SEU effects several techniques were applied to the digital parts of the ASIC [4].

The DICE (Dual Interlocked Cell) architecture is implemented in the data registers since it provides a sufficient protection of the data information without an excessive area penalty.

Different techniques have been used for the pixel configuration register. Half of the matrix implements D-type Flip-Flops (DFF) circuits with the Triple Modular Redundancy (TMR) error detection and correction circuitry, while the second half of the matrix uses Hamming encoding that detects and corrects errors. This solution has been adopted in order to explore the best trade off of the area vs protection level.

In the FIFO each 32-bits cell has been implemented with 37 DFF in order to implement a single error correction Hamming encoding. This technique is less demanding in terms of space than the TMR, especially with large number of bits per data word. No attempt is made to correct the error before the data is readout from the FIFO.

The same Hamming encoding is used for the state machines that controls the data flow in the chip logic. Each state is encoded with a specific bit sequence in such a way that the minimum Hamming distance between two valid codes is 3. A non valid code is then assumed to be a single bit error and therefore equal to the closest valid code. In this implementation a wrong state due to an upset is corrected in the following clock cycle, without waiting for the next state transition.

EXPERIMENTAL SETUP

The setup for testing ToPix4 is based on a Xilinx Virtex-6 ML605 Evaluation Kit board, connected to the ToPix4 test board via a flat cable. The readout board provides all the data and control signals except the clock

and a counter reset signal that can be used for time stamp synchronization of multiple boards when the system is used in beam test. The readout board is connected to a computer via a UDP link and is controlled by a LABView program.

In the SEU tests the pixel configuration register is periodically read-out and compared with the value stored at the beginning of the run. If an error is detected, it is recorded and the correct value is re-written in the register.

The Hamming decoders in the output FIFOs and in the state machines generate an error signal every time a wrong code is detected. These error signals are put in logical OR inside the chip and sent out via a dedicated output pin (SEU_err_fsm). The acquisition program counts the number of time when the error line goes to one, therefore obtaining the number of errors which have been detected and corrected.

RESULTS AND CONCLUSIONS

In July 2014, a test at the SIRAD facility gave the first evaluation of the SEU errors for the configuration registers of ToPix4. Several ions were used and some tilted configurations (20° and 30°) in addition to the perpendicular one between the chip and the ion beam, namely 0°, were tested. Similar results were obtained for the two different types of pixel configuration register SEU. Indeed in figure 2 the SEU error ratio between Hamming encoding and TMR is about 1 for the most of ions and tilted configurations. In the case of the C ion, the SEU error of the Hamming encoding part was zero while for the ion F at 0° it is about 3 times higher than TMR's one.

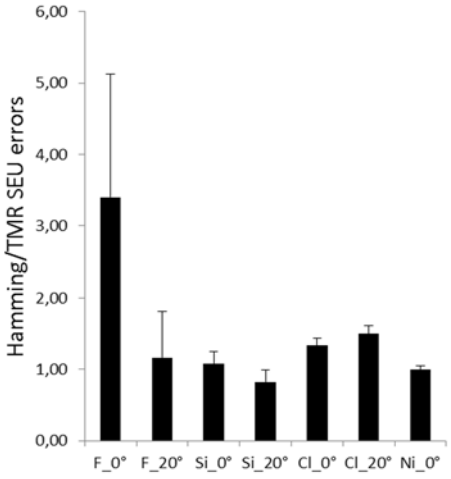

Fig. 2. SEU errors ratio between the Hamming encoding and TMR.

The experimental points corresponding to the total number of the detected SEU errors in all the configuration registers of ToPix4, normalized to the bit number, are reported for several ions in figure 3. With C ions (1.5 MeV cm^2/mg LET), a few SEU errors were detected in the TMR part, while no errors had been detected in the previous prototype ToPix3 with N ions (2.23 MeV cm^2/mg LET) [5]. This low LET region will require more focused studies at higher ion fluence in order to be understood.

The points corresponding to the SEU_err_fsm signal values, normalized to the bit number, are reported in figure 4.

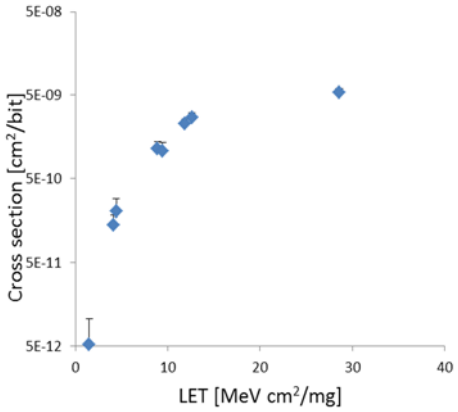

Fig. 3. SEU cross section of the ToPix4 configuration registers.

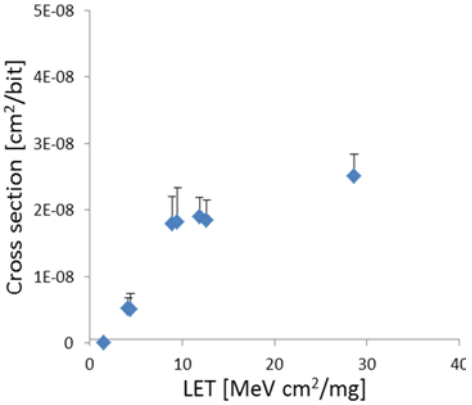

Fig. 4. SEU cross section of the ToPix4 FIFO circuits.

No errors have been detected with ion C. The higher asymptotic value of the SEU cross section can be explained taking into account that these experimental points correspond to the total number of errors before any correction.

ACKNOWLEDGEMENTS

The authors would like to tank M. Tessaro for his continuous support to the data taking. A special acknowledgment to M. Mignone and F. Dumitrache for their professionalism in preparing the ToPix4 setup.

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