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ABSTRACT: ToPiX v4 is the prototype for the readout of the silicon pixel sensors for the Micro Vertex Detector of the PANDA experiment. ToPiX provides position, time and energy measurement of the incoming particles and is designed for the triggerless environment foreseen in PANDA. The prototype includes 640 pixels with a size of 100×100 μm^2, a 160 MHz time stamp distribution circuit to measure both particle arrival time and released energy (via ToT technique) and the full control logic. The ASIC is designed in a 0.13 μm CMOS technology with SEU protection techniques for the digital parts.

KEYWORDS: Radiation-hard electronics, Front-end electronics for detector readout, Digital electronic circuits.

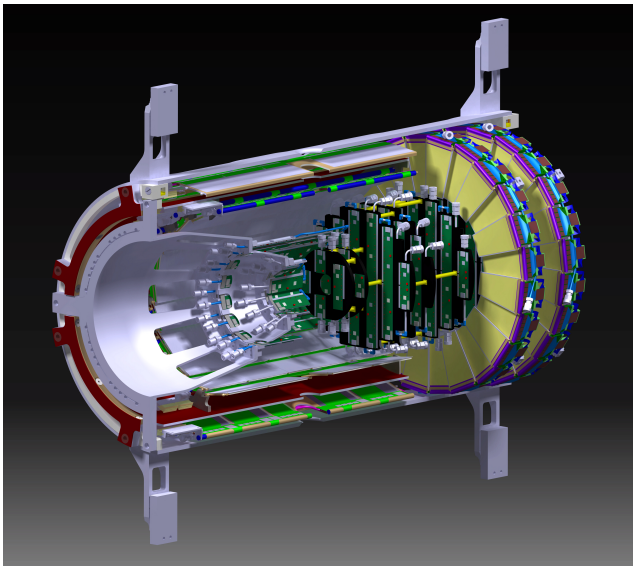

Figure 1. The PANDA Micro Vertex Detector (MVD)

1. Introduction

PANDA [**?**] is one of the main experiments foreseen at the future FAIR facility under construction on the area of the GSI research centre at Darmstadt, Germany. The facility will provide intense secondary beams of antiprotons and rare isotopes which will be used for research at the main experimental setups.

The PANDA experiment will make use of antiprotons in the momentum range from 1.5 GeV/c to 15 GeV/c, which will be directed onto a proton or nucleus target. The consequent annihilation reaction will allow the high precision spectroscopy of the charmonium system and the production of hypernuclei. The beam structure is divided into 2 µs bursts with an 80% duty cycle.

The PANDA apparatus is composed of two spectrometers : the Target Spectrometer, surrounding the interaction point, which will be used to detect particles emitted at large angles, and the Forward Spectrometer, located immediately after the interaction point, for small angle tracks. The pipe for the injection of target material will therefore cross the target spectrometer perpendicular to the beam pipe. Moreover, a silicon vertex detector will surround the interaction point.

2. The PANDA Micro Vertex Detector

The design of the Micro Vertex Detector (MVD) [**?**] is optimized for the detection of secondary vertices from D and hyperon decays and maximum acceptance close to the interaction point. It will also strongly improve the transverse momentum resolution obtained with the tracking system of the experiment. The setup is depicted in figure **??**.

The MVD is based on hybrid silicon pixel detectors (SPD) and double-sided silicon strip detectors (SSD). The layout foresees a four layer barrel detector with an inner radius of 28 mm and an outer radius of 120 mm. The two innermost layers will consist of SPDs while the outer two layers will be made of SSDs. Six detector wheels arranged perpendicular to the beam will achieve

the best acceptance for the forward part of the emitted spectrum. Here the inner four layers are made entirely of SPDs, while the following two are a combination of SSDs on the outer radius and SPDs closer to the beam pipe.

The SPDs will be based on the well-known hybrid pixel technology in order to cope with the radiation levels foreseen in PANDA. The p-in-n configuration on an epitaxial substrate has been chosen for the sensor [**?**]. The pixel matrix will be connected via bump bonding to a custom ASIC, designed at INFN Torino, which will measure the position, arrival time and deposited charge of the particle crossing the sensor.

The sensor and the corresponding readout chips, toghether with the interconnection cable, is assembled in structures called modules. In the foreseen readout architecture, shown in figure **??**, each module is powered by a radiation tolerant DC-DC converter [**?**] and sends and receives data and clock from the GBT radiation tolerant optical transceiver [**?**]. These two groups of boards are placed close to the MVD barrel in the backward direction.

3. The ToPiX ASIC

The ToPiX ASIC is a custom development in 0.13 µm CMOS technology for the readout of the PANDA SPDs. It will consist of a 116 × 110 pixel matrix arranged in 55 double columns and controlled by the same number of column controllers, and a Chip Control Unit (CCU) which multiplexes the data from the column controllers and send them to the GBT board via two 320 Mb/s serial links. The main ToPiX specifications are summarized on table **??**.

The current prototype features 640 cells with the full pixel cell divided into 8 columns, 4 complete column controllers and a simplified CCU with a single output serial link.

Figure **??** shows a simplified schematic of the pixel cell. A preamplifier with a 4.9 fC feedback capacitor and a constant current discharge circuit is followed by a comparator. A digital Control Unit detects the rising and the falling edges of the comparator output and stores the value present on the time stamp bus in correspondance to the two edges in two 12-bits registers. The time stamp bus is used to distribute a common time reference to all the columns and therefore its value at the

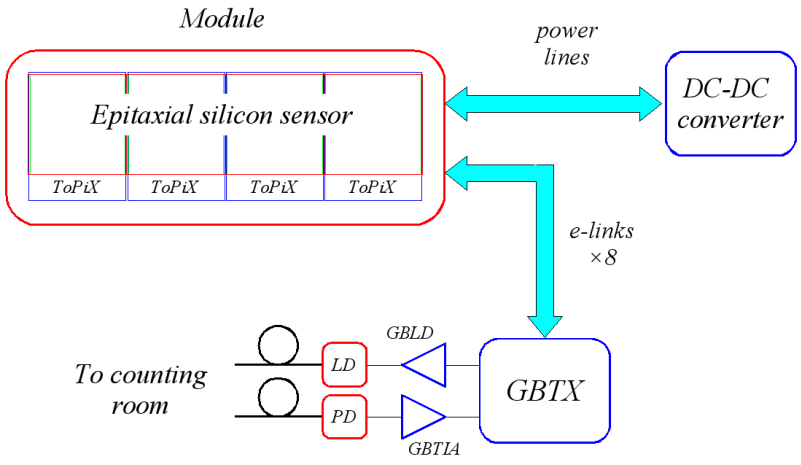

Figure 2. Pixel module architecture

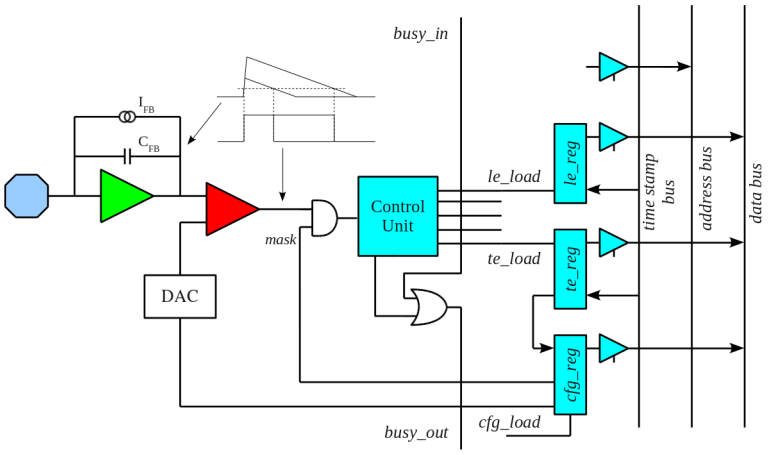

Figure 3. Pixel cell simplified schematic

comparator rising edge time gives its arrival time. Due to the linear discharge of the integrating capacitor, the duration of the comparator pulse is a linear measure of the integrated charge and therefore the difference between the trailing and leading edge time stamps provides a measure of the charge released by the particle in the detector. This analog-to-digital conversion technique is known as Time-over-Threshold (ToT) [**?**].

When both leading and trailing edge time stamp information have been loaded in the corresponding pixel registers, the Control Unit issues a busy signal which is propagated to the column controller via a fast-OR chain. The column controller then enables the hit pixel to write its address and data on the corresponding readout bus. The readout priority among pixels is fixed and is given by the busy fast-OR chain.

The pixel cell logic is fully asynchronous, thus avoiding the propagation of the 160 MHz clock to the full matrix. It includes a configuration register to control the comparator threshold fine tuning, the pixel masking and the test features. The time stamp bus is used to upload the configuration register value during a configuration phase which has to be executed before the data taking phase. The configuration register is not directly connected to the time stamp bus, but is

Table 1. ToPiX main specification

Pixel size	100 µm × 100 µm
Chip active area	11.4 mm × 11.6 mm
dE/dx measurement	ToT, 12 bits dynamic range
Max input charge	50 fC
Preamplifier noise	< 32 aC (200 e^-)
Input clock frequency	160 MHz
Time resolution	6.25 ns (1.8 ns r.m.s.)
Power consumption	< 800 mW/cm^2
Max hit rate	6.1 $\times 10^6$/cm^2
Total ionizing dose	< 100 kGy

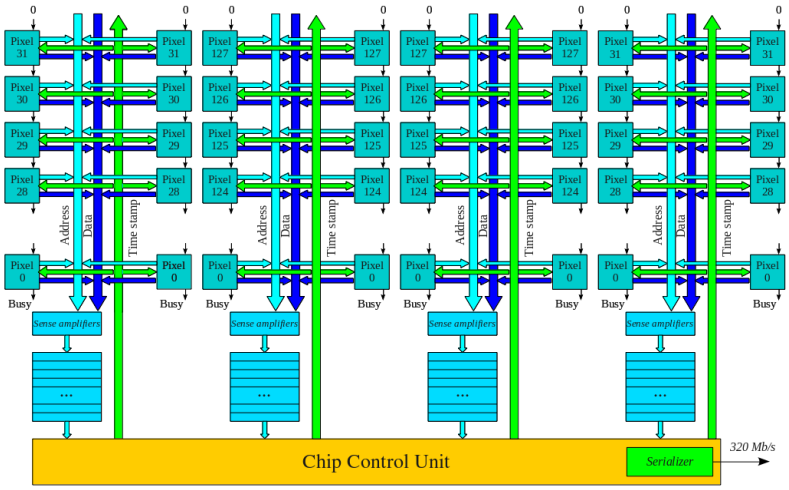

Figure 4. ToPiX v4 schematic

loaded via the trailing edge register in order to decrease the capacitive load on the bus.

In the ToPiX v4 prototype the 640 pixel cells are organized in four double columns. The two central columns consist of 2×128 pixel cells, while the two external are four times shorter, i.e. 2×32, as shown in figure **??**. This double size column arrangement has been chosen in order to decouple possible problems related to the data transmission on the time stamp, address and data buses from other issues. Indeed the estimated total capacitance and resistance of the bus is 50 fF/cell and 9 Ω/cell, respectively. The RC delay is therefore critical, especially for the transmission of the time stamp. Various techniques, ranging from differential transmission with reduced swing, pre-emphasis and Gray encoding have been adopted in order to guarantee the correct time stamp propagation.

As shown in figure **??**, the double column readout buses are connected to a 32-words FIFO via sense amplifier (to improve the readout time). The four FIFOs are read-out by the CCU, which send out the data via a 320 Mb/s serial link based on the SLVS standard. The CCU also provides the time stamp generation and the upload of configuration data via a dedicated serial interface.

The ToPiX v4 prototype has been designed in a commercial 0.13 µm CMOS technology and tested. The die size is 6 mm × 3 mm. The 2 × 128 cells columns have been folded in four 2 × 32 cells columns, thus obtaining a 20 × 32 cells matrix, which copes better with the available sensor prototype [**?**]. The column folding requires three extra U-shaped bus interconnections, thus making the data transmission over the bus more critical in the prototype compared to the final ASIC. Figure **??** shows the layout of the ToPiX v4 prototype. The ToPiX digital interface pads are all differential and located on the right side of the die. Analog bias and test pads are placed on the top and bottom sides of the die, and are grouped in the rightmost position in order not to interfere with the detector guard ring. These pads will not be present in the final ASIC as the corresponding bias lines will be controlled by internal DACs.

4. Test results

ToPiX has been tested via a Xilinx Virtex-6 ML605 Evaluation Kit board [**?**]. The readout board is

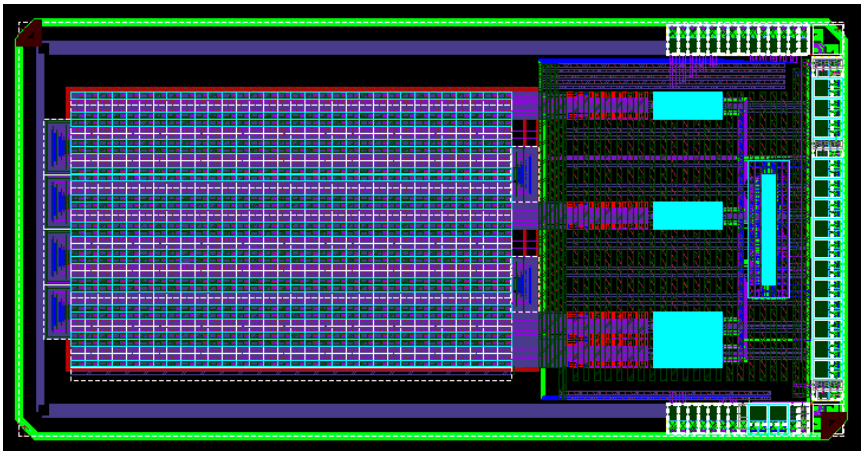

Figure 5. ToPiX v4 layout

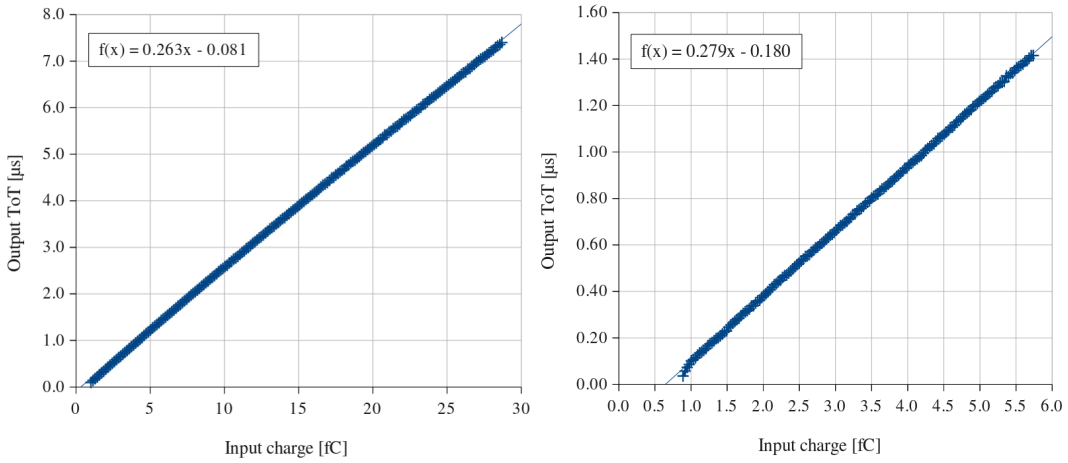

Figure 6. ToPiX v4 linear range

connected to a computer via a UDP link and is controlled by a LabView program.

Figure **??** shows the ToT as a function of the input charge for both the full input range (on the left) and for charges below 6 fC (on the right). The measurements are taken with a threshold voltage of approximately 0.25 fC and are averaged over the 640 pixels of a single chip. The circuit shows a good linearity down to about 0.8 fC. The ToT gain is 0.26 µs/fC, in good agreement with the 0.23 µs/fC obtained from simulation.

Figure **??** left shows the voltage noise at the input of the comparator taken with the S-curve method. An average value of 0.78 mV is obtained, which corresponds to an input referred charge of 6.34 aC with the simulated preamplifier gain. This value is compatible with the 6.86 aC of the quantization noise and thus shows that the preamplifier noise has practically no influence on the measurement of the leading edge.

On the other hand the noise has much more effect on the measure of the trailing edge since the discharge slope is much more gentle. As shown in figure **??** (right), the sigma of the ToT measurement (which is dominated by the trailing edge) corresponds to an input referred charge

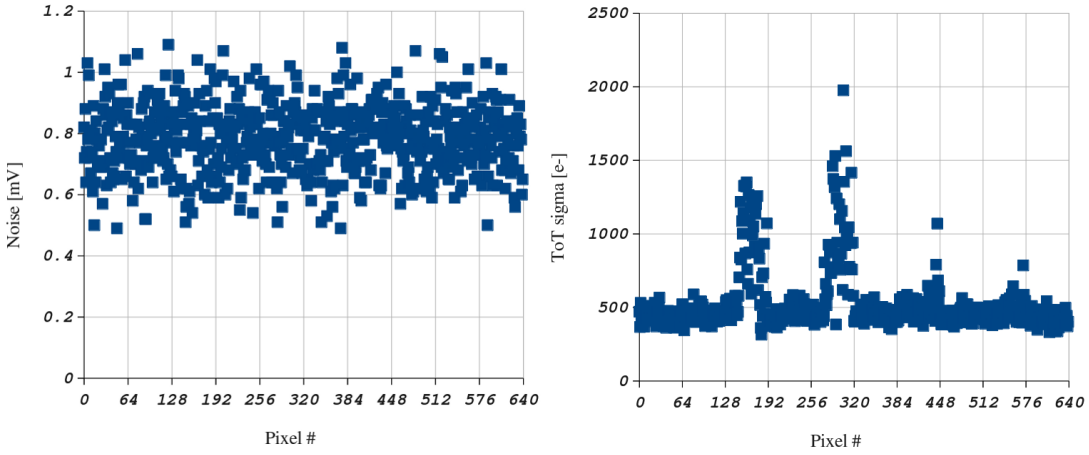

Figure 7. ToPiX v4 time and ToT noise

noise of 0.08 fC. It can be also observed that some pixels show a ToT noise much higher than the average (up to four times). A more detailed analysis has shown that the problem is due to a digital transmission problem for the farthest pixels from the end of the column. For these pixels the probability of reading a bit 0 on the bus LSBs is significantly higher than reading a bit 1, and this translates into a higher ToT sigma. As expected, the two shorter columns (2×32 cells), corresponding to pixel numbers 0-63 and 576-639, respectively, are not affected by this problem. Moreover, from figure **??** (right) it can also be observed that the readout problem is more severe for the first two long columns (corresponding to pixel ranges 64-191 and 192-319) than for the last two (320-447 and 575-639). This effect is due to the fact that the first half of the matrix uses Triple Modular Redundancy (TMR) as a SEU protection scheme, while the second half uses Hamming encoding. The TMR scheme leads to a slightly higher capacitive load on the bus and therefore an higher number of critical cells.

These measurements show that the data transmission on the column bus is still a critical issue and some improvement will be required in the final version. However, as mentioned before, the ToPiX v4 prototype has 12 more cells per column than the final verson and the bus traces are longer due to the folding.

Figure **??** left shows the baseline residual variation after individual pixel calibration via the internal DAC. The average baseline value is 727 mV with a sigma of 0.73 mV. On the right side of the same figure the ToT slope variation is reported. The previously described issue related to the transmission problem for the cells at the end of the long columns is clearly visible as an increase of ToT slope variation.

The measured power consumption of the ToPiX v4 prototype is around 120 mW for a power supply of 1.2 V and a clock frequency of 160 MHz. The contribution of the analog power is quite small (6.5%) while a large fraction (41%) is taken by the SLVS drivers and receivers as well as by the circuits to drive and readout the column buses (30%). From these data the power density of the full size ToPiX can be estimated to 725 mW/cm^2, thus matching the requirement.

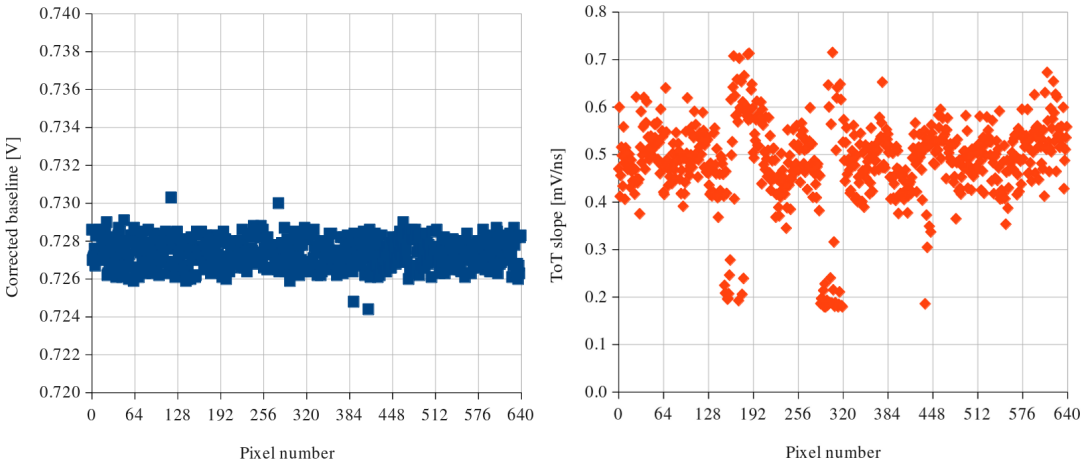

Figure 8. ToPiX v4 baseline and ToT slope variation

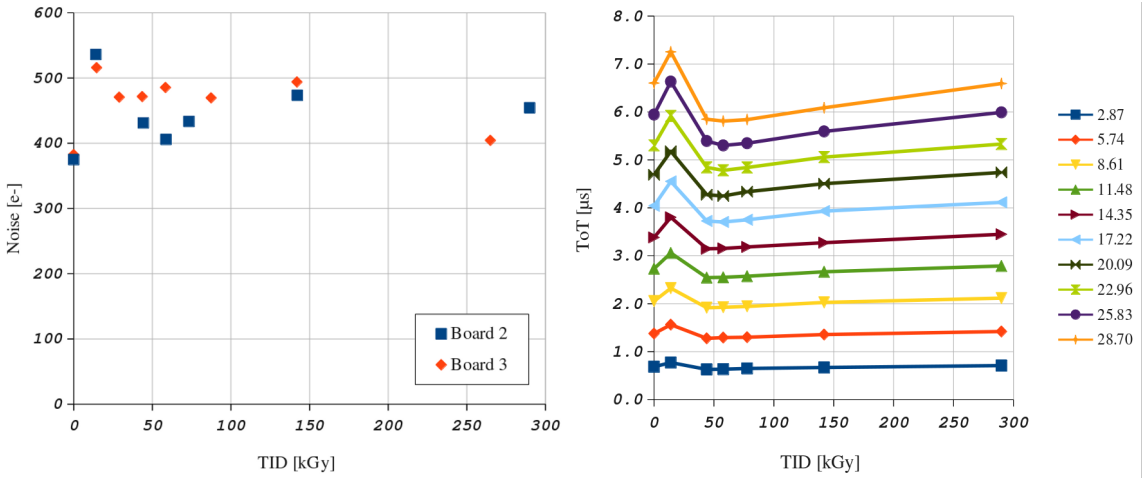

Figure 9. ToT noise and ToT variation (for different input charges) with irradiation

5. Radiation test results

5.1 TID effects

The ToPiX ASIC will have to withstand a maximum integrated dose of 100 kGy. In order to assess its radiation tolerance, two ToPiX v4 prototypes have been irradiated for Total Ionizing Dose (TID) effects with 10 keV X-rays up to a dose of 300 kGy (SiO_2) at the CERN PH-ESE X-ray irradiation facility.

Figure **??** left shows the average ToT noise variation as a function of the dose for the two boards. A 30% increase around 10 kGys has been observed. Above that value, the noise remains constant or slightly smaller. Figure **??** right shows the measured ToT as a function of the dose for different input charges. An increase of the ToT gain around 10 kGys is observed. As in the previous case, the increase is recovered for higher doses.

The TID tests show that the variation of the ToPiX main parameters are, albeit not negligible,

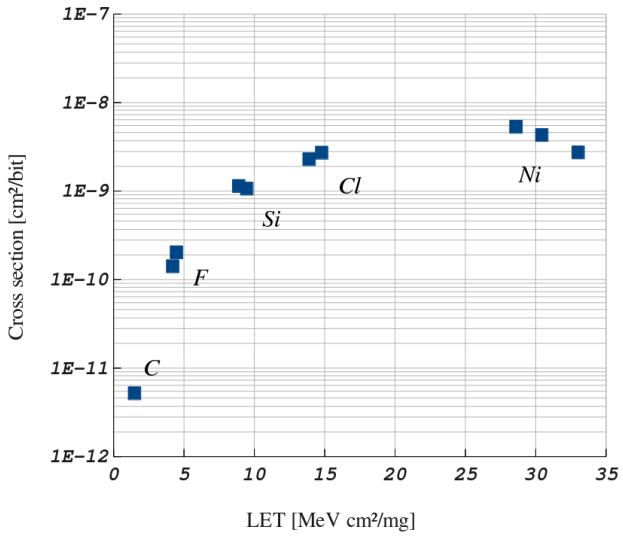

Figure 10. Cross section of the pixel configuration registers

compatible with the requirements of the experiment. The effects observed in the 10-20 kGy region are realated to an increase of the leakage currents, and are explained in more details in [**?**]. A ToT gain calibration will be probably required to compensate for the gain changes in the first 10-20 kGy.

5.2 SEU effects

The ToPiX ASIC has been exposed to several ions beams at the INFN Sirad facility at Laboratori Nazionali di Legnaro. The ASIC was placed in a vacuum chamber during irradiation while the pixel configuration registers were periodically written and read-out. Results are shown in figure **??** for different ions and different angles between the beam and the chip plane ($90^o, 70^o$ and 60^o). The results are similar to those obtained with the same technology and automatic place and route based TMR protection scheme [**?**]. No significant difference between Hamming encoding and TMR has been observed.

In parallel, test pulses were injected and data readout was performed during irradiation. The acquisition worked without interruptions, thus showing that the Hamming protection on the finite state machines works properly. On the other hand, errors were observed in the data. A detailed data analysis is still ongoing.

6. Conclusions

The reduced size prototype of the readout ASIC for the PANDA MVD pixel detector has been designed and tested. Analog performances satisfy the requirements. Correct operation at 160 MHz has been proved, albeit column data transmission is at the limit and some margin has to be added. TID and SEU tests show that the ASIC can work in the radiation environment foreseen for the PANDA experiment.

Acknowledgments

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