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06 May 2026

A Digital-Based Virtual Voltage Reference

Paolo S. Crovetti, *Member, IEEE*

***Abstract*—A novel *virtual reference* concept is introduced in this paper to design accurate, mostly digital, software-defined, process-supply-and-temperature (PVT)-independent voltage references suitable to replace conventional analog reference circuits in present day, low voltage, aggressively scaled, mainly digital integrated systems. The operation and the performance of references based on the proposed approach are tested by computer simulations and experiments carried out on a proof-of-concept, microcontroller-based prototype, reporting a measured thermal drift of 16 ppm/°C in a range from -10°C to 100°C and a line regulation of 0.15%/V. The advantages in terms of costs and performance of the proposed digital references in comparison with state-of-the-art analog solutions are finally discussed.**

***Index Terms*—Virtual Voltage Reference, Digital-Based Analog Circuits, Digital Bandgap Circuit, PVT-independent Reference.**

I. Introduction

REFERENCE voltages and currents are essential in present-day mainly digital electronic systems as the *measurement standards* in terms of which any other voltage and current are directly or indirectly compared, whenever their absolute value is associated to relevant information or needs to be controlled. The precision of references and their stability under all possible operating conditions are therefore of paramount importance and often pose the ultimate limit to the accuracy of an electronic system.

The demand for accurate references in integrated circuits (ICs) has been addressed so far by analog cells exploiting the physical properties of integrated devices - like diodes, BJTs and MOS transistors operated under specific bias conditions - to obtain an output voltage and/or current which is constant and as independent as possible of process variations, of the power supply and of the operating temperature (PVT) [1-16].

Unfortunately, traditional integrated references [1-7], like basic bandgap cells, are not suitable to operate from a low supply voltage ($< 1.5\,\mathrm{V}$) and are therefore not compatible with present day aggressively scaled CMOS technologies [17]. Even though very-low-voltage references have been devised over the last years [8-16], the design of such circuits is often challenging because of the poor analog characteristics of nano-scale devices. In particular, their accuracy often relies on a tight control of process-related parameters and on stringent matching requirements, that can only be achieved by expensive post-fabrication trimming and/or by devices with drawn dimensions which are orders of magnitude larger than the lithographical minimum. As a consequence, the design of integrated references does not take any advantage from technology scaling and, on the contrary, is going to be a more and more serious concern and a limiting factor in the development of present and future integrated systems [17].

P.S. Crovetti is with the Dept. of Electronics and Telecommunications (DET) - Politectico di Torino, corso Duca degli Abruzzi, 24 - 10129 Torino, Italy, Phone: +39 011 0904220, e-mail: paolo.crovetti@polito.it – Copyright (c) 2014 IEEE. Personal use of this material is permitted. However, permission to use this material for any other purposes must be obtained from the IEEE by sending an email to pubs-permissions@ieee.org.

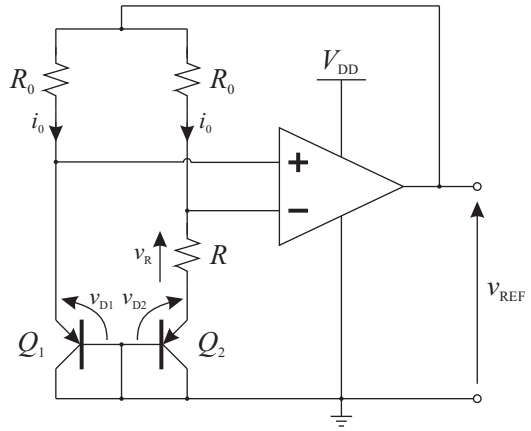

Fig. 1. Kuijk Bandgap Reference Circuit [2].

In this scenario, the possibility to re-think a reference circuit in digital terms, taking advantage of scaling to reduce costs and enhance performance, as done for other inherently analog cells in recent literature [18-20], sounds particularly attractive and poses a new research challenge [21].

In this paper, the implementation of a PVT-independent voltage reference in a mostly-digital integrated system is addressed by a novel *virtual reference* concept. In particular, it is suggested that a binary number, i.e. a *virtual reference*, can be employed in a digital system including an A/D converter (ADC) and a D/A converter (DAC) as a full replacement of a physical PVT-independent reference. Such a virtual reference can be evaluated algorithmically on the basis of non-PVT-invariant quantities acquired and converted into digital by the ADC against a possibly non-PVT-invariant physical pseudo-reference by translating the functions of an analog reference circuit into their digital equivalent.

The paper is organized as follows: in Section II, the operation of a traditional bandgap reference (BGR) is revised from a functional point of view, highlighting the functions that could be conveniently moved to the digital domain. In Section III, a digital circuit, functionally equivalent to the BGR considered in Section II, is then proposed and the virtual reference concept is introduced. This approach is generalized in Section IV and is exploited in Section V to design digital reference circuits whose performance is assessed by simulations. Then, a proof-of-concept, microcontroller-based prototype of a digital virtual reference is introduced in Section VI and its measured performance is reported. In Section VII, the proposed references are compared with state-of-the-art analog references and, finally, in Section VIII, some concluding remarks are drawn.

II. A Bandgap Reference from a Functional Perspective

The operation of a traditional analog BGR circuit is revised in this section from a functional point of view, so that to describe it in terms of elementary functions to be possibly implemented in a digital form. To this purpose, the well-known Kuijk circuit [2], whose schematic is reported in Fig.1, is considered to fix the ideas.

A. The Kuijk Bandgap Circuit

In the Kuijk circuit, a temperature independent reference voltage is obtained taking advantage of the opposite thermal drift of the forward voltage $v_{\rm D}$ of a silicon pn junction biased at a constant current density and of the difference $\Delta v_{\rm D} = v_{\rm D1} - v_{\rm D2}$ of the forward voltages $v_{\rm D1}$ and $v_{\rm D2}$ of two pn junctions biased at current densities J_1 and J_2 in a fixed ratio $\frac{J_1}{J_2} = h^\star$. From solid-state physics, in fact, $v_{\rm D}$ decreases with the absolute temperature T whereas $\Delta v_{\rm D}$ can be expressed as

$$\Delta v_{\rm D} = \frac{\kappa T}{q} \log h^\star, \tag{1}$$

being κ the Boltzmann's contstant and q the electron charge, and is therefore proportional to the absolute temperature T (PTAT). Moreover, a constant χ exists for which

$$v_{\rm REF} = v_{\rm D} + \chi \Delta v_{\rm D} \tag{2}$$

is non-zero and first-order temperature independent, i.e. for which $\frac{\partial v_{\rm REF}}{\partial T}\big|_{T=T_{\rm nom}} = 0$ where $T_{\rm nom}$ is the nominal operating temperature. Since it can be demonstrated [4] that temperature compensation is achieved for $v_{\rm REF}$ close to the bandgap voltage of silicon (1.1 V-1.2 V), circuits based on this mechanism - like Kuijk's - are known as *bandgap references*.

The principle outlined so far is implemented in the Kuijk circuit exploiting the emitter-base junctions of two diode-connected pnp BJTs Q_1 and Q_2 with emitter areas S_1 and S_2 in a $1 : h^\star$ ratio and biased at the same emitter current i_0. Being bandgap compensation (2) intrinsically related to the physical properties of silicon pn junctions, Q_1 and Q_2 can be regarded as the core *physical standard* of the circuit, providing the *voltage primitives* $v_{\rm D} = v_{\rm D1}$ and $\Delta v_{\rm D} = v_{\rm D1} - v_{\rm D2}$ appearing in (2). The bias current i_0 for the BJTs is obtained from the output of an operational amplifier (opamp) via two matched resistors R_0, the voltage across which is kept equal by negative feedback. It is worth noting that, neglecting the finite power supply rejection of the opamp, the BJTs bias current

$$i_0 = \frac{v_{\rm REF} - v_{\rm D1}}{R_0}, \tag{3}$$

where $v_{\rm REF}$ is the PVT-invariant output voltage of the circuit, is not explicitly related to the power supply. From a functional perspective, the resistors R_0 and the opamp can be therefore regarded as a power supply-independent *bias* network for the physical standard.

Moreover, the same opamp in the circuit of Fig.1, with its negative (R_0, R and Q_2) and positive (R_0, Q_1) feedback networks, is exploited for analog *signal processing* to get the temperature-compensated output voltage $v_{\rm REF}$ starting from the voltage primitives by implementing the *weighted sum* (2) in the voltage domain. Since $v_{\rm R} = \Delta v_{\rm D} = v_{\rm D1} - v_{\rm D2}$, in fact, assuming that the opamp is ideal, $v_{\rm REF}$ can be expressed as

$$v_{\rm REF} = v_{\rm D1} + \frac{R_0}{R}\Delta v_{\rm D} \tag{4}$$

which is analogous to (2) provided that $\frac{R_0}{R} = \chi$.

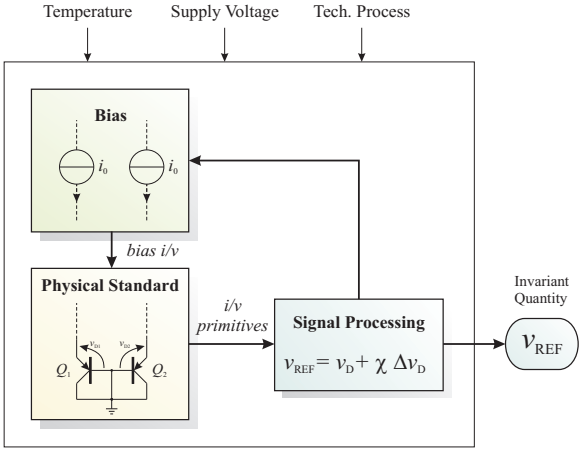

Fig. 2. Functional Blocks of a Reference Circuit.

B. Kuijk's Bandgap Functional Block Diagram

The operation of the Kuijk circuit can be therefore described in terms of the three main functional units depicted in Fig.2: a *physical standard* (Q_1 and Q_2), whose properties are exploited to get the *voltage primitives* ($v_{\rm D}$ and $\Delta v_{\rm D}$) required for bandgap compensation, a *bias* network, that provides the *bias currents* to the physical standard, and a *signal processing* element, which combines the primitives to get the actual PVT-invariant reference and drives the bias network independently of the external power supply. These functional units can be found in almost all integrated references so that the block diagram in Fig.2 is quite general. Maintaining that the same physical standard of the Kuijk BGR is exploited, the possibility and the opportunity to move its *bias* and *signal processing* functions to the digital domain will be discussed in what follows to address the challenges of present day integrated systems.

III. A Digital-Based Virtual Bandgap Reference

A digital-based voltage reference, functionally equivalent to a Kuijk BGR, is now proposed mapping the *bias* and *signal processing* functions highlighted in the previous Section on the hardware platform of a mainly digital System on Chip (SoC). To this purpose, after a generic SoC hardware architecture is defined, a software procedure implementing bandgap compensation is proposed and the *virtual reference* concept is introduced. Then, this concept is exploited to generate a supply-independent bias for the physical standard, in full analogy with the traditional Kuijk circuit. Finally, the execution time and the resources required by the proposed PVT-compensation software procedure are discussed.

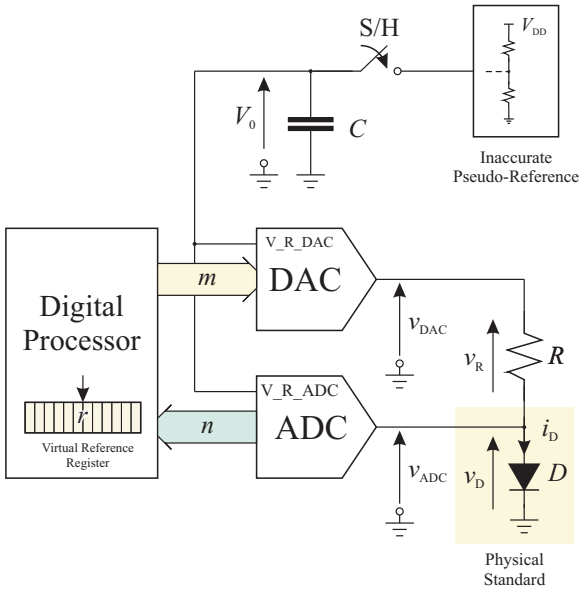

Fig. 3. System-on-Chip Hardware Platform considered for the implementation of a Digital-Based Virtual Voltage Reference.

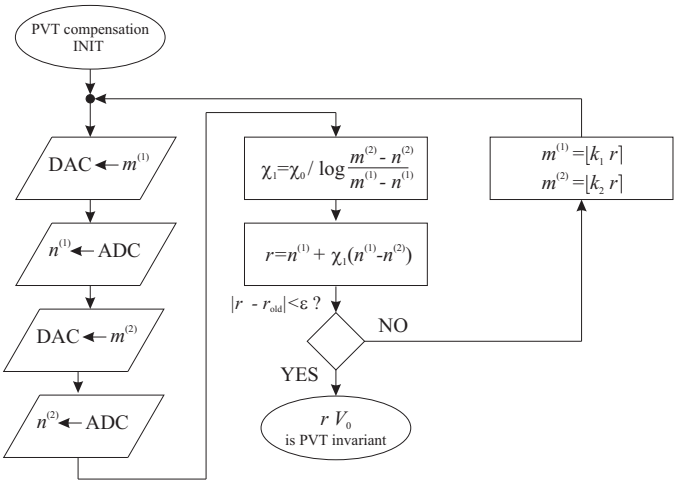

Fig. 4. Flow chart of the software procedure intended to evaluate the PVT-independent virtual reference.

A. Hardware Architecture

A digital implementation of the Kuijk bandgap circuit is proposed in the following considering the hardware platform of a mostly digital SoC in Fig.3, which includes a digital processor, an ADC and a DAC.

Here, for a given input voltage $0 < v_{\rm ADC} < V_0$, the ADC makes available to the processor, after a time[1] $T_{\rm A/D}$, an integer n represented on N bits so that

$$v_{\rm ADC} = \frac{n}{2^N} V_0 + v_\varepsilon \tag{5}$$

where V_0 is a possibly non-PVT independent pseudo-reference voltage, that is only required to be *constant* within one least significant bit (LSB) for a conveniently long time, as it will be better clarified in what follows. In practice, a pseudo-reference V_0 with the required characteristics can be obtained sampling a (partition of a) non-stabilized power supply voltage as in Fig.3 by an integrated, low leakage, elementary sample and hold (S/H), which can be designed to maintain the *hold* voltage constant with a high accuracy and for a long time (tens or hundreds of seconds), as in [24]. The error term v_ε in (5), which takes into account of all ADC non-idealities, is assumed to be dominated by quantization so that $|v_\varepsilon| < \frac{V_0}{2^{N+1}} = \frac{1}{2}$LSB.

The DAC in Fig.3 converts an integer m represented on N bits from the processor into a constant output voltage

$$v_{\rm DAC} = \frac{m}{2^N} V_0 + v_\varepsilon \tag{6}$$

after a settling time $T_{\rm D/A}$, where V_0 is the same pseudo-reference of the ADC[2] and it is assumed that the error term v_ε, describing all DAC non-idealities, is less than $\pm\frac{1}{2}$LSB. The error terms v_ε in (5) and (6) will be neglected in the following of this Section while their impact will be considered in simulations and experiments in Sections V and VI.

The ADC and the DAC circuits in Fig.3 are supposed to be needed and mostly used for the main SoC application (e.g. biomedical, control, multimedia,...) and designed on the basis of its functional requirements. Their resolution, in particular, which is related to the SoC specifications, can be regarded as the ultimate accuracy goal for the proposed reference. Moreover, no specific ADC/DAC architecture is assumed, even though mostly digital, low-voltage, low-power, oversampling ADCs and DACs, achieving a high resolution with a reduced silicon area occupancy, like those proposed in [18], [22], [23] and others currently being developed, can be preferred to take full advantage of the proposed approach.

The platform in Fig.3 is completed by a diode D connected to the DAC output through a resistor R and in parallel to the ADC input port. The diode D is used as the physical standard of a virtual Kuijk BGR, whose main functions are implemented in software, as described in what follows.

B. Bandgap Compensation Procedure

With reference to the architecture in Fig.3, a digital BGR implementing in software, by the procedure outlined in Fig.4, the *bias* and the *signal processing* functions of a Kuijk circuit, is now proposed. Following this procedure, two integers $m^{(1)} = \lfloor k_1\, r_0 \rceil$ and $m^{(2)} = \lfloor k_2\, r_0 \rceil$, where $\lfloor\cdot\rceil$ is the rounding operator, r_0 is a convenient initial guess value[3] and k_1 and k_2 are two constant rational scaling factors defining two bias points, are first converted into analog by the DAC, so that to apply two different voltages

$$v_{\rm DAC}^{(i)} = \frac{m^{(i)}}{2^N} V_0, \qquad i \in \{1, 2\} \tag{7}$$

to the R-D branch in Fig.3 and hence to bias the diode D at two different current densities, as in the definition of the voltage primitives $v_{\rm D}$ and $\Delta v_{\rm D}$ appearing in (2). The diode

[1]The ADC conversion time and all other delays in the acquisition chain are included in $T_{\rm A/D}$ for the sake of simplicity.

[2]The requirement that the ADC and the DAC share the same pseudo-reference voltage V_0 can be released by converting into digital the output voltage of the DAC using the same ADC.

[3]The value of r_0 should be chosen close to the nominal value of what will be defined as the *virtual reference* in what follows.

forward voltages $v_{\rm D}^{(1)}$ and $v_{\rm D}^{(2)}$, corresponding to the two bias conditions, are acquired by the ADC in Fig.3 and can be therefore expressed in terms of the pseudo-reference V_0 as

$$v_{\rm D}^{(i)} = \frac{n^{(i)}}{2^N} V_0, \qquad i \in \{1,2\} \tag{8}$$

where the integers $n^{(1)}$ and $n^{(2)}$ are the results of the A/D conversions. Moreover, the corresponding forward currents $i_{\rm D}^{(1)}$ and $i_{\rm D}^{(2)}$ flowing through the diode can be expressed as

$$i_{\rm D}^{(i)} = \frac{v_{\rm DAC}^{(i)} - v_{\rm D}^{(i)}}{R} = \left(m^{(i)} - n^{(i)}\right) \frac{V_0}{2^N R},\ i \in \{1,2\}\,. \tag{9}$$

On the basis of (9), it can be observed that the ratio h of the diode current densities under the two above bias conditions is not intrinsically fixed. Nonetheless, it can be expressed as

$$h = \frac{J_1}{J_2} = \frac{i_{\rm D}^{(1)}}{i_{\rm D}^{(2)}} = \frac{v_{\rm DAC}^{(1)} - v_{\rm D}^{(1)}}{v_{\rm DAC}^{(2)} - v_{\rm D}^{(2)}} = \frac{m^{(1)} - n^{(1)}}{m^{(2)} - n^{(2)}} \tag{10}$$

and can be numerically evaluated from the acquired values $n^{(1)}$ and $n^{(2)}$ independently of the pseudo-reference V_0 and of the resistance R. As a consequence, taking into account of (1), the voltage primitive $\Delta v_{\rm D}$ in (2), which is defined with reference to pn junctions biased at a *fixed* current density ratio $h^\star$, can be expressed in terms of h, $v_{\rm D}^{(1)}$ and $v_{\rm D}^{(2)}$ as

$$\Delta v_{\rm D} = \frac{\log h^\star}{\log h} \left(v_{\rm D}^{(1)} - v_{\rm D}^{(2)}\right) \tag{11}$$

where the factor $\frac{\log h^\star}{\log h}$ can be numerically evaluated. It is worth noting that neither (10) nor (11) rely on assumptions on device matching.

Considering $v_{\rm D} = v_{\rm D}^{(1)}$ and the expression of $\Delta v_{\rm D}$ in (11), neglecting quantization errors, Eqn.(2) can be written as

$$\begin{aligned} v_{\rm REF} &= v_{\rm D}^{(1)} + \chi \frac{\log h^\star}{\log h} \left(v_{\rm D}^{(1)} - v_{\rm D}^{(2)}\right) \\ &= \frac{V_0}{2^N} \left[n^{(1)} + \frac{\chi_0}{\log h} \left(n^{(1)} - n^{(2)}\right)\right] = \frac{V_0}{2^N} r \end{aligned} \tag{12}$$

where (12), that defines the quantity r, is obtained replacing $v_{\rm D}^{(1)}$ and $v_{\rm D}^{(2)}$ with their expressions in (8) and including the constant terms in the factor $\chi_0 = \chi \log h^\star$. Since the l.h.s. of Eqn.(12) is first-order temperature independent, it follows that, under the above approximations, also the r.h.s. expression is first-order temperature independent regardless of the pseudo-reference V_0 and PVT-related variations of V_0 are necessarily countered by opposite variations of r. Thanks to this property, the quantity r, which can be numerically evaluated in terms of acquired data (Fig.4, second column), conveys all the information needed to set a temperature independent reference in terms of V_0 and can be therefore regarded as a *virtual reference* as discussed in what follows.

C. A Virtual Voltage Reference

On the basis of (12), any external input voltage $v_{\rm ADC}$ converted by the ADC in Fig.3 into the integer k with respect to its pseudo-reference V_0, i.e. so that

$$v_{\rm ADC} = \frac{k}{2^N} V_0 \tag{13}$$

can be expressed in terms of the temperature-independent reference $v_{\rm REF}$, by replacing the expression of $\frac{V_0}{2^N}$ from (12) into (13), as

$$v_{\rm ADC} = \frac{k}{r} v_{\rm REF} = \frac{\frac{2^N k}{r}}{2^N} v_{\rm REF} \tag{14}$$

where, comparing (13) and (14), the quantity $k_0 = \frac{2^N k}{r}$ is formally equivalent to the result of the conversion of $v_{\rm ADC}$ into digital performed by the same ADC in Fig.3, now referenced to the temperature-independent voltage $v_{\rm REF}$. In other words, neglecting quantization errors, k_0 is the same value that would be obtained converting $v_{\rm ADC}$ into digital by the ADC in Fig.3, where a temperature-compensated voltage $v_{\rm REF}$, e.g. the output of the Kuijk circuit, is used as a physical reference. Similarly, replacing (12) into (6), the output of the DAC in Fig.3, physically connected to the pseudo-reference V_0, can be expressed in terms of the temperature-compensated reference $v_{\rm REF}$ and of r as

$$v_{\rm DAC} = \frac{m}{r} v_{\rm REF} = \frac{m}{2^N} \left(\frac{2^N}{r} v_{\rm REF}\right). \tag{15}$$

Considering (14) and (15), the number r, evaluated as in Eqn.(12), can be regarded as a *virtual voltage reference* which can effectively replace an actual temperature-independent reference voltage for A/D and D/A conversion. Moreover, based on (15), a physical reference voltage (proportional to) $v_{\rm REF}$ can be obtained - only if and when it is really necessary - as the output of the DAC in Fig.3, by converting into analog (a value m proportional to) the virtual reference r.

D. Supply-Independent Bias

The possibility to obtain a physical voltage proportional to $v_{\rm REF}$ by D/A conversion, as discussed above, is exploited in the software procedure of Fig.4 to remove the residual dependence on V_0 of the diode bias currents $i_{\rm D}^{(1)}$ and $i_{\rm D}^{(2)}$, which can be observed in Eqn.(9). To this purpose, in analogy with Eqn.(3) and considering (12), the temperature compensation procedure described so far is iterated using $m^{(i)} = \lfloor k_i\, r \rceil$, with $i \in \{1,2\}$ (Fig.4, third column), where r is the virtual reference obtained at the previous step and k_i are the constant scaling factors introduced in Section IIIb to get convenient bias voltages $v_{\rm DAC}^{(i)}$. By so doing, Eqn.(9) can be rewritten as

$$i_{\rm D}^{(i)} = \frac{\lfloor k_i\, r \rceil \frac{V_0}{2^N} - v_{\rm D1}^{(i)}}{R} \simeq \frac{k_i\, v_{\rm REF} - v_{\rm D1}^{(i)}}{R},\ i \in \{1,2\}\,, \tag{16}$$

where the rounding error in the last passage is less than $\frac{1}{2}$ LSB and $i_{\rm D}^{(i)}$, $i \in \{1,2\}$ are now independent of V_0, in full analogy with Eqn.(3). Such a procedure can be repeated until the values of the virtual reference r in two next iterations are equal within a tolerance ε (Fig.4, decision block in the second column). In practice, two or three steps are sufficient to get a fixed value $r^\star$, which can be regarded as a PVT-independent virtual reference and that could be also converted into analog and sampled as a replacement of the pseudo-reference V_0. By the same approach, different PVT-independent voltages, possibly needed in digital-assisted analog cells, can be also obtained converting into analog values proportional to $r^\star$ and sampling the resulting voltages by S/H circuits.

E. Execution and Refresh Time

The execution time of the PVT compensation procedure described so far can be roughly estimated as

$$T_{\mathrm{PVT}} = p \cdot T_{\mathrm{D/A}} + q \cdot T_{\mathrm{A/D}} + T_{\mathrm{proc}}, \tag{17}$$

where p and q are, respectively, the required D/A and A/D conversions ($p = q = 2$ in Fig.4) and T_{proc} is the time needed for digital processing. In practice, T_{PVT} is dominated by the time required for the q A/D conversions and ranges from hundreds of nanoseconds up to tens of milliseconds, depending on the ADC architecture and on the target resolution [25].

The execution time T_{PVT} should be sufficiently small so that PVT-related variations of the voltage primitives during T_{PVT} are less than 1 LSB. In particular, T_{PVT} should be small in comparison with thermal time constants or, in alternative, transient temperature variations during T_{PVT} should be accounted for in the compensation procedure. Supply variations during T_{PVT} are a minor concern since, considering (16), their impact on the virtual reference is only related to the power supply rejection of the DAC and of the ADC. Moreover, high frequency power supply fluctuations are also attenuated by decoupling capacitors on the (analog) power supply of a SoC.

After T_{PVT}, the ADC and DAC resources can be allocated, by multiplexing, to other SoC functions. Nonetheless, since the virtual reference $r^\star$ is valid as far as V_0 is constant within one LSB, the procedure in Fig.4 needs to be scheduled every

$$T_{\mathrm{REFR}} = \frac{CV_0}{I_{\mathrm{leak}} 2^N} \tag{18}$$

being C the capacitance of the hold capacitor in Fig.3 and I_{leak} the average leakage current flowing through it. For a low-leakage S/H [24], the refresh time T_{REFR} can be as long as tens of seconds for $N = 14$ and $C = 2.5\mathrm{pF}$.

Based on (17) and (18), the activity factor

$$\delta = \frac{T_{\mathrm{PVT}}}{T_{\mathrm{REFR}}}, \tag{19}$$

that is an estimate of the percentage of SoC resources utilized by a virtual reference, can be defined. Considering the practical values of T_{PVT} and T_{REFR} discussed above, an activity factor δ ranging from 10^{-8} to 10^{-3} can be achieved, so that a virtual reference can be in included in a mostly digital SoC with a minimum impact on its processing performance.

IV. A Generalized Digital Virtual Reference

The virtual voltage reference concept, illustrated so far with reference to the Kuijk circuit, can be extended to other analog references, possibly based on different physical standards suitable to very-low-voltage operation, and can be also further generalized taking advantage of the computational power and of the versatility of digital processing.

It can be observed, in fact, that the *signal processing* function in Fig.2, which is the weak point of all analog references - its accuracy being impaired by technology spreads, mismatch and poor analog characteristics of active devices - can be the point of strength of a digital reference, in which virtually any mathematical function of the acquired primitives can be *exactly* numerically evaluated with a 16-bit, 32-bit or higher working precision by a digital core, whose performance is boosted and whose cost and power consumption decrease with technology scaling [17].

The implementation of complex signal processing functions, intended to improve the accuracy and the stability of a voltage or current reference under PVT variations, which are unfeasible or at least impractical in the analog domain, can be therefore an option for a digital reference, opening new design perspectives. For instance, an algorithmic approach can be adopted to achieve high-order temperature compensation [26], to reduce the effects of technology process variability, acquiring and combining data from different physical standards following the idea proposed in [27] to improve the accuracy of integrated resistors, and even to achieve a high immunity to electromagnetic interference (EMI) by implementing the technique proposed in [28] in the PVT compensation procedure.

Considering the above discussion, the PVT-invariant voltage in (2) can be conveniently generalized to a generic *invariant function* f of (possibly PVT dependent) voltage primitives $\mathbf{v} = (v_1, v_2, \ldots, v_N)$ obtained from one or more physical standards (diodes, BJTs, MOS transistors, integrated resistors of different types,...) operated under different bias conditions, devised so that f is constant-valued, within a prescribed tolerance ε, for PVT variations in a specified range. i.e. a continuous function f for which $\frac{\partial f}{\partial v_i} \neq 0$ for $1 \leq i \leq N$ and

$$|f(\mathbf{v}) - f_{\mathrm{c}}| < \varepsilon \quad \forall\, \mathbf{v} \in V, \tag{20}$$

where $f_{\mathrm{c}} = f(\mathbf{v}_{\mathrm{n}})$ is the value of f corresponding to the voltage primitives $\mathbf{v}_{\mathrm{n}}$ under nominal PVT conditions and the set V includes all the values that can be assumed by such primitives under their specified PVT variability intervals. Considering that f, expressed in (20) as a function of voltages (dimensioned quantities) can be equivalently stated in terms of their dimensionless *values* measured with respect to a fixed unit[4] V_{u} and assuming $\varepsilon = 0$, Eqn.(20) can be re-written as

$$f\left(\frac{\mathbf{v}}{V_{\mathrm{u}}}\right) - f_{\mathrm{c}} = 0 \quad \forall\, \mathbf{v} \in V. \tag{21}$$

Provided that the values of the voltage primitives are acquired and converted into digital by an ADC on the basis of a possibly non-PVT invariant pseudo-reference voltage V_0 as in Fig.3, neglecting quantization errors, Eqn.(21) can be expressed in terms of the vector $\mathbf{n} = (n_1, n_2, \ldots, n_N)$ of the acquired samples as

$$f\left(\frac{V_0}{2^N V_{\mathrm{u}}}\mathbf{n}\right) - f_{\mathrm{c}} = f(\alpha \mathbf{n}) - f_{\mathrm{c}} = 0. \tag{22}$$

For a given vector $\mathbf{n} = \mathbf{n}^\star$ of acquired values, (22) can be therefore regarded as a (generally nonlinear) equation in the scalar quantity α proportional to the unknown pseudo-reference voltage V_0. Assuming that a unique solution $\alpha^\star$ of (22) exists, it follows that

$$\alpha^\star = \frac{V_0}{2^N V_{\mathrm{u}}} \rightarrow V_{\mathrm{u}} = \frac{V_0}{2^N}\frac{1}{\alpha^\star}. \tag{23}$$

Being (23) formally equivalent to (12), the quantity $r = \frac{1}{\alpha^\star}$ can be regarded as a generalized virtual voltage reference for A/D and D/A conversion, as discussed in the previous Section.

[4] A natural choice could be to fix $V_{\mathrm{u}} = 1\,\mathrm{V}$

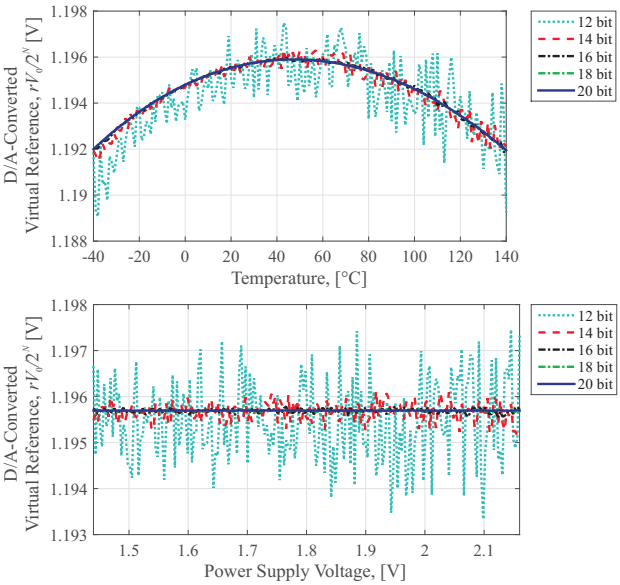

Fig. 5. Virtual Kuijk Bandgap (VKB) circuit: D/A-Converted Virtual Reference vs. Temperature (top) and D/A-Converted Virtual Reference vs. Power Supply (bottom).

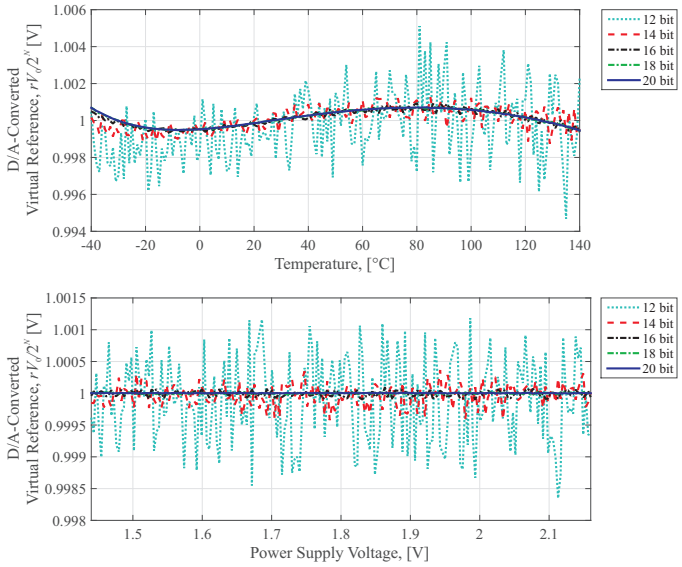

Fig. 6. Generalized Virtual Reference (GVR) circuit: D/A-Converted Virtual Reference vs. Temperature (top) and D/A-Converted Virtual Reference vs. Power Supply (bottom).

V. Design and Simulations

The design of two PVT-independent digital voltage references, based on the technique proposed in the previous Sections, is now addressed and their stability under PVT variations is tested by computer simulations. In particular, the impact of quantization error, neglected so far in derivations, is highlighted and discussed in what follows.

A. Virtual Reference Circuit Design

The virtual reference concept introduced in this paper has been exploited to design a Virtual Kuijk Bandgap (VKB), first-order temperature independent voltage reference, which mimics the operation of the Kuijk BGR as described in Section III, and a generalized virtual reference (GVR) achieving second-order temperature compensation by the approach discussed in Section IV. Both the proposed virtual references have been designed in a 1.8V, 180nm CMOS technology and are based on the same hardware platform of Fig.3, the difference among them being only in the PVT-compensation software procedure.

In particular, both the references include a $10\mu\text{m} \times 10\mu\text{m}$, $p+$ over n-well diode D as a physical standard, which is biased as in Fig.3 by a high-resistivity poly resistor $R = 23\text{k}\Omega$, with drawn dimensions $L = 60\mu\text{m}$ and $W = 4\mu\text{m}$, connected to the output of the DAC. Both the diode and the resistor are described in simulations by experimentally validated DC models from the silicon foundry, which accurately reproduce their characteristics over temperature and process spreads.

With reference to the above physical standard, the diode D forward voltages $v_{\text{D}}^{(1)}$ and $v_{\text{D}}^{(2)}$, corresponding to $v_{\text{DAC}}^{(1)} \simeq 900\text{mV}$ and $v_{\text{DAC}}^{(2)} \simeq 700\text{mV}$ and to nominal bias currents at ambient temperature of about $10\mu\text{A}$ and $2\mu\text{A}$, respectively, are considered as voltage primitives for both the VKB and GVR circuits.

Both the proposed references are suitable to operate from a power supply as low as[5] $v_{\text{DAC}}^{(1)} = 900\text{mV}$. Moreover, assuming that a 2.5pF hold capacitor is used in the S/H, the extra silicon area required by the references, in a SoC including a digital core, an ADC and a DAC, is of only $600\mu\text{m}^2$.

The ADC, the DAC and the digital core in Fig.3 are described in behavioral terms for simulation purposes, considering a pseudo-reference voltage V_0 equal to the $1.8\,\text{V} \pm 20\%$ power supply and introducing N-bit uniform quantization in the values of the electrical quantities acquired from/applied to the physical standard. Moreover, the ADC in [22] and the DAC in [23], both integrated in a 180nm CMOS technology, will be considered as possible implementations for benchmarking in Section VII. All ADC and DAC error sources including noise, nonlinearity and finite power supply rejection, are assumed to be negligible with respect to quantization errors and are not considered. The number of bits N of the ADC and of the DAC are assumed to be equal and equal to the working precision of the digital core.

The procedure in Fig.4 has been finally followed to obtain the virtual reference: for the VKB circuit, in particular, the virtual reference is evaluated by Eqn.(12), where a factor $\chi_0 = 20.1$ has been chosen to achieve first-order temperature compensation. For the GVR reference, instead, the expression

$$f(v_{\text{D}}^{(1)}, \Delta v_{\text{D}}) = v_{\text{D}}^{(1)} + a \cdot \Delta v_{\text{D}} + \text{e}^{b + c \cdot v_{\text{D}}^{(1)} + d \cdot \Delta v_{\text{D}}}, \qquad (24)$$

where Δv_{D} is defined as in (11) and $a = 20.46\,\text{V}^{-1}$, $b = -19.56$, $c = 18.75\,\text{V}^{-1}$, $d = 1\,\text{V}^{-1}$, has been chosen for the function $f(\cdot)$ appearing in (22), to achieve second-order temperature compensation.

B. Computer Simulations

The VKB and GVR references have been simulated in Matlab to test their stability under PVT variations, highlighting

[5]Unless more stringent limitations arise from the ADC and/or the DAC.

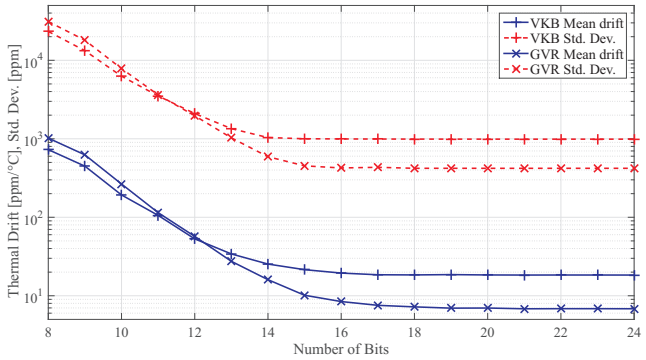

Fig. 7. Mean temperature coefficient (box method) and standard deviation of the D/A-converted virtual reference for the VKB and GVR circuits in the $-40°\mathrm{C}$ - $140°\mathrm{C}$ temperature range versus number of bits.

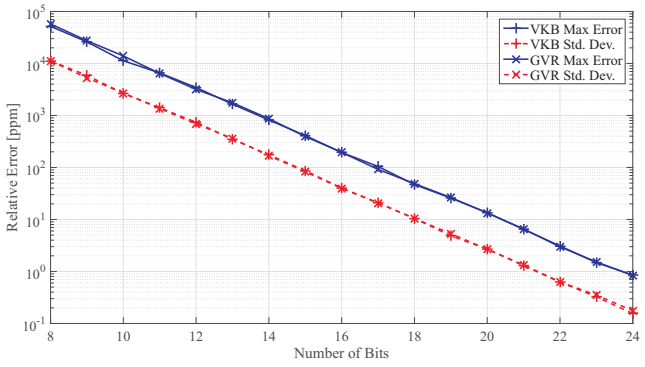

Fig. 8. Maximum relative error $\frac{x_{\max}-x_{\min}}{x_{\mathrm{nom}}}$ and Standard Deviation of the D/A converted virtual reference for the VKB and GVR circuits for variations of the power supply voltage in the 1.4V-2.2V range vs. number of bits.

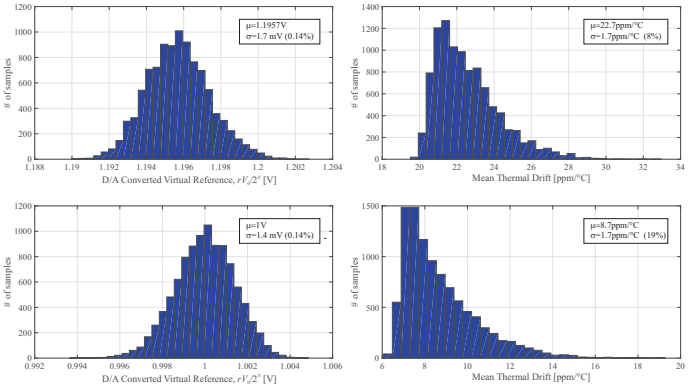

Fig. 9. Statistical distribution of the nominal reference voltage at ambient temperature (left plots) and of the mean thermal drift (right plots) obtained from 10,000 Montecarlo simulations for a 14-bit VKB (top plots) and for a 16-bit GVR (bottom plots) over process variations.

the effects of quantization error. To this purpose, the reference voltage obtained by the proposed circuits converting into analog the virtual reference r with respect to the pseudo-reference V_0, as discussed in Section IIIc, has been simulated versus temperature in the range $-40°\mathrm{C}$ - $+140°\mathrm{C}$, for a nominal 1.8V power supply, and then considering variations from -20% to +20% of the power supply voltage (and hence of the pseudo-reference), at ambient temperature ($T = 27°\mathrm{C}$). The results of these simulations are reported in Fig.5 and in Fig.6 for the VKB and the GVR references for different values of the ADC/DAC resolution. Moreover, the mean thermal drift (box method) and the standard deviation (SD) of the reference voltage in the range $-40°\mathrm{C}$ - $+140°\mathrm{C}$ are reported in Fig.7 versus the number of bits of the ADC/DAC converters. Similarly, the maximum value and the SD of the relative error for supply variations from -20% to $+20\%$ are reported versus the number of bits in Fig.8. The untrimmed characteristics of the references over process spreads have been finally tested by Monte Carlo simulations whose results are reported in Fig.9. Simulation results are discussed in what follows.

1) Thermal Drift: from Fig.5, it can be observed that the VKB provides a reference voltage of $1.196\,\mathrm{V}$ with a mean thermal drift of about $19\,\mathrm{ppm}/°\mathrm{C}$, for a resolution of 16 bits or more, which is similar to that achieved by an analog Kuijk bandgap. For a 14-bit (12-bit) resolution, the thermal drift increases to about $22\,\mathrm{ppm}/°\mathrm{C}$ ($35\,\mathrm{ppm}/°\mathrm{C}$) and is dominated by quantization. In these last cases, the reference voltage vs. temperature curve is not smooth because of transitions of quantized primitives from one discrete value to another.

From Fig.6, the GVR circuit provides a reference voltage of $1\,\mathrm{V}$, corresponding to the value of V_{u} considered in (22), and a reduced thermal drift of $7\,\mathrm{ppm}/°\mathrm{C}$ is achieved thanks to exponential curvature compensation. Such an improvement, however, can be appreciated in practice only if the ADC/DAC resolution is increased above 14 bits. Since both the VKB and the GVR are based on the same physical standard under the same bias conditions, this result highlights the enhancement that can be obtained in a digital reference taking advantage of digital signal processing, as discussed in Section IV.

2) Power Supply Rejection: from the bottom plots in Fig.5 and in Fig.6, it can be observed that the proposed VKB and GVR digital references are independent of the power supply voltage, from which the ADC/DAC pseudo-reference is derived, with fluctuations that are only related to quantization.

3) Quantization: from Fig.7, it can be observed that the SD of the reference voltage variations over temperature is reduced by a factor two for each additional bit up to about 14 bits for the VKB and up to 16 bits for the GVR. Above, the accuracy over temperature is limited by the residual error in thermal compensation rather than by quantization. Moreover, from Fig.8, the SD of the fluctuations in the reference voltage is about $700\,\mathrm{ppm}$ for a $12\,\mathrm{bit}$ ADC/DAC resolution both for VKB and GVR references, i.e. about $3\,\mathrm{LSBs}$, and decrease by a factor two for each additional bit. Comparing Fig.8 with Fig.7, it can be noticed that when quantization is dominant, the SD of the reference voltage variations over temperature and supply are comparable. The effects of quantization could be mitigated by the dithering effect of thermal noise [29] and by convenient digital filtering, that will be considered in future work to achieve an accuracy close to $1\,\mathrm{LSB}$.

4) Technology Spreads: The operation of the proposed references in the presence of technology spreads has been simulated by Monte Carlo analyses (10,000 runs) considering the statistical variability of the process parameters of the diode D and of the resistor R in Fig.3. The statistical distributions of the untrimmed reference voltages and of the untrimmed thermal drift for the VKB, simulated with a 14-bit resolution, and

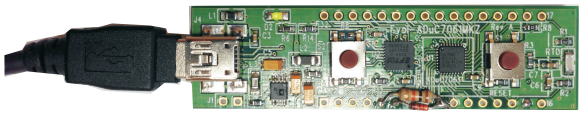

Fig. 10. Photograph of the Proof-of-Concept Prototype.

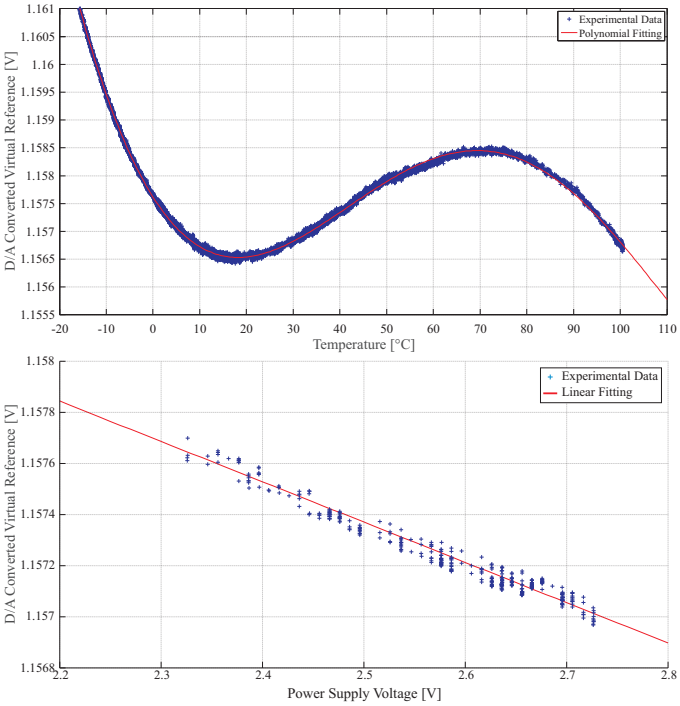

Fig. 11. Measured D/A-Converted Virtual Reference versus Temperature (top) and versus Power Supply Voltage (bottom) for the proof-of-concept prototype.

for the GVR, simulated with a 16-bit resolution, are reported in Fig.9. In the plots on the left of the figure, it can be observed that the simulated SD of the untrimmed reference voltage at ambient temperature over process variations is of only 1.7mV for the VKB and 1.4mV for the GVR, corresponding in both cases to about 0.14%. Moreover, from the plots on the right, the mean value of the untrimmed thermal drift is 22.7 ppm/°C (with a SD of 1.7 ppm/°C) for the VKB and of 8.7 ppm/°C (with a SD of 1.7 ppm/°C) for the GVR. Such variations can be fully compensated by software calibration.

VI. Experimental Results

A microcontroller-based proof-of-concept prototype of a virtual voltage reference implementing the technique proposed so far is considered in this Section for validation and its performance is experimentally verified.

A. Proof-of-Concept Prototype

A proof-of-concept virtual reference prototype based on the MiniKit Evaluation Board of the ADuC7061 microcontroller unit (MCU) by Analog Devices [30] has been developed to verify the operation and the effectiveness of the technique introduced in this paper. The ADuC7061 MCU in the prototype is based on a 32-bit ARM7TDMI© RISC core operated at a clock frequency of 10MHz and includes,

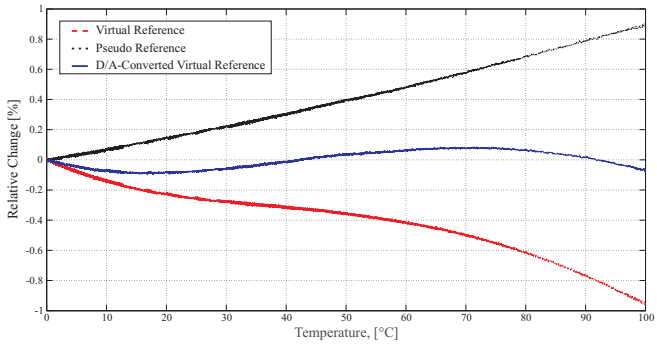

Fig. 12. Measured Relative Variations $\frac{x(T)-x(T=0)}{x(T=0)} \cdot 100$ of the pseudo-reference V_0, of the virtual reference r and of the D/A-converted virtual reference $r\frac{V_0}{2^N}$ during the test over temperature of Fig.11, top plot.

among its peripherals, a 24-bit Sigma-Delta ADC, a 16-bit DAC (14 bit ENOB), an accurate analog reference and a temperature sensor. The ADC and the DAC, which have been used to map the corresponding blocks of the digital reference architecture in Fig.3, have been configured via software for a resolution of 16 bit and to use an on-chip partition $\frac{V_{\rm DD}}{2}$ of the $V_{\rm DD} = 2.5{\rm V} \pm 5\%$ power supply as a physical pseudo-reference. It is worth noting that, unlike in Fig.3, the pseudo-reference is not sampled-and-held in this prototype, since an integrated S/H was not available. A discrete 1N4148 diode, biased via a $10{\rm k}\Omega$ resistor, has been connected to the MiniKit board to implement the physical standard in Fig.3. A photograph of the prototype is reported in Fig.10.

With reference to the hardware prototype described so far, a software procedure implementing a digital VKB reference according with the flow chart in Fig.4 has been written in ANSI C. Such a procedure requires less than 1kB of extra program memory and is executed in a time $T_{\rm PVT} = 4\,{\rm ms}$, that is approximatively the time needed for the A/D conversions[6]. At the end of the procedure, which is called in an infinite loop, the virtual reference is converted into analog by the DAC and the corresponding pin voltage, which is PVT-independent according with the theory in Section III and can be regarded as the physical output of the prototype, has been measured over temperature and supply variations. Measured results are reported and commented in what follows.

B. Test Results

The digital virtual reference prototype described so far has been tested in a temperature range from $-10°{\rm C}$ to $+100°{\rm C}$ and varying the power supply voltage from 2.3V to 2.7V. The corresponding reference voltage is reported in Fig.11 versus temperature (top plot) and versus the power supply voltage, at ambient temperature $25°{\rm C}$ (bottom plot). From the top plot, it can be observed that the proposed reference shows a nominal value of $1.157\,{\rm V}$ with a residual thermal drift of about $16{\rm ppm}^\circ/{\rm C}$, which is comparable with the performance of the precision reference embedded in the ADuC7061 IC [30].

[6]For $T_{\rm REFR} = 10{\rm s}$, this corresponds to an activity factor $\delta = 4 \cdot 10^{-4}$. Since the S/H is not included in the prototype and the compensation procedure runs continuously, the activity factor δ has not been experimentally tested.

TABLE I
VOLTAGE REFERENCE CIRCUITS PERFORMANCE COMPARISON

Reference		[2]	[6]	[9]	[10]	[11]	[12]	This work		
Year		1973	2012	2007	2013	2014	2007	2015		
Author		Kuijk	Andreou	De Vita	Osaki	Ma	Crovetti	VKB	GVR	VKB Prot.
Technology	μm	$0.18^{\sharp}$	0.35	0.35	0.l8	0.18	0.35	0.18	0.18	PCB
Type		Analog	Analog	Analog	Analog	Analog	Analog	Digital	Digital	Digital
Characterization		Meas.	Meas.	Meas.	Meas.	Meas.	Meas.	Sim.	Sim.	Meas.
Reference Voltage	V	1.210	0.6177	0.67	1.09	0.767	0.047	1.196	1.000	1.157
ADC/DAC Resolution	bit	N/A	N/A	N/A	N/A	N/A	N/A	14	16	16
Untrimmed Accuracy Std. Dev.	mV (%)	66 (5.5%)	N/A	21 (3.1%)	5 (0.5%)	N/A	1.5 (3.2%)	1.7 (0.14%)	1.4 (0.14%)	N/A
Temp. Range	°C	-40/+125	-15/150	0/80	-40/+120	-40/+120	-40/+110	-40/+140	-40/+140	-10/100
Nominal Temp. Coeff.	ppm/°C	30	3.9	10	147	4.5	30	22	7	16
Untrimm. TC, Avg.	ppm/°C	33	15.5	N/A	N/A	5	33	22.7	8.7	N/A
Untrimm. TC, Std. Dev.	ppm/°C (%)	33 (100%)	7.4 (45%)	N/A	N/A	1.5 (25%)	33 (100%)	1.7 (8%)	1.7 (19%)	N/A
Silicon Area	mm^2	0.0121	0.1019	0.045	0.030	0.036	0.0036	$0.0006^{\dagger a}$ $0.0007^{\dagger b}$ $1.02^{\dagger c}$	$0.0006^{\dagger a}$ $0.0007^{\dagger b}$ $1.02^{\dagger c}$	N/A
Line Regulation	%/V	0.05	0.039	0.27	1.5	0.1	1	0.08	0.02	0.15
Min. Supply Voltage	V	1.62	1.7	0.9	1.2	1.2	0.85	0.9	0.9	$2.4^{\natural}$
Power Cons.	μW	32	95	0.055	0.1	43	30	$20 \cdot \delta^{\ddagger a}$ $0.12^{\ddagger b}$	$20 \cdot \delta^{\ddagger a}$ $0.12^{\ddagger b}$	$120 \cdot \delta^{\ddagger c}$

$^{\sharp}$ Kuijk BGR standard cell in a 0.18μm CMOS technology. $^{\natural}$ Limited by the charateristics of the ADuC7061 microcontroller.
† Silicon area: *a*) phys. standard + S/H (PSH); *b*) PSH plus the area of the ADC [22] ($0.49\mathrm{mm}^2$) and of the DAC [23] ($0.53\mathrm{mm}^2$) scaled by $\delta = 10^{-4}$, evaluated as in (19) for $T_{\mathrm{REFR}} = 1$s and $T_{\mathrm{PVT}} = 100\mu$s (estimate based on [22]-[23]); *c*) PSH plus the total area of the ADC [22] and of the DAC [23].
† Power consumption: *a*) phys. standard + S/H (PSH), as a function of δ; *b*) PSH plus the power absorbed by the ADC in [22] (140μW) and by the DAC in [23] ($1.1\mathrm{mW}$) and considering $\delta = 10^{-4}$, *c*) PSH + ADuC7061 ADC and DAC, as a function of δ (estimated from the datasheet).

Second-order curvature is not present even though it has not been compensated by the VKB procedure. It is worth noting that the power supply voltage of the MCU, used as a pseudo-reference, undergoes a change of more than 25mV (1%) during this test, as shown in Fig.12. In the same figure it can be observed how the variations of the pseudo-reference are countered by opposite changes in the (digital) virtual reference so that to obtain the overall drift in Fig.11, in accordance with the theory in Section III.

From the bottom plot of Fig.11, a line regulation of $0.15\%/\mathrm{V}$ can be observed. Such performance is likely to be limited by the power supply rejection of the ADC in the ADuC7061, which is 55dB from the datasheets [30]. Finally, the measured root-mean-square (r.m.s.) noise of the reference voltage, evaluated taking the r.m.s. value of the D/A-converted virtual reference sampled after each iteration of the PVT compensation procedure, is about $35\mu\mathrm{V}$ r.m.s. and corresponds to about 1 LSB of the ADC and of the DAC in the prototype.

VII. COMPARISON AND DISCUSSION

The digital virtual voltage references introduced in this paper are compared in terms of performance with state-of-the-art analog references proposed in recent literature in Tab.I. The results of such a comparison are discussed in what follows.

A. Thermal Drift and Line Regulation

From the results in Tab.I, the proposed VKB and GVR references achieve a low thermal drift and a good line regulation, comparable with state-of-the-art analog references. For the GVR, in particular, the improvement in thermal drift achieved by signal processing techniques not suitable to be implemented in analog form, as discussed in Section V, can be appreciated.

B. Technology-related issues

The digital voltage references proposed in this paper can be operated from a power supply voltage as low as the minimum required by the digital core and by the physical standard (0.9V for the VKB and GVR, operation at lower supply can be achieved using MOS transistors in the subthreshold region [14]) and low voltage operation is not traded-off with accuracy. In particular, it can be observed that the digital references in Tab.I show a better untrimmed accuracy and a reduced spread of the untrimmed thermal drift in comparison with most analog implementations. This can be ascribed to the fact that the untrimmed performance of a digital reference is only limited by the variability of the physical standard in itself and/or by the ADC and DAC resolution and is not affected by the intrinsic limitations of analog signal processing, which are particularly severe in nano-scale technologies. Furthermore, circuit trimming, which could be still necessary to compensate process-related spreads of the physical standard, can be replaced by software calibration with a significant reduction in costs. The above features make digital references well-suited to aggressively scaled digital CMOS technologies.

Finally, even though the whole system in Fig.3 is much more complex than a stand-alone analog reference and the total area occupancy, considering the ADC in [22] and the DAC in [23] is about $1\mathrm{mm}^2$, the extra area needed to implement the digital references in a SoC including an ADC and a DAC, is limited to the area of the physical standard and of the S/H, which is only $600\mu\mathrm{m}^2$ in 180nm CMOS. Moreover, weighting the ADC and DAC area by the activity factor δ defined in (19), which can be conservatively estimated as 10^{-4} for the referenced ADC and DAC, their weighted area occupancy is only of $100\ \mu\mathrm{m}^2$.

C. Power Consumption and Start-up Issues

The power consumption P of a digital reference can be expressed in terms of the activity factor δ in (19) and of the average power $P_{\rm PVT}$, absorbed when the PVT compensation procedure is executed, as $P = \delta \cdot P_{\rm PVT}$. Being $P_{\rm PVT}$, in the milliwatt range ($1.2\rm mW$ for the VKB and GVR in Tab.I, including the ADC in [22] and the DAC in [23]), the actual power consumption of a digital reference can be as low as a few hundred nanowatts ($120\rm nW$ for the VKB and GVR in Tab.I) thanks to the scaling factor δ. It is worth noting that such low power consumption is achieved during normal operation and not switching off the reference when not in use.

Moreover, a start-up circuit is not required for a digital reference, provided that a roughly pre-regulated power supply voltage with a modest accuracy (of the order of $\pm 10\%$), sufficient just to safely operate the digital system, is provided at power up, before the virtual reference is evaluated for the first time. After the virtual voltage reference is available, it could be also exploited for power supply management, e.g. as a reference for integrated linear and/or switching-mode voltage regulators in a SoC.

VIII. Conclusion

A novel virtual voltage reference concept has been introduced and generalized in this paper to design mostly digital, PVT-independent voltage reference circuits suitable to replace analog references in present day, very low voltage, aggressively scaled integrated systems. The performance of digital voltage references based on the novel concept have been tested by simulations and experiments carried out an a microcontroller-based prototype and have been compared with state-of-the-art analog voltage references proposed in recent literature. On the basis of these results, the effectiveness and the potential of the proposed concept as a fully digital, new approach in integrated reference circuit design, is highlighted.

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Paolo S. Crovetti (S'00, M'03) was born in Torino, Italy, in 1976. He received the Laurea (summa cum laude) and Ph.D. degrees in Electronic Engineering from the Politecnico di Torino in 2000 and 2003, respectively. Currently he is with the Department of Electronics and Telecommunications (DET) of the Politecnico di Torino, Italy, where he works as an Assistant Professor of Electronics. His main research interests are in the fields of analog integrated circuits, nonlinear circuits, IC-level EMC. His recent research activities are focused on the development of fully digital implementations of analog functions and on the application of MIMO signal processing and RF techniques in EMC. He is co-author of more than 40 papers appearing in journals and international conference proceedings.