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Abstract

The errors which are induced by Radio-Frequency Interference in switched capacitor (SC) circuits are discussed and the main role played by the distortion of MOS switches in the on-state is highlighted. Furthermore, a new simple analytical model which enables one to predict RFI-induced errors in SC circuits is proposed and the validity of this model is verified by comparison of model predictions and time-domain computer simulation results.

Index Terms

Integrated Circuits, Switched Capacitors (SC) Circuits, Radio-Frequency Interference (RFI), Electromagnetic Interference (EMI).

I. Introduction

THE level of Electromagnetic Interference (EMI) is continuously increasing in the last years and unwanted RF voltages and currents are almost always superimposed onto nominal signals in any integrated circuit (IC). Such RF interference (RFI) affects the operation of baseband integrated circuits (ICs) up to cause serious failures [1-8], as a consequence, the prediction of the effects of RFI in baseband ICs and the design of ICs which are immune to RFI have become key issues in present day microelectronics.

In particular, the operation of switched capacitor (SC) circuits, which are widely employed in order to perform low frequency signal processing in ICs [9-10], can be severely impaired by RFI which is conveyed to SC circuits through the input terminal(s), through the power supply lines and through the silicon substrate. Even though the analysis and the design of MOS SC circuits, i.e. of circuits which only include MOS switches, capacitors and operational amplifiers (opamps), have been extensively discussed in the literature [11-14],

the failures, which are induced by RFI in SC circuits, cannot be highlighted by standard SC circuit analysis techniques. Such failures are related, in general, both to the opamp RFI-induced distortion and to the high-frequency behavior of MOS switches. While the nonlinear effects of RFI in opamp circuits have been previously discussed in the literature [6-8], the high-frequency distortion of MOS closed switches, that is the main (or the only) cause of RFI-induced failures in most practical SC circuits, deserves further investigation.

In this paper, the RFI-induced failures in SC circuits which are due to the high-frequency behavior of MOS switches are investigated with reference to some elementary SC circuits, that are the basic building blocks of complex SC filter architectures. In particular, RFI-induced errors in basic SC circuits are predicted by a new simple analytical model which relates such errors to design parameters and that can be directly employed in order to increase the immunity to RFI of SC circuits by design.

The paper has the following structure: in Section II, the effects of RFI in SC circuits are discussed and the basic SC topologies, which are considered in this paper, are introduced. In Section III, a model which is suitable to predict the errors induced in SC circuits by MOS switch high-frequency distortion is derived and such a model is employed, in Section IV, in order to predict the effects of continuous wave (CW) RFI in basic SC circuits. In Section V, model predictions are compared with the results of time-domain computer simulations and some considerations about the influence of design parameters on SC circuit distortion are discussed. Finally, in Section VI, some concluding remarks are drawn.

II. RFI Effects in Switched Capacitor Circuits

The failures which are induced in SC circuits by the high-frequency distortion of MOS switches are investigated in the following with reference to the elementary SC topologies in Fig.1. The RFI-induced failures in complex SC circuits such as SC filters and SC amplifiers

can be related to these basic SC topologies and/or to the distortion of RFI in negative feedback opamp circuits, which had been investigated in previous work [6].

The circuit in Fig.1a includes a capacitor C and an MOS switch M1 that connects the capacitor to the input voltage. Such a switch is driven by a square-wave clock signal $v_{\rm CK}$: during the clock high state (*track* phase), the switch M1 is on and connects the capacitor C to the input voltage while, during the clock low state (*hold* phase), the switch is off and the voltage across the capacitor is constant and equal to the voltage at the beginning of the *hold* phase. The transition between *track* and *hold* phases is the *sample* phase, which corresponds to the falling edge of the clock waveform. In the SC topology shown in Fig.1b, which is known as bottom plate sampling topology, the capacitor C is connected to the input voltage by the switch M1 and to the reference voltage by a second MOS switch, M2, which is driven by the same clock signal of M1.

With reference to the SC circuits in Fig.1, the effects of RFI are now described with reference to the *track*, *sample* and *hold* phases. To this purpose, it is assumed that the input voltage $v_{\rm IN}$ is in the form

$$v_{\rm IN}(t) = V_{\rm IN} + v_{\rm in}(t), \tag{1}$$

where $V_{\rm IN}$ is the nominal input voltage, that can be assumed to be constant during the track phase without loss of generality, and $v_{\rm in}(t)$ is the RFI term, whose mean value is zero. The typical waveforms of the SC circuit voltages in the presence of RFI are shown in Fig. 2.

A. Track Phase

During the *track* phase, the capacitor C is connected to the input voltage through the closed switch M1. If the input signal only includes spectral components with frequencies

that are much lower than the cutoff frequency

$$f_{\mathrm{SC}} = \frac{1}{2\pi r_{\mathrm{ON}} C},$$

where r_{ON} is the (equivalent) small-signal on-resistance of the closed switch(es), the output voltage v_{OUT} follows the input voltage v_{IN} almost instantaneously and the voltage across the switch(es) is almost zero. As a consequence, even though the on resistance of the switch(es) is nonlinear, such a nonlinearity is not excited and does not affect the output voltage.

On the contrary, in the presence of RFI, the input voltage may include relevant spectral components at frequencies that are much higher than f_{SC}. As a consequence, the RF voltage across M1 (and M2) is non-zero and excites the nonlinear characteristics of the on switch(es). For this reason, in the presence of RFI, the output voltage, which can be expressed as

$$v_{\mathrm{OUT}}(t) = V_{\mathrm{OUT}} + v_{\mathrm{out}}(t), \tag{2}$$

where V_{OUT} is the DC term of the output voltage and $v_{\mathrm{out}}(t)$ is the zero-mean RFI component of the output voltage, does not track v_{IN}. In particular, $v_{\mathrm{out}}(t) \neq v_{\mathrm{in}}(t)$, as the zero-mean RFI component of the input voltage is attenuated by the low-pass filtering effect of r_{ON} and C, while $V_{\mathrm{OUT}} \neq V_{\mathrm{IN}}$ because of the distortion of the on switch(es).

B. Sample Phase

With reference to Fig.2, the *sample* phase coincides with the falling edge of the clock waveform, in which the nonlinear conductance of the switch(es) changes from the on-state value to zero. During this phase, the output voltage is still sensitive to the input voltage and, as a consequence, the voltage which is stored in the output capacitor at the sampling instant T_{S}, in which the clock transition terminates, in general, is a function of the input waveform during the whole *sample* phase.

The effects of the input voltage changes during the *sample* phase have been investigated in [15] with reference to *track-and-hold* mixers. Nonetheless, computer simulations show that, if the falling time of the clock waveform $t_{\rm f}$ is negligible with respect to the on-state time constant

$$\tau = r_{\rm ON} C,$$

as in almost all practical SC circuits, the changes of the output voltage during the *sample* phase are negligible independently of the frequency of the input signal and the voltage that is sampled on the capacitor C can be conveniently approximated as

$$V_{\rm S} = v_{\rm OUT}(T_{\rm S}) + V_{\rm CH} \tag{3}$$

where $v_{\rm OUT}(T_{\rm S})$ is the sample of the track-state *output* voltage $v_{\rm OUT}(t)$, given by Eqn.(2), at the instant $T_{\rm S}$ in which the switch(es) is (are) completely turned off (i.e., if $i_{\rm SW}(t)$ is the current which flows through the switch(es), $i_{\rm SW}(t) = 0$ for $t > T_{\rm S}$) and $V_{\rm CH}$ is an additive error term due to charge injection. The error term $V_{\rm CH}$, which takes into account the charge that is injected into the capacitor C through the parasitic capacitances of the MOS transistor(s) during the falling edge of the clock signal, is not affected by the presence of RFI and it will not be considered hereafter.

C. Hold Phase

In the hold phase, the switch(es) is (are) off, the capacitor C is ideally disconnected from the input signal and it stores the voltage $V_{\rm S}$. Nonetheless, very high frequency RFI can bypass the off-state switch(es) because of its (their) nonzero drain-to-source capacitance. In particular the output voltage can be expressed as

$$v_{\rm OUT}(t) = V_{\rm S} + v_{\rm out}(t) = V_{\rm S} + \frac{C_{\rm DS}}{C_{\rm DS} + C}\, v_{\rm in}(t). \tag{4}$$

where, with reference to the circuit in Fig. 1a, $C_{\rm DS}$ is the drain-to-source capacitance of M1 and, with reference to the circuit in Fig. 1b,

$$C_{\rm DS} = \frac{C_{\rm DS1} C_{\rm DS2}}{C_{\rm DS1} + C_{\rm DS2}},$$

where $C_{\rm DS1}$ and $C_{\rm DS2}$ are the drain-to-source capacitances of M1 and M2, respectively. In both the circuits, and in any practical SC circuit, the contribution of RFI, $v_{\rm out}(t)$, is always negligible because $C_{\rm DS} \ll C$ and it will not be considered hereafter.

In conclusion, with reference to Fig. 2, the voltage $V_{\rm S}$, which is stored in the capacitor C during the *hold* phase, can be expressed as

$$\begin{aligned} V_{\rm S} &= V_{\rm OUT} + v_{\rm out}(T_{\rm S}) + V_{\rm CH} \\ &= V_{\rm IN} + (V_{\rm OUT} - V_{\rm IN}) + v_{\rm out}(T_{\rm S}) + V_{\rm CH} \\ &= V_{\rm IN} + \Delta V + \delta V + V_{\rm CH}, \end{aligned} \tag{5}$$

where $V_{\rm IN}$ is the nominal input voltage which should be sampled, ΔV is the RFI-induced offset in the sampled voltage, while δV is a sample of the zero-mean high-frequency RFI term $v_{\rm out}(t)$ and $V_{\rm CH}$ is the error term due to charge injection.

In the following Section, the RFI-induced errors ΔV and δV in the circuit of Fig.1a are predicted and related to the SC circuit parameters, to the amplitude of RFI and to its frequency. The RFI induced errors in the circuit of Fig.1b will be considered in Section IV.

III. Prediction of RFI-Induced Errors in Switched Capacitor Circuits

In this Section, the RFI-induced errors in the sampled voltage ΔV and δV, which have been highlighted in Eqn.(5), are predicted by a new analytical model with reference to the basic SC circuit in Fig.1a. In particular, the bulk-referred EKV model [16] for the operation of the MOS transistor in the linear region, which is employed to describe the nonlinear

behavior of MOS switches, is firstly presented. Then, the errors which are induced by RFI that is superimposed onto the input voltage of the circuit in Fig.1a are predicted under the hypothesis that the MOS switch always operates in the linear region during the *hold* phase. Finally, the effects of RFI which is superimposed onto the clock and/or onto the substrate voltage are taken into account and the hypothesis of operation in the linear region for the MOS switch is removed.

A. Bulk-Referred MOS Transistor Model

In MOS floating switches, that are employed in SC circuits (e.g. M1 in Fig.1a), source and drain terminals are not properly defined, as the voltage of one terminal can be either higher or lower than the voltage of the other terminal, even during the same phase. For this reason, the operation of MOS switches in SC circuits is conveniently described employing a bulk-referred model for the MOS switch, i.e. a model in which the terminal voltages of the MOS device are referred to the bulk voltage rather than to the source voltage. For this reason, the bulk-referred EKV model presented in [16], is employed in the following to analyze RFI-induced distortion in SC circuits.

According to the EKV model, with reference to Fig.3, the current which flows through an MOS switch in the on state is expressed as

$$i_{\mathrm{SW}}\left(v_{\mathrm{A}}, v_{\mathrm{B}}\right) = n\beta\left(v_{\mathrm{P}} - \frac{v_{\mathrm{A}} + v_{\mathrm{B}}}{2}\right)\left(v_{\mathrm{A}} - v_{\mathrm{B}}\right), \tag{6}$$

where v_{A} and v_{B} are the bulk-referred terminal voltages of the MOS switch (the current is assumed to flow from terminal A to terminal B), β is the transconductance parameter, which is defined as

$$\beta = \mu C_{\mathrm{ox}} \frac{W}{L},$$

where μ is the mobility of the channel carriers, C_{ox} is the gate capacitance per unit area, $\frac{W}{L}$

is the aspect ratio of the transistor,

$$v_{\mathrm{P}} = v_{\mathrm{G}} - V_{\mathrm{T0}} - \gamma \left[\sqrt{v_{\mathrm{G}} - V_{\mathrm{T0}} + \left(\Psi_0 + \frac{\gamma}{2} \right)^2} - \left(\Psi_0 + \frac{\gamma}{2} \right) \right] \tag{7}$$

in which v_{G} is the bulk-referred gate voltage, V_{T0} is the bulk-referred threshold voltage (which is, in general, different from the usual source-referred threshold voltage), Ψ_0 is the approximation of the surface potential in strong inversion at equilibrium and γ is the body effect factor which is defined as

$$\gamma = \frac{\sqrt{2\mathrm{q}\epsilon_{\mathrm{S}} N_{\mathrm{sub}}}}{C_{\mathrm{ox}}}$$

where q is the elementary charge, ϵ_{S} is the silicon permittivity and N_{sub} is the doping concentration of the substrate. Finally, the slope factor n is defined as

$$n = \frac{\mathrm{d}v_{\mathrm{G}}}{\mathrm{d}v_{\mathrm{P}}} = 1 + \frac{\gamma}{2\sqrt{\Psi_0 + v_{\mathrm{P}}}}. \tag{8}$$

The model in Eqn.(6) is valid for MOS transistors which are biased in the linear region, i.e., under the assumption that both $v_{\mathrm{A}} < v_{\mathrm{P}}$ and $v_{\mathrm{B}} < v_{\mathrm{P}}$. If either $v_{\mathrm{A}} > v_{\mathrm{P}}$ or $v_{\mathrm{B}} > v_{\mathrm{P}}$, the MOS transistor is biased in the saturation region. In particular, if $v_{\mathrm{A}} > v_{\mathrm{P}}$ and $v_{\mathrm{B}} < v_{\mathrm{P}}$, the current $i_{\mathrm{SW,sat}}$ which flows through the switch, neglecting the channel length modulation effect, can be written as

$$i_{\mathrm{SW,sat}}\left(v_{\mathrm{A}}, v_{\mathrm{B}}\right) = \frac{n\beta}{2}\left(v_{\mathrm{P}} - v_{\mathrm{B}}\right)^2 = i_{\mathrm{SW}}\left(v_{\mathrm{P}}, v_{\mathrm{B}}\right), \tag{9}$$

while, if $v_{\mathrm{A}} < v_{\mathrm{P}}$ and $v_{\mathrm{B}} > v_{\mathrm{P}}$,

$$i_{\mathrm{SW,sat}}\left(v_{\mathrm{A}}, v_{\mathrm{B}}\right) = -\frac{n\beta}{2}\left(v_{\mathrm{P}} - v_{\mathrm{A}}\right)^2 = i_{\mathrm{SW}}\left(v_{\mathrm{A}}, v_{\mathrm{P}}\right), \tag{10}$$

where $i_{\mathrm{SW}}\left(v_{\mathrm{A}}, v_{\mathrm{B}}\right)$ is the expression of the MOS current in the linear region given in Eqn.(6). Equations (6), (9) and (28) will be employed in the following in order to predict the errors which are induced in the sampled voltage of a SC circuit in the presence of RFI.

B. Basic Derivation

With reference to the SC circuit in Fig.1a in the *track* phase, assuming that the MOS switch operates in the linear region, from Eqns. (1), (2) and (6) the current $i_{\rm SW}$ which flows through the switch can be expressed as

$$\begin{aligned} i_{\rm SW} &= n\beta\left[V_{\rm P}-\frac{1}{2}\left(V_{\rm IN}+v_{\rm in}+V_{\rm OUT}+v_{\rm out}\right)\right]\left(V_{\rm IN}+v_{\rm in}-V_{\rm OUT}-v_{\rm out}\right) \\ &= n\beta\left[V_{\rm P}\left(V_{\rm IN}-V_{\rm OUT}+v_{\rm in}-v_{\rm out}\right)-\frac{1}{2}\left(V_{\rm IN}+v_{\rm in}\right)^2+\frac{1}{2}\left(V_{\rm OUT}+v_{\rm out}\right)^2\right], \end{aligned} \tag{11}$$

in which $V_{\rm P}$ is the value of $v_{\rm P}$ given by (7) for $v_{\rm G}=V_{\rm G}$, where $V_{\rm G}$ is the gate voltage of the MOS switch in the *track* phase, that is now assumed to be constant and not affected by RFI.

The current $i_{\rm SW}$ also flows through the capacitor C and, consequently, in steady state condition[1], its mean value $\overline{i_{\rm SW}}$ is zero, i.e.

$$\overline{i_{\rm SW}}=n\beta\left[V_{\rm P}\left(V_{\rm IN}-V_{\rm OUT}\right)-\frac{1}{2}\left(V_{\rm IN}^2+\overline{v_{\rm in}^2}-V_{\rm OUT}^2-\overline{v_{\rm out}^2}\right)\right]=0, \tag{12}$$

where zero mean terms have been dropped and where $\overline{v_{\rm in}^2}$ and $\overline{v_{\rm out}^2}$ are the mean-square values of the RFI voltages $v_{\rm in}$ and $v_{\rm out}$, respectively.

Equation (12) can be solved in order to find out the mean value of the output voltage $V_{\rm OUT}$. To this purpose, it should be rearranged as

$$V_{\rm OUT}^2-2V_{\rm P}V_{\rm OUT}+2V_{\rm P}V_{\rm IN}-V_{\rm IN}^2-\overline{v_{\rm in}^2}+\overline{v_{\rm out}^2}=0 \tag{13}$$

which gives:

$$\begin{aligned} V_{\rm OUT} &= V_{\rm P}-\sqrt{V_{\rm P}^2-2V_{\rm P}V_{\rm IN}+V_{\rm IN}^2+\overline{v_{\rm in}^2}-\overline{v_{\rm out}^2}} \\ &= V_{\rm P}-\left(V_{\rm P}-V_{\rm IN}\right)\sqrt{1+\frac{\overline{v_{\rm in}^2}-\overline{v_{\rm out}^2}}{\left(V_{\rm P}-V_{\rm IN}\right)^2}}. \end{aligned} \tag{14}$$

[1] the steady state condition is always reached at the end of the track phase, as the time constant $\tau=r_{\rm ON}C$ must be much smaller than the duration of the hold phase, in order to assure the correct operation of an SC circuit at a given clock frequency.

As a consequence, the RFI-induced offset term ΔV can be expressed as

$$\Delta V = V_{\mathrm{OUT}} - V_{\mathrm{IN}} = (V_{\mathrm{P}} - V_{\mathrm{IN}}) \left(1 - \sqrt{1 + \frac{\overline{v_{\mathrm{in}}^2} - \overline{v_{\mathrm{out}}^2}}{(V_{\mathrm{P}} - V_{\mathrm{IN}})^2}} \right). \tag{15}$$

From Eqn.(15) it can be observed that the RFI-induced distortion in the MOS switch is driven by the difference in the mean-square values of RFI superimposed onto the input and the output terminals. For low-frequency operation, the mean-square value of the input waveform is identical to the mean-square value of the output waveform, as a consequence, according with (15), no offset is generated.

Equation (15) enables one to predict the RFI-induced offset in the circuit of Fig.1a in the presence of RFI with an arbitrary power spectral density (PSD). In particular, if $S_{V_{\mathrm{in}}}(\omega)$ is the PSD of the RFI superimposed onto the input voltage of the SC circuit, the mean-square value of the input voltage $\overline{v_{\mathrm{in}}^2}$ can be evaluated as

$$\overline{v_{\mathrm{in}}^2} = \int_{-\infty}^{+\infty} S_{V_{\mathrm{in}}}(\omega) \mathrm{d}\omega \tag{16}$$

and the mean-square value of the output voltage $\overline{v_{\mathrm{out}}^2}$ can be calculated, with good approximation, by frequency domain linear analysis, neglecting the distortion due to the switch in the on state:

$$\overline{v_{\mathrm{out}}^2} = \int_{-\infty}^{+\infty} S_{V_{\mathrm{in}}}(\omega) \left| H(\omega) \right|^2 \mathrm{d}\omega \tag{17}$$

where

$$H(\omega) = \frac{V_{\mathrm{out}}(\omega)}{V_{\mathrm{in}}(\omega)} = \frac{1}{1 + \mathrm{j}\omega C r_{\mathrm{ON}}} \tag{18}$$

is the frequency domain transfer function of the SC circuit in the *track* phase and, on the basis of the MOS model (6),

$$r_{\mathrm{ON}} = \left(\left. \frac{\partial i_{\mathrm{SW}}}{\partial v_{\mathrm{AB}}} \right|_{v_{\mathrm{A}}, v_{\mathrm{B}} = V_{\mathrm{IN}}} \right)^{-1} = \frac{1}{n\beta \left(V_{\mathrm{P}} - V_{\mathrm{IN}} \right)}. \tag{19}$$

From Eqn.(17), the root-mean-square (rms) value of the zero-mean error due to sampled RFI, δV, defined in Eqn. (5), can be predicted as well. In particular

$$\delta V_{\rm rms} = \sqrt{\overline{v_{\rm out}^2}}. \tag{20}$$

In the special case of CW RFI, i.e. if the input signal $v_{\rm IN}$ is written in the form

$$v_{\rm IN} = V_{\rm IN} + V_{\rm in}\cos\left(\omega_0 t\right), \tag{21}$$

where $V_{\rm IN}$ is the nominal DC signal, $V_{\rm in}$ is the peak amplitude of CW RFI and ω_0 is the angular frequency of CW RFI, the mean-square value of the input voltage is given by

$$\overline{v_{\rm in}^2} = \frac{V_{\rm in}^2}{2} \tag{22}$$

and, from Eqn.(17), the mean-square value of the output voltage is expressed as

$$\overline{v_{\rm out}^2} = \frac{V_{\rm in}^2}{2}\frac{1}{1+\omega_0^2 r_{\rm ON}^2 C^2}. \tag{23}$$

As a consequence, from (15), (17) and (22), in the special case of CW RFI,

$$\Delta V = \left(V_{\rm P} - V_{\rm IN}\right)\left(1 - \sqrt{1 + \frac{V_{\rm in}^2}{2\left(V_{\rm P} - V_{\rm IN}\right)^2}\frac{\omega_0^2 r_{\rm ON}^2 C^2}{1+\omega_0^2 r_{\rm ON}^2 C^2}}\right) \tag{24}$$

and

$$\delta V_{\rm rms} = \frac{V_{\rm in}}{\sqrt{2}}\sqrt{\frac{1}{1+\omega_0^2 r_{\rm ON}^2 C^2}}. \tag{25}$$

C. RFI Superimposed onto the Gate and onto the Substrate Voltage

The predictions which have been obtained by Eqn.(15) can be extended in order to take into account the effects of RFI which is superimposed onto the gate voltage and/or onto the substrate voltage. To this purpose, with reference to Fig.4, the bulk-referred gate voltage of the MOS transistor can be expressed as

$$v_{\rm G}(t) = V_{\rm G} + v_{\rm g}(t) - v_{\rm b}(t)$$

where $V_{\rm G}$ is the nominal bulk-referred voltage and $v_{\rm g}$ and $v_{\rm b}$ are the zero-mean RFI terms which are superimposed onto the gate voltage and onto the substrate voltage, respectively.

Neglecting the distortion due to the body effect and neglecting the RFI induced fluctuations of the slope factor n, the voltage $v_{\rm P}$ in Eqn.(7), in the presence of RFI onto the gate and substrate voltages, can be expressed as

$$v_{\rm P} = V_{\rm P} + \frac{v_{\rm g}(t) - v_{\rm b}(t)}{n} = V_{\rm P} + v_{\rm n}(t) \tag{26}$$

where $V_{\rm P}$ is the nominal value of $v_{\rm P}$ when no gate and/or substrate RFI is considered, and

$$v_{\rm n}(t) = \frac{v_{\rm g}(t) - v_{\rm b}(t)}{n} \simeq v_{\rm g}(t) - v_{\rm b}(t).$$

On the basis of Eqns. (6) and (26), the current $i^{\circ}_{\rm SW}$ which flows through the MOS switch in the presence of RFI superimposed onto the gate and onto the substrate voltage can be written as

$$\begin{aligned} i^{\circ}_{\rm SW}(v_{\rm A}, v_{\rm B}) &= n\beta\left(V_{\rm P} + v_{\rm n} - \frac{v_{\rm A}+v_{\rm B}}{2}\right)(v_{\rm A} - v_{\rm B}) \\ &= n\beta\left[V_{\rm P} - \frac{(v_{\rm A}-v_{\rm n})+(v_{\rm B}-v_{\rm n})}{2}\right][(v_{\rm A}-v_{\rm n}) - (v_{\rm B}-v_{\rm n})] \\ &= i_{\rm SW}(v_{\rm A}-v_{\rm n}, v_{\rm B}-v_{\rm n}). \end{aligned} \tag{27}$$

As a consequence, the circuit in Fig.4a is equivalent in terms of RFI-induced distortion to the circuit in Fig.4b and the effects of RFI superimposed onto the gate voltage and onto the substrate voltage in the circuit in Fig.4a can be predicted by Eqn.(15) with reference to the circuit in Fig.4b.

D. MOS Switch out of the linear region

In the above derivation, the effects of RFI on the circuit in Fig.1a have been predicted under the assumption that the MOS transistor M1 operates in the linear region during the

track phase, i.e., with reference to Fig.1a, assuming that both $v_{\mathrm{IN}} < v_{\mathrm{P}}$ and $v_{\mathrm{OUT}} < v_{\mathrm{P}}$. These conditions, unfortunately, are not always met when large signal RFI is applied and/or when the nominal signal voltage V_{IN} approaches V_{P}. Nonetheless, the model which has been presented above can be extended to cover these cases.

To this purpose, from Eqn.(9), neglecting the channel length modulation effect, if $v_{\mathrm{IN}} > v_{\mathrm{P}}$, the switch current can be expressed as

$$i_{\mathrm{SW,sat}}\left(v_{\mathrm{IN}}, v_{\mathrm{OUT}}\right) = i_{\mathrm{SW}}\left(v_{\mathrm{P}}, v_{\mathrm{OUT}}\right), \tag{28}$$

whereas, if $v_{\mathrm{OUT}} > v_{\mathrm{P}}$

$$i_{\mathrm{SW,sat}}\left(v_{\mathrm{IN}}, v_{\mathrm{OUT}}\right) = i_{\mathrm{SW}}\left(v_{\mathrm{IN}}, v_{\mathrm{P}}\right). \tag{29}$$

Merging the results of Eqns. (6), (28) and (29), the current $i^{\star}_{\mathrm{SW}}\left(v_{\mathrm{IN}}, v_{\mathrm{OUT}}\right)$, which flows through an MOS switch in any region of operation, can be related the expression of the current which flows through an MOS switch in the linear region $i_{\mathrm{SW}}\left(v_{\mathrm{A}}, v_{\mathrm{B}}\right)$ in Eqn.(6), as follows

$$i^{\star}_{\mathrm{SW}}\left(v_{\mathrm{IN}}, v_{\mathrm{OUT}}\right) = i_{\mathrm{SW}}\left(v^{\star}_{\mathrm{IN}}, v^{\star}_{\mathrm{OUT}}\right) \tag{30}$$

where

$$v^{\star}_{\mathrm{IN}} = \min\left(v_{\mathrm{IN}}, v_{\mathrm{P}}\right) \tag{31}$$

and

$$v^{\star}_{\mathrm{OUT}} = \min\left(v_{\mathrm{OUT}}, v_{\mathrm{P}}\right) \tag{32}$$

It can be observed that, if both $v_{\mathrm{IN}} > v_{\mathrm{P}}$ and $v_{\mathrm{OUT}} > v_{\mathrm{P}}$, the MOS switch is off and Eqn. (30) correctly predicts

$$i^{\star}_{\mathrm{SW}}\left(v_{\mathrm{IN}}, v_{\mathrm{OUT}}\right) = i_{\mathrm{SW}}\left(v_{\mathrm{P}}, v_{\mathrm{P}}\right) = 0.$$

On the basis of Eqn.(30), the RFI-induced errors in the circuit of Fig.5a, with no hypothesis on v_{IN}, can be related to the distortion of the circuit in Fig.5b , in which the MOS

transistor is always biased in the linear region. To this purpose, it should be observed that, from the equivalence (30), the currents which flow through the switches of the circuits in Fig.5 are the same. In fact, with reference to the circuit in Fig.5a, assuming a zero initial condition for the capacitor C, the output voltage $v_{\rm OUT}$ is driven by the input voltage through the switch M1, as a consequence the inequality $v_{\rm OUT} < v_{\rm P}$ is always satisfied and $v^{\star}_{\rm OUT} = v_{\rm OUT}$. From the equality of the switch instantaneous currents and from the substitution theorem, it follows that the output voltages $v_{\rm OUT}$ of the two circuits are identical, too.

The RFI-induced errors ΔV^{*} and $\delta V^{\star}_{\rm rms}$ in the circuit of Fig.5b can be predicted on the basis of Eqns.(15) and (20), with reference to the input voltage

$$v^{\star}_{\rm IN}(t) = V^{\star}_{\rm IN} + v^{\star}_{\rm in}(t)$$

in which $V^{\star}_{\rm IN}$ is the mean value of the input signal clamped to $V_{\rm P}$ and $v^{\star}_{\rm in}$ is the zero-mean component of the same signal. The values of $V^{\star}_{\rm IN}$ and $v^{\star}_{\rm in}$ in the case of CW RFI are expressed in terms of $V_{\rm IN}$, $V_{\rm in}$ and $V_{\rm P}$ in Appendix A.

As the output voltages of the circuits in Fig.5 are the same, the RFI-induced errors ΔV and $\delta V_{\rm rms}$ in the circuit of Fig.5a, can be expressed as

$$\delta V_{\rm rms} = \delta V^{\star}_{\rm rms} \tag{33}$$

$$\begin{aligned} \Delta V &= V_{\rm OUT} - V_{\rm IN} = V^{\star}_{\rm OUT} - V^{\star}_{\rm IN} + V^{\star}_{\rm IN} - V_{\rm IN} \\ &= \Delta V^{\star} + V^{\star}_{\rm IN} - V_{\rm IN}. \end{aligned} \tag{34}$$

The equivalence which has been shown above can also be applied to the circuit which takes into account the effects of RFI that is superimposed onto the switch gate voltage and/or onto the substrate voltage and enables one to predict RFI-induced errors in the SC circuit of Fig.1a under general RFI excitation.

IV. Bottom-Plate Sampling Topology

The results which have been presented with reference to the basic SC block in Fig.1a can be extended to more complex topologies which are employed in SC filter design. In particular, the RFI-induced errors in the SC configuration of Fig.1b, which is known as *bottom plate sampling* topology, is now considered.

To this purpose, with reference to Fig.1, it should be observed that, in steady state conditions, the mean currents which flow through the switches M1 and M2 are both zero, as a consequence, Eqn.(15) holds for each switch separately and the overall RFI-induced offset error across the capacitor C can be expressed as the difference of the RFI offset at node A and node B separately. In particular, the RFI offset sampled on the capacitor C can be written as

$$\Delta V = (V_{\mathrm{P}} - V_{\mathrm{IN}}) \left(1 - \sqrt{1 + \frac{\overline{v_{\mathrm{in}}^2} - \overline{v_{\mathrm{A}}^2}}{(V_{\mathrm{P}} - V_{\mathrm{IN}})^2}} \right) - V_{\mathrm{P}} \left(1 - \sqrt{1 - \frac{\overline{v_{\mathrm{B}}^2}}{V_{\mathrm{P}}^2}} \right) \tag{35}$$

where $\overline{v_{\mathrm{in}}^2}$, $\overline{v_{\mathrm{A}}^2}$ and $\overline{v_{\mathrm{B}}^2}$ are the mean-square values of the RFI voltages superimposed onto the input voltage, onto the voltage at node A and onto the voltage at node B respectively.

In particular, $\overline{v_{\mathrm{A}}^2}$ and $\overline{v_{\mathrm{B}}^2}$ can be related to the power spectral density of the input RFI voltage $S_{V_{\mathrm{in}}}(\omega)$ as

$$\overline{v_{\mathrm{A}}^2} = \int_{-\infty}^{+\infty} S_{V_{\mathrm{in}}}(\omega) \left| H_{\mathrm{A}}(\omega) \right|^2 \mathrm{d}\omega \tag{36}$$

and

$$\overline{v_{\mathrm{B}}^2} = \int_{-\infty}^{+\infty} S_{V_{\mathrm{in}}}(\omega) \left| H_{\mathrm{B}}(\omega) \right|^2 \mathrm{d}\omega \tag{37}$$

where

$$H_{\mathrm{A}}(\omega) = \frac{1 + \mathrm{j}\omega C r_{\mathrm{ON},2}}{1 + \mathrm{j}\omega C \left(r_{\mathrm{ON},1} + r_{\mathrm{ON},2} \right)} \tag{38}$$

and

$$H_{\mathrm{B}}(\omega) = \frac{\mathrm{j}\omega C r_{\mathrm{ON},2}}{1 + \mathrm{j}\omega C \left(r_{\mathrm{ON},1} + r_{\mathrm{ON},2} \right)}, \tag{39}$$

where $r_{\mathrm{ON},1}$ and $r_{\mathrm{ON},2}$ are the on-state resistances of MOS switches M1 and M2 respectively. Finally, the rms value of the zero-mean error across the capacitor C can be expressed as

$$\delta V_{\mathrm{rms}} = \sqrt{\overline{v_{\mathrm{AB}}^2}} = \sqrt{\int_{-\infty}^{+\infty} S_{V_{\mathrm{in}}}(\omega) \left| H_{\mathrm{A}}(\omega) - H_{\mathrm{B}}(\omega) \right|^2 \mathrm{d}\omega}. \tag{40}$$

In the case of CW RFI, from Eqns.(35), (38) and (39), the RFI-induced offset voltage is expressed as

$$\begin{aligned} \Delta V &= (V_{\mathrm{P}} - V_{\mathrm{IN}}) \left(1 - \sqrt{1 + \frac{V_{\mathrm{in}}^2}{2 (V_{\mathrm{P}} - V_{\mathrm{IN}})^2} \frac{\omega_0^2 r_{\mathrm{ON},1} (r_{\mathrm{ON},1} + 2 r_{\mathrm{ON},2}) C^2}{1 + \omega_0^2 C^2 (r_{\mathrm{ON},1} + r_{\mathrm{ON},2})^2}} \right) + \\ &- V_{\mathrm{P}} \sqrt{1 - \frac{V_{\mathrm{in}}^2}{2 V_{\mathrm{P}}^2} \frac{\omega_0^2 r_{\mathrm{ON},2} C^2}{1 + \omega_0^2 C^2 (r_{\mathrm{ON},1} + r_{\mathrm{ON},2})^2}}. \end{aligned} \tag{41}$$

while, from Eqn.(40), the rms value of δV is expressed as

$$\delta V_{\mathrm{rms}} = \frac{V_{\mathrm{in}}}{\sqrt{2}} \left| H_{\mathrm{A}}(\omega_0) - H_{\mathrm{B}}(\omega_0) \right|. \tag{42}$$

With reference to the circuit in Fig.1b, the effects of RFI that is superimposed onto the gate and onto the substrate voltage can be taken into account employing the equivalence described in Sec.IIIC to M1 and M2 separately and then applying Eqns.(35) and (40) to the equivalent circuit. The effects of the operation of transistors M1 and M2 out of the linear region can be predicted employing the approach which has been presented in Sec.IIID.

V. Model Validation

The basic SC circuit in Fig.1a has been simulated using Spectre, a Spice-like circuit simulator, with reference to the MOS devices of the 0.8μm technology BYQ by AMS, in order to evaluate the RFI induced offset ΔV due to RFI and the results of time-domain computer simulations have been compared with the predictions obtained from Eqn.(24).

In Figg. 6, 7, 8, and 9, the SC circuit in Fig.1a is considered and the CW RFI induced offset ΔV has been plotted, respectively, versus the amplitude of CW RFI, versus

the frequency of CW RFI, versus the nominal DC value of the input voltage and versus the on-state time constant $\tau = r_{\rm ON}C$ of the SC circuit. In Fig.10, the RFI induced offset ΔV is plotted versus the peak amplitude of CW RFI superimposed onto the substrate voltage, comparing the effects of RFI which is superimposed onto the substrate voltage only and the effects of the simultaneous presence of CW RFI superimposed onto the substrate and onto the input voltages. For the quantities which are not considered in the different sweeps, the parameters in Tab.I have been employed[2]. The predictions which have been obtained by Eqn. (24) are shown in continuous line, while the crosses represent the results of computer simulations. It can be observed that in all cases the agreement of model prediction with computer simulations is good and, consequently, the model which has been proposed above is suitable to discuss the influence of different parameters in RFI-induced distortion.

In Figg. 11 and 12, the RFI-induced offset in the SC circuit in Fig.1b is considered and it is plotted versus the amplitude and frequency of CW RFI respectively. With reference to this circuit, two identical MOS switches have been assumed and for each switch the parameters in Tab.I have been considered. The predictions which have been obtained by the model equation (41) are shown in continuous line, while the crosses represent the results of computer simulations. Even in this case, the agreement between model prediction and simulation results is good.

On the basis of the results in Figg.6-12, the effects of different SC design parameters on RFI induced offset can be discussed. In particular, from Figg.6 and 7,it can be observed that RFI-induced offset increases with the amplitude of RFI and increases with the frequency of RFI, according with the considerations which have been presented in Section II.

From Fig.9 it can be observed that, for a given frequency of RFI, the RFI-induced

[2] The sweep in Fig.9 has been obtained for a constant aspect ratio of the MOS switch and different values of the hold capacitor C. An identical result is obtained if C is kept constant and the aspect ratio of the MOS switch is swept in order to get a given value of τ.

offset increases with the time constant of the SC circuit. As a consequence, the choice of a large time constant of the SC circuit (i.e. the choice of a large hold capacitance and/or a low aspect ratio of the MOS switch) in order to limit the bandwidth of a SC circuit is not effective in order to reduce the RFI-induced offset error. Furthermore, from Fig.8, it can be observed that the RFI-induced distortion in a SC circuit depends on the value of the input signal: in particular, it increases as the input voltage increases and the MOS transistor reaches the limit of the linear region of operation. Finally, in Fig.10, it can be observed that an SC circuit is more susceptible to RFI superimposed onto the input voltage than to RFI superimposed onto the substrate voltage. Nonetheless, the effects of RFI onto the input voltage are magnified by the simultaneous presence of RFI superimposed onto the substrate voltage.

VI. Conclusion

In this paper the errors which are induced in SC circuits by the high-frequency nonlinear behavior of MOS switches have been discussed and the main role which is played by the distortion of MOS switches in the on-state during the *track* phase has been highlighted. Such a distortion has been analyzed employing a suitable bulk-referred model for the MOS transistor and an analytical model which relates RFI-induced errors to SC parameters has been proposed. The predictions of this model have been compared with the results of time-domain computer simulations and the agreement between predicted and simulated results is very good.

Appendix I

If the input signal is in the form

$$v_{\mathrm{IN}} = V_{\mathrm{IN}} + V_{\mathrm{in}} \cos\left(\omega_0 t\right),$$

and $V_{\rm P}$ is a constant voltage, $V_{\rm IN}^{\star}$ can be expressed as

$$\begin{aligned} V_{\rm IN}^{\star} &= \frac{1}{T}\int_0^T \min\left(V_{\rm IN}+V_{\rm in}\cos\left(\omega_0 t\right),V_{\rm P}\right)\mathrm{d}t \\ &= \frac{1}{T}\int_0^T \min\left(V_{\rm IN}-V_{\rm P}+V_{\rm in}\cos\left(\omega_0 t\right),0\right)\mathrm{d}t+V_{\rm P} \\ &= V_{\rm in}\frac{1}{T}\int_0^T \min\left(\frac{V_{\rm IN}-V_{\rm P}}{V_{\rm in}}+\cos\left(\omega_0 t\right),0\right)\mathrm{d}t+V_{\rm P} \\ &= V_{\rm in}F_1\left(\frac{V_{\rm IN}-V_{\rm P}}{V_{\rm in}}\right)+V_{\rm P} \end{aligned} \tag{43}$$

where $T=\frac{2\pi}{\omega_0}$ and

$$F_1(x)=\int_0^1 \min\left(x+\cos\left(2\pi y\right),0\right)\mathrm{d}y \tag{44}$$

can be expressed as

$$F_1(x)=\begin{cases} x & x<-1 \\ \frac{1}{\pi}\left(x\arccos(x)-\sqrt{1-x^2}\right) & -1\le x\le 1 \\ 0 & x>1 \end{cases}. \tag{45}$$

The mean-square value of $v_{\rm in}^{\star}$, $\overline{v_{\rm in}^{\star}}^2$, can be expressed as

$$\begin{aligned} \overline{v_{\rm in}^{\star}}^2 &= \frac{1}{T}\int_0^T \left[\min\left(V_{\rm IN}+V_{\rm in}\cos\left(\omega_0 t\right),V_{\rm P}\right)-V_{\rm IN}^{\star}\right]^2\mathrm{d}t \\ &= \frac{1}{T}\int_0^T \left[V_{\rm in}\min\left(\frac{V_{\rm IN}-V_{\rm P}}{V_{\rm in}}+\cos\left(\omega_0 t\right),0\right)-V_{\rm in}F_1\left(\frac{V_{\rm IN}-V_{\rm P}}{V_{\rm in}}\right)\right]^2\mathrm{d}t \\ &= V_{\rm in}^2\frac{1}{T}\int_0^T \left[\min\left(\frac{V_{\rm IN}-V_{\rm P}}{V_{\rm in}}+\cos\left(\omega_0 t\right),0\right)-F_1\left(\frac{V_{\rm IN}-V_{\rm P}}{V_{\rm in}}\right)\right]^2\mathrm{d}t \\ &= V_{\rm in}^2F_2\left(\frac{V_{\rm IN}-V_{\rm P}}{V_{\rm in}}\right) \end{aligned} \tag{46}$$

where

$$F_2(x)=\int_0^1 \left[\min\left(x+\cos\left(2\pi y\right),0\right)-F_1(x)\right]^2\mathrm{d}y \tag{47}$$

can be expressed as

$$F_2(x)=\begin{cases} \frac{1}{2} & x<-1 \\ \frac{x^2-1}{\pi^2}-\frac{3}{2\pi}x\sqrt{1-x^2}+\arccos(x)\left[\frac{2x\sqrt{1-x^2}+x^2\arcsin x}{\pi^2}+\frac{1+x^2}{2\pi}\right] & -1\le x\le 1. \\ 0 & x>1 \end{cases} \tag{48}$$

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List of Figures

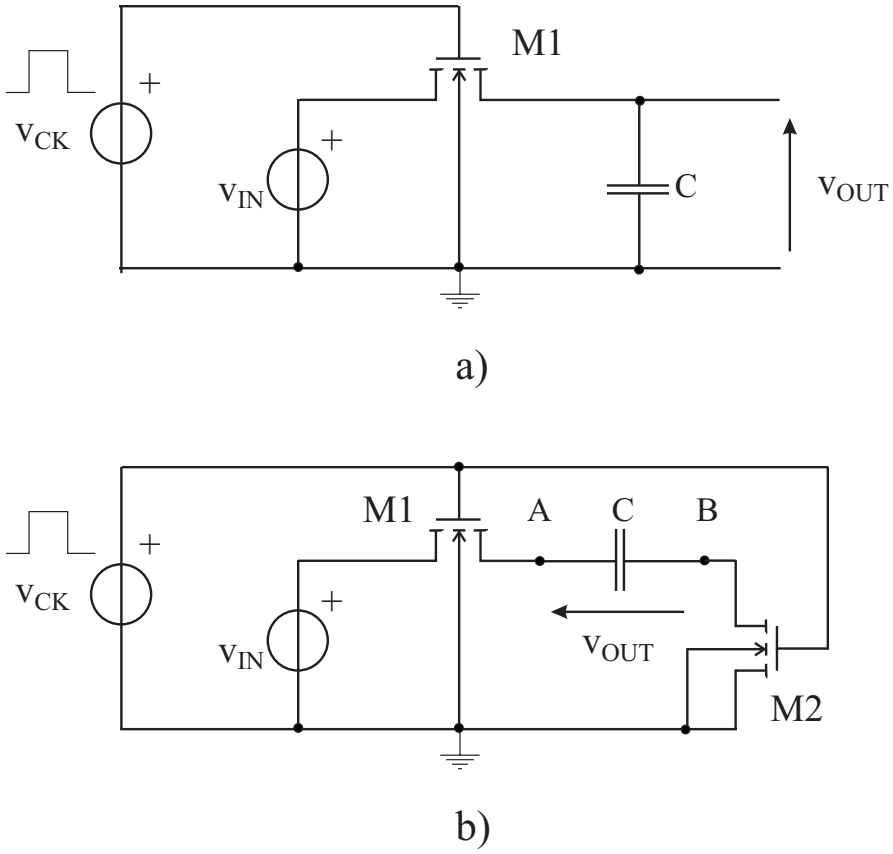

Fig. 1. Basic SC circuit configurations.

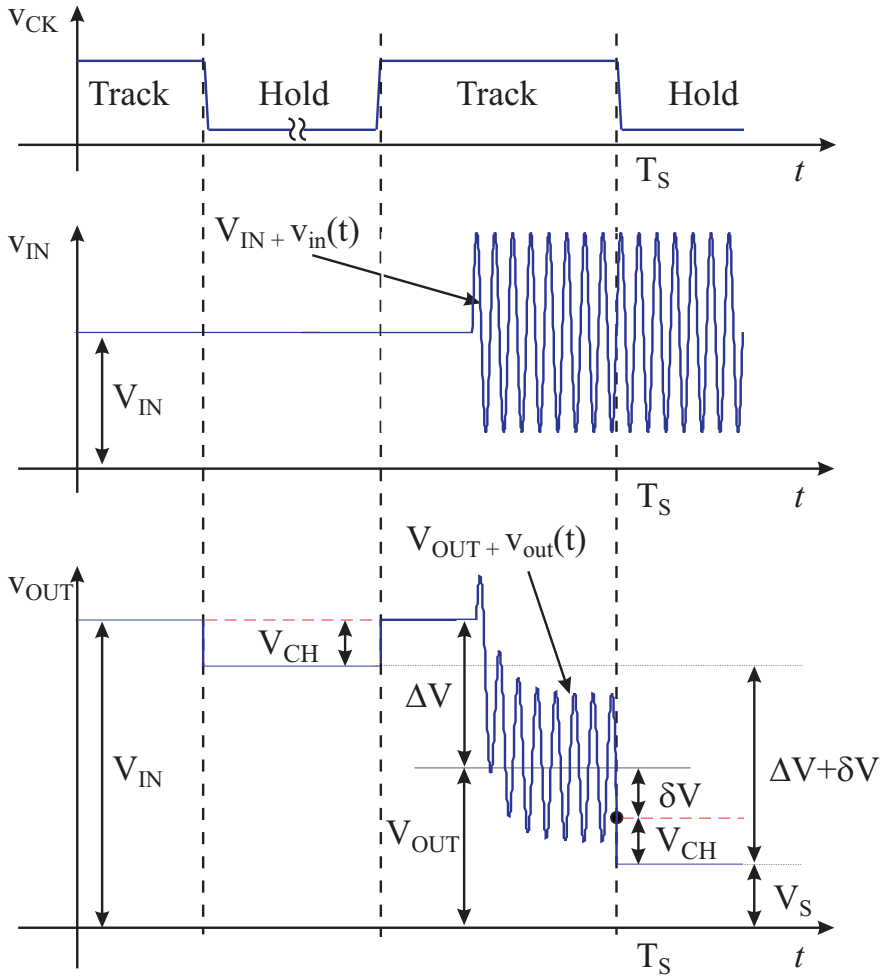

Fig. 2. Typical SC waveforms in the presence of RFI.

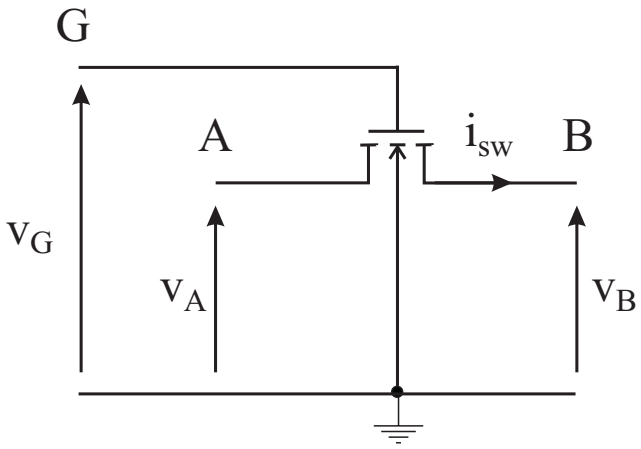

Fig. 3. Bulk-Referred MOS transistor Voltages.

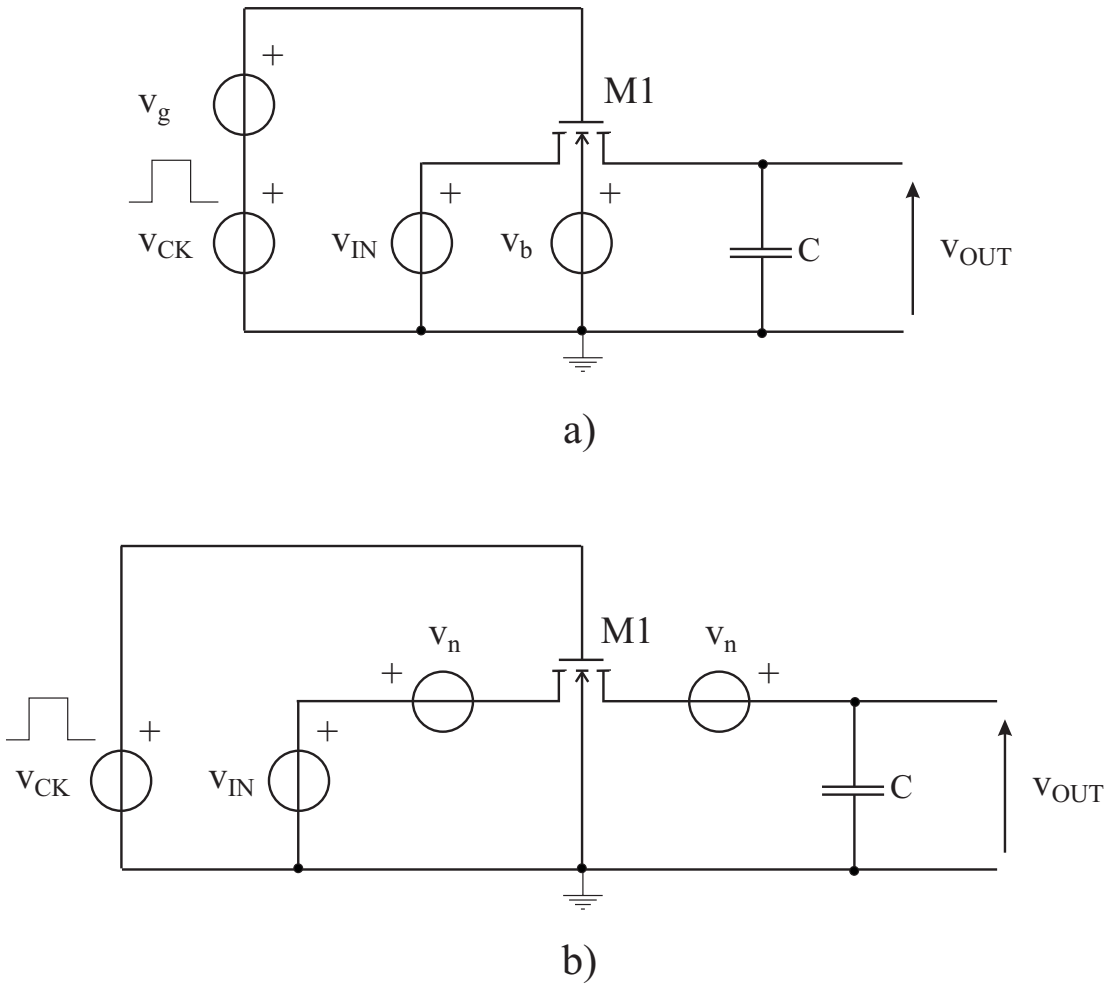

Fig. 4. Equivalent circuits for the prediction of the effects of RFI superimposed onto the gate and onto the substrate voltage.

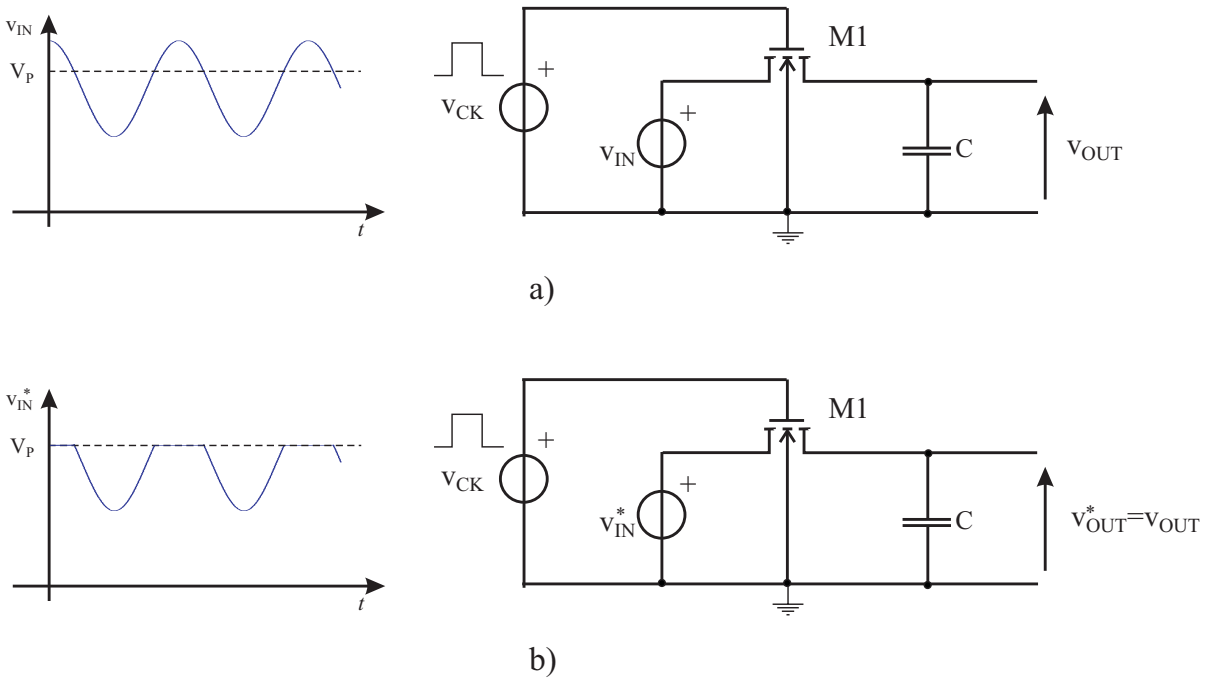

Fig. 5. Equivalent circuit for the prediction of the effects of RFI with arbitrary amplitude.

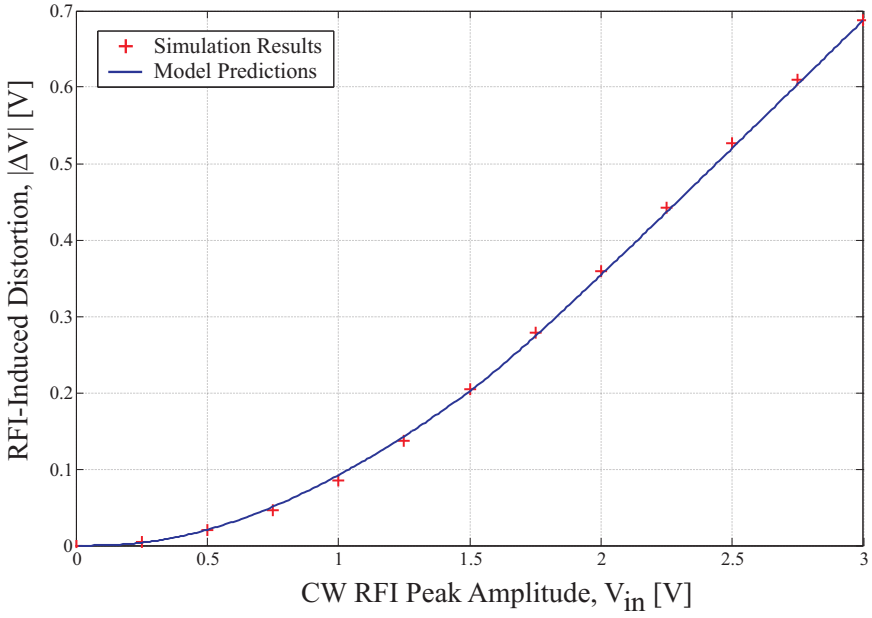

Fig. 6. RFI-Induced Offset Voltage ΔV Vs. CW RFI Peak Amplitude V_{in} for a CW RFI frequency f=100MHz, a switch aspect ratio $\frac{W}{L} = \frac{10\mu\text{m}}{2\mu\text{m}}$, a hold capacitance C=1pF and a DC input voltage V_{IN}=2V.

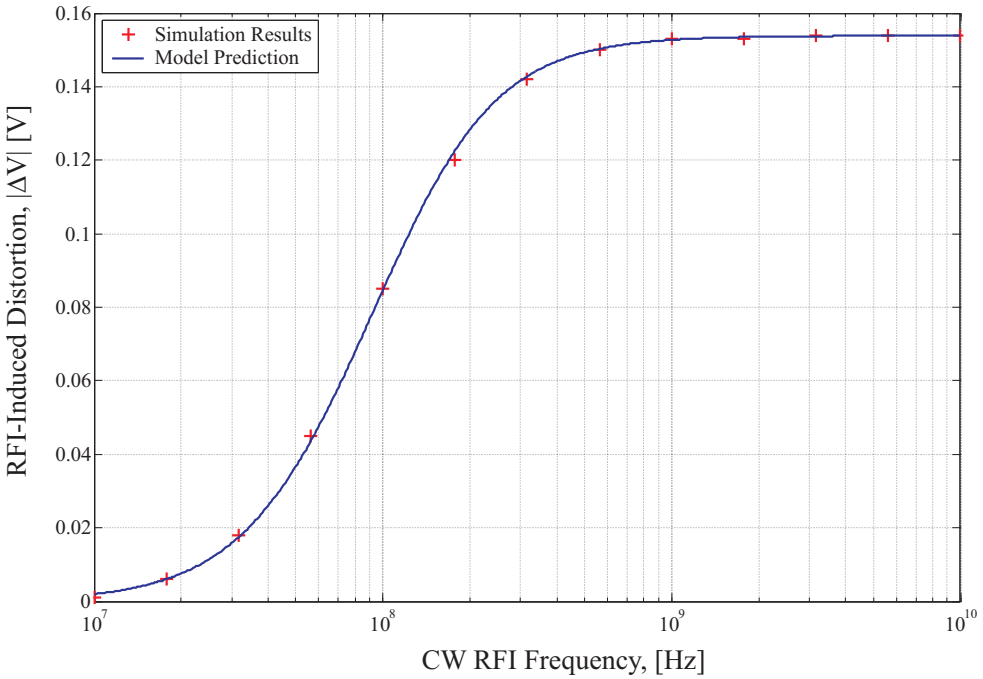

Fig. 7. RFI-Induced Offset Voltage ΔV Vs. CW RFI Frequency for a CW RFI peak amplitude $V_{\text{in}} = 1\text{V}$, a switch aspect ratio $\frac{W}{L} = \frac{10\mu\text{m}}{2\mu\text{m}}$, a hold capacitance C=1pF and a DC input voltage V_{IN}=2V.

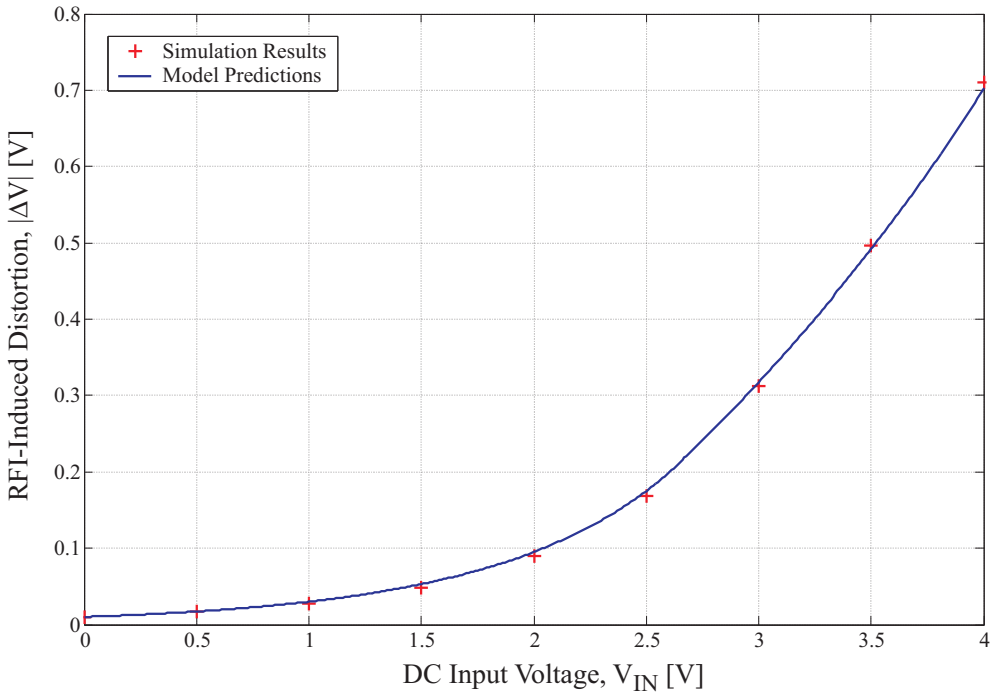

Fig. 8. RFI-Induced Offset Voltage ΔV Vs. DC Input Voltage $V_{\rm IN}$ for a CW RFI peak amplitude $V_{\rm in} = 1$V, a CW RFI frequency f=100MHz, a switch aspect ratio $\frac{W}{L} = \frac{10\mu{\rm m}}{2\mu{\rm m}}$ and a hold capacitance C=1pF.

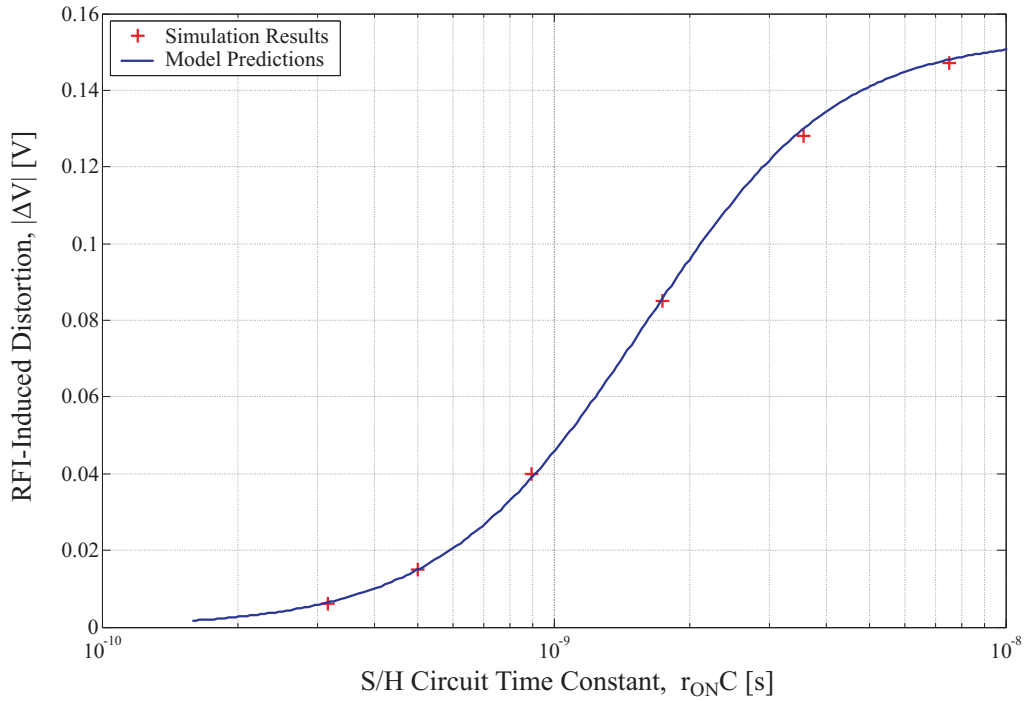

Fig. 9. RFI-Induced Offset Voltage ΔV Vs. SC Circuit Time Constant $\tau = r_{\mathrm{ON}}C$, for a CW RFI Frequency for a CW RFI peak amplitude $V_{\mathrm{in}} = 1\mathrm{V}$, a switch aspect ratio $\frac{W}{L} = \frac{10\mu\mathrm{m}}{2\mu\mathrm{m}}$ and a DC input voltage V_{IN}=2V.

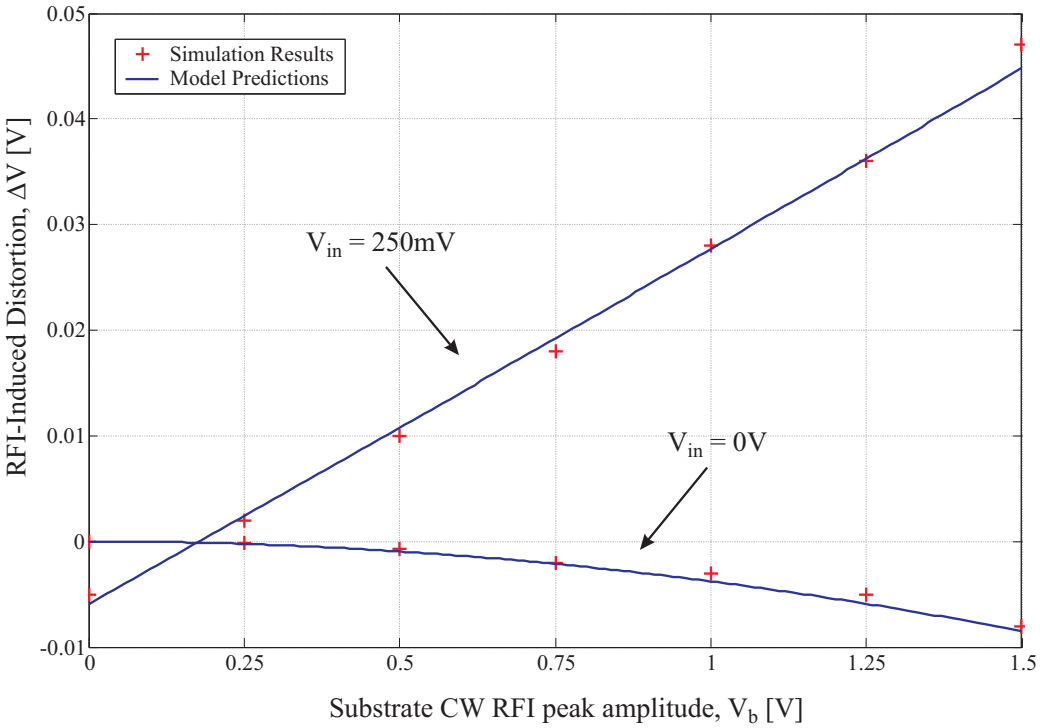

Fig. 10. RFI-Induced Offset Voltage ΔV Vs. Peak Amplitude of CW RFI superimposed onto the substrate voltage.

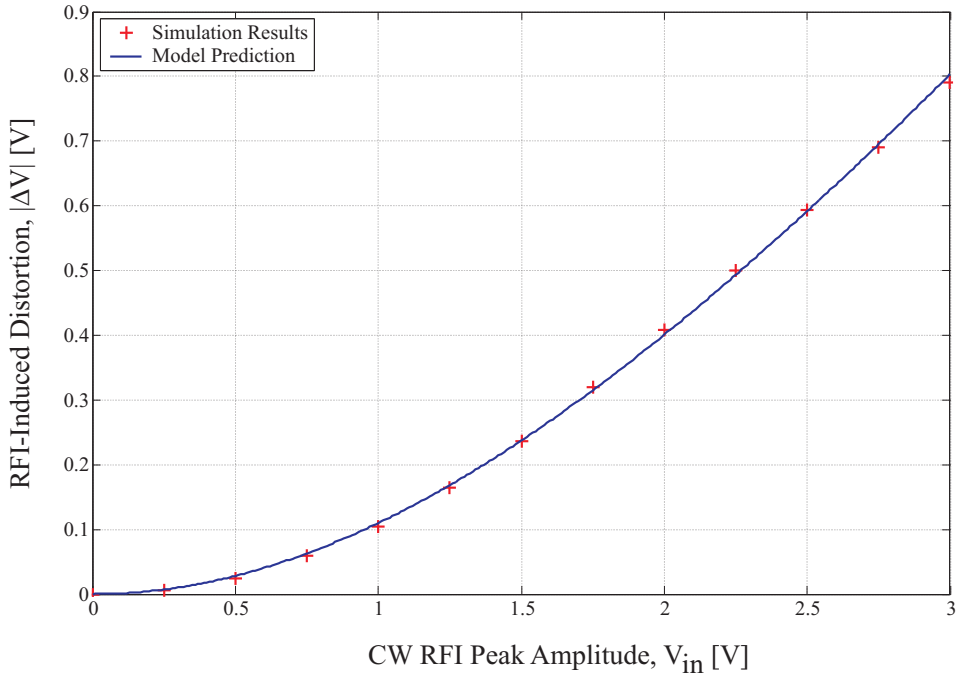

Fig. 11. RFI-Induced Offset Voltage ΔV Vs. CW RFI Peak Amplitude V_{in} in the Two-Switch SC circuit, for a CW RFI frequency f=100MHz, a switch aspect ratio $\frac{W}{L} = \frac{10\mu\text{m}}{2\mu\text{m}}$, a hold capacitance C=1pF and a DC input voltage V_{IN}=2V.

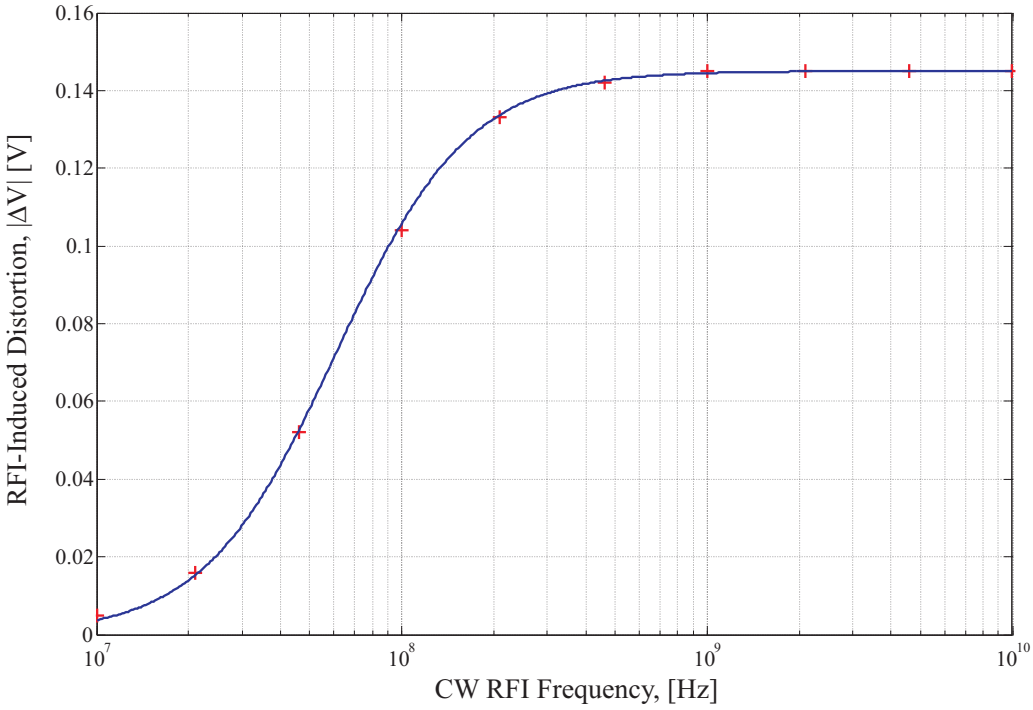

Fig. 12. RFI-Induced Offset Voltage ΔV Vs. CW RFI Frequency in the Two-Switch SC circuit, for a CW RFI peak amplitude $V_{\text{in}} = 1\text{V}$, a switch aspect ratio $\frac{W}{L} = \frac{10\mu\text{m}}{2\mu\text{m}}$, a hold capacitance C=1pF and a DC input voltage V_{IN}=2V.

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TABLE I
SC Circuit Parameters for Simulations

Parameter	Symbol	Default Value
Switch Aspect Ratio	W/L	$\frac{10\mu\text{m}}{2\mu\text{m}}$
Bulk-Referred Gate Voltage	V_{G}	5V
Hold Capacitor	C	1 pF
DC Input Voltage	V_{IN}	2V
Input CW RFI Peak Amplitude	V_{in}	1V
Substrate CW RFI Peak Amplitude	V_{b}	0V
Phase shift between substrate and input CW RFI	φ	0°
CW RFI Frequency	f	100 MHz