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Influence of Parasitic Capacitance Variations on 65 nm and 32 nm Predictive Technology Model SRAM Core-Cells

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Abstract

The continuos improving of CMOS technology allows the realization of digital circuits and in particular Static Random Access Memories that, compared with previous technologies, contain an impressive number of transistors. The use of new production processes introduces a set of parasitic effects that gain more and more importance with the scaling down of the technology. In particular, even small variations of parasitic capacitances in CMOS devices are expected to become an additional source of fective behaviors in future technologies. This paper analyzes and compares the effect of parasitic capacitance variations in a SRAM memory circuit realized with 65 nm and 32 nm predictive technology models.

1. Introduction

Semiconductor memories are the predominant majority of semiconductor devices production. The Semiconductor Industry Association (SIA) forecasts that in the next 15 years up to 95% of the entire chip area will be used to create memory blocks. Memories will therefore represent one of the most critical elements to guarantee the success of next generation digital devices [1].

Memories have been used for a long time to push the state-of-the-art in the semiconductor industry. While new technologies allow a significant improvement in terms of performance and capacity, the continuous scaling and the high integration density make memories highly sensitive to physical defects and process variations. Precise fault modeling and efficient test design are therefore mandatory to guarantee high quality products.

Memory testing is historically based on the definition of Functional Fault Models (FFM) together with very efficient test algorithms such as march tests [2]. Functional fault models are independent of the specific memory technology and allow the definition of test sequences not tight to a specific architecture. Several publications propose an extensive set of memory fault models together with the corresponding march tests for their detection. Classical fault models include static faults, i.e., faults that require a single memory operation to be sensitized [3], [4], [5], [6], [7] as well as more complex dynamic faults, i.e., faults that require more than one memory operation to be sensitized [5], [8]. Dynamic faults are one of the main manifestations of the negative effects Very Deep Sub Micron (VDSM) technologies have on memory devices. Their complexity strongly reduces the efficiency of traditional test algorithms requiring complex at-speed test sequences to be detected.

Recent publications analyzing the effect of VDSM technologies on memory devices, mainly focused on studying the effect of resistive defects in static random access memories by injecting these defects into an electrical model of the memory, and by performing electrical simulations [9], [10], [11], [12], [13], [14], [15], [16], [6]. Nevertheless, recent works also show that, as the device size is down-scaled into nanometer range, the transistor characteristics are liable to various changes due to shift of underlying device physics and in particular new parasitic capacitances become increasingly serious [17], [18], [19].

This paper analyzes the influence of parasitic capacitance variations on 6-transistors SRAM memory cells implemented using VDSM technologies. In particular, the paper proposes a comparative analysis among two memory technologies with feature sizes of $65\,\mathrm{nm}$ and $32\,\mathrm{nm}$ respectively. The analysis is performed by considering different defect locations, and defect sizes. The fault analysis is based on a set of SPICE simulations of a defective memory model with the support

of an automatic fault model extraction algorithm for an efficient exploration of the space of possible faulty behaviors. Experimental results show that capacitive defects may introduce dynamic faulty behaviors that need to be considered and tested in future memory devices.

The paper is organized as follows: Section 2 details the main characteristics of the proposed experimental design while Section 3 proposes a preliminary defect analysis on the memory behavior in terms of identified faulty behaviors and relationship with the technology process used to build the memory. Finally Section 4 summarizes the main contributions of the work and concludes the paper.

2. Experimental design

This section introduces the characteristics of the proposed experimental design.

The core of the experiment is a set of electrical simulations performed on a SPICE model of a Static Random Access Memory (SRAM) block. Our reference architecture includes a cell array organized as a 512x512 matrix including, the pre-charge circuits for bit and word lines, the sense amplifier, the write circuitry, and the address decoder. In order to keep the simulation time into a reasonable level, due to the amount of required simulations, we considered a simplified memory architecture including a limited number of memory cells.

Figure 1 shows the architecture of a core memory cell realized with a standard 6-transistors structure. Figure 1 also includes a set of five candidate defect locations considered during the fault analysis. The proposed analysis is limited to single defects only, not considering the effect of multiple defects.

The set of proposed defects does not include all possible locations. The number of candidate locations has been reduced by considering the internal circuit symmetry. In particular, we considered the right part of the circuit for defects DFC_1 and DFC_2, the left part of the circuit for defect DFC_5, while defects DFC_3 and DFC_4 are not asymmetric.

The defects introduced in Figure 1 try to model a set of physical parasitic effects gaining importance with technology down scaling. Crystallographic defects in the interface between the oxide layer and the substrate of a mosfet transistor may produce an electron trap effect that acts as a capacitance, which can be modeled as an alteration of the capacitive load of the transistor. This effect leads to an alteration of the capacitive load of the CMOS inverter in the self refreshment loop of the memory cell (see Figure 1) identified

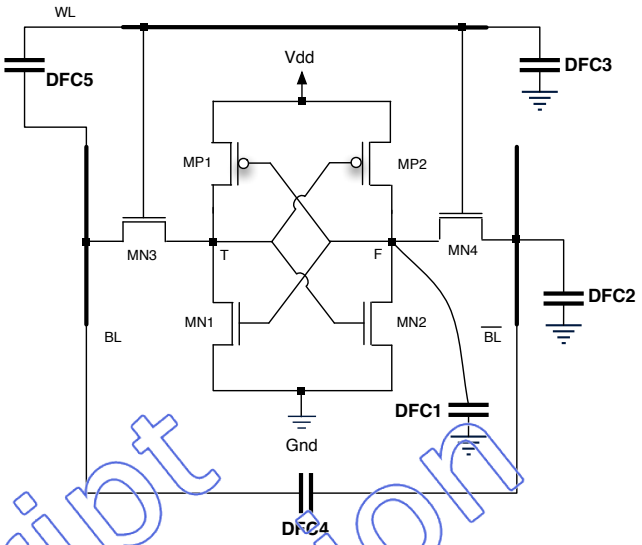

Figure 1. 6-transistors memory cell with candidate defects

by DFC_1. The capacitive parasitic effects due to the metallization-substrate coupling and the capacitive coupling between two lines are also additional sources of defects. They are modeled by defects DFC_2, DFC_3, DFC_4, and DFC_5.

This paper analyzes and compares the effect of the proposed list of defects on SRAMs considering two different technologies from Predictive Technology Model [20], with transistor feature size of $65\,\mathrm{nm}$ and $32\,\mathrm{nm}$ respectively. To allow a correct comparison, all experiments have been performed in similar working conditions, i.e., same operational temperature $27^\circ\,\mathrm{C}$, process type *typical*, and timing with a clock period of $1.5\,\mathrm{ns}$ ($666\mathrm{MHz}$ clock frequency). The only different parameter passing from one technology to the other one is the supply voltage that requires to be scaled to adapt the memory behavior to the specific technology. Table 1 summarizes the main parameters applied during simulations.

We considered defect values in the range of a few fF to hundreds of fF in order to extensively analyze the memory behavior and to obtain a clear view of the observed phenomena.

All the experiments have been conducted by running electrical simulations using HSPICE. In particular the main goal of the analysis is the identification of dynamic faulty behaviors caused by the insertion of the proposed defects.

From preliminary analyses and simulations, and looking at the results of previous studies on the effect of resistive defects in static random access memories [16] we observed that in many situations dynamic

Table 1. Experimental conditions

	65 nm technology	32 nm technology
Process corner	Typical	Typical
Supply voltage	1.1 V	0.9 V
Temperature	27° C	27° C
Timing	1.5 ns	1.5 ns
Mode	Active	Active

faults are generated in very specific conditions usually identified by a specific value (or a very thin interval of values) of the target defect representing a cut point between the fault free domain and the static faults domain. The experimental approach used during our analysis mainly focuses on the identification of this cut point, if present.

For each defect, to reduce the number of simulations to perform, we applied a binary search procedure. The analysis starts with two defect values, one big enough to generate a static faulty behavior, while the second one small enough to be not influent on the memory behavior. These two values represent the starting search space for the analysis.

With this initial range, we split the interval in two parts and we simulate the middle point analyzing the effect on the memory. We can find three situations:

- The middle point identifies a dynamic behavior. In this case we reached the cut point and the search is concluded;
- The middle point falls in the no fault domain. In this case we need to restrict the search space to the upper half of the initial range;
- The middle point falls in the static faults domain. In this case we need to restrict the search to the lower half of the initial range.

This procedure is repeated until either we find the cut point (i.e., we identify a dynamic behavior) or we reach a sharp transition from the no fault domain to the static faults domain (i.e., the defect do not lead to a dynamic fault). Obviously once the cut point is identified, additional simulations around its value are performed to precisely characterize the behavior of the memory in this defect area.

Concerning the test sequences applied during the analysis, since we mainly focus on the identification of dynamic faulty behaviors in the memory, we look for activation sequences longer than one operation. Possibly, two, three or more operations should be analyzed. In this context exploring all possible activation sequences is unfeasible due to the extended search space and simulation time. We thus resorted to an automation algorithm able to efficiently target those sequences that most likely lead to faulty behaviors. This algorithm actually analyzes the simulation results of a good memory model and a faulty memory model and based on this comparison, and applying opportune heuristics, generates test sequences to simulate.

This automatic simulation approach allows us to explore a wider set of test sequences thus increasing the meaningfulness of the proposed analysis.

3. Fault Analysis

This section analyzes the results obtained during the experiments proposed in Section 2.

Table 2 and Table 3 summarize the results obtained observing the simulations. For each table the first column reports the target defect, the second column the technology used to build the SRAM circuit, the third column the minimum defect value able to introduce the corresponding faulty behavior, while the last column shows the faulty behavior expressed in terms either of fault primitives or fault models.

All the identified faulty behaviors belong to the following functional faults categories:

- **Transition Faults (TFs):** a memory cell fails to perform an up transition ($0 \rightarrow 1$) or a down transition ($1 \rightarrow 0$) after a write operation;
- **Incorrect Read Fault (IRF):** a cell stores a correct logic value but the output read circuitry returns an incorrect value after a read operation;
- **dynamic Transition Fault (dTF):** a cell is unable to perform an up/down transition after a write operation which immediately follows another operation on the same cell (i.e., read or write operation).

Moreover, by observing the results of Table 2 we had the confirmation that for this technology the range of values that lead to dynamic faulty behaviors is actually reduced to a single cut point.

Figure 4 summarizes the sensitivity of the memory to the target defects based on the technology. It shows, for each defect, the minimum value required to introduce a faulty behavior.

As expected 32 nm technology is more sensitive to parasitic capacitance variations. In general, with 32 nm technology, faulty behaviors arise with a smaller defect value w.r.t. 65 nm technology. The only exception concerns DFC_4. For this defect 65 nm technology becomes more sensitive even if the experimental data show that the faulty behavior emerge only for a defect size of the order of a hundred fF.

This behavior is connected with the reduced ability of the 65 nm memory to work at high frequencies, and to the relative bigger size of the 65 nm cell w.r.t. the

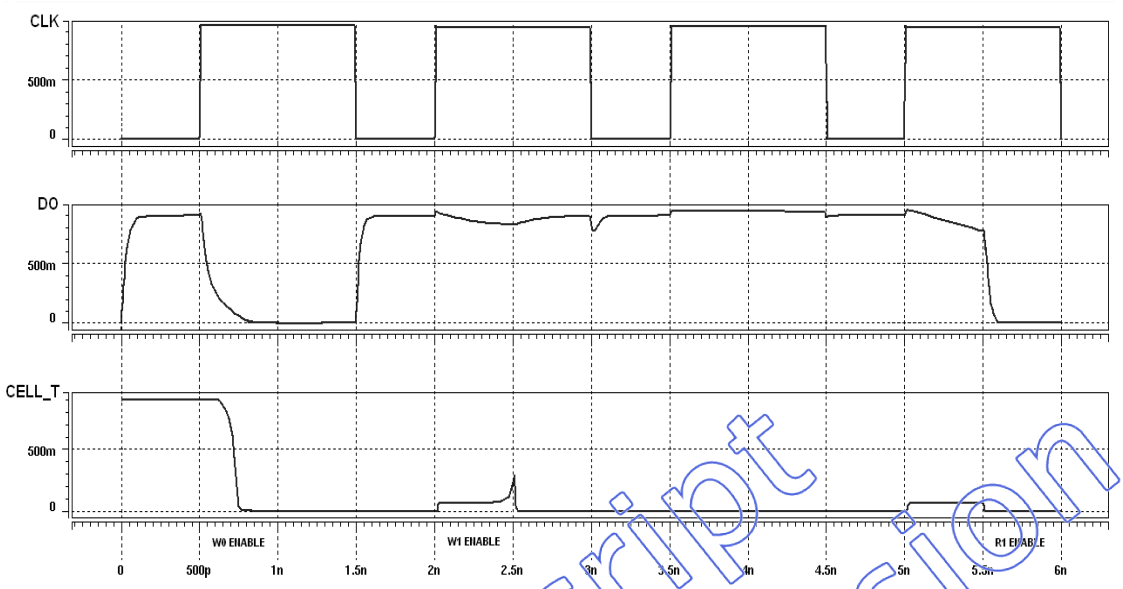

Figure 2. Dynamic faulty behavior for DFC2 in the 32 nm technology based memory

32 nm one. Moreover we have to remark that each technology uses a different supply voltage that may contribute to this result.

Table 2. Dynamic fault behaviors

#DFC	Technology	Min. defect size	Fault primitive
DFC_1	65 nm	14.20 fF	$\langle 1w_0w_1 \,/\, 0 \,/ - \rangle$
	32 nm	-	-
DFC_2	65 nm	-	-
	32 nm	68.40 fF	$\langle 1w_0w_1 \,/\, 0 \,/ - \rangle$
DFC_3	65 nm	-	-
	32 nm	-	-
DFC_4	65 nm	252.00 fF	$\langle 0 \text{ Any } w_1 \,/\, 0 \,/ - \rangle$
	32 nm	274.00 fF	$\langle 0 \text{ Any } w_1 \,/\, 0 \,/ - \rangle$
DFC_5	65 nm	21.68 fF	$\langle 1 \text{ Any } w_0 \,/\, 1 \,/ - \rangle$
	32 nm	-	-

Looking into more details at the causes of the different faulty behaviors, DFC_1 introduces a transition fault in the cell. The capacitive parasitic effect introduces a delay in the propagation of the signal from the output of the inverter 2 (i.e., the inverter composed of MN2 and MP2 transistors) and the input of inverter 1 (i.e., the inverter composed of MN1 and MP1 transistors). The inverter 1 does not have enough time to reach the correct threshold for the cell switching. Depending on the technology, the defect may lead to a simple static fault or to a more complex dynamic faulty behavior.

Table 3. Static faulty behaviors

#DFC	Technology	Min. defect size	Fault type
DFC_1	65 nm	14.21 fF	TF
	32 nm	9.30 fF	TF
DFC_2	65 nm	134.34 fF	TF
	32 nm	68.41 fF	TF
DFC_3	65 nm	42.08 fF	TF
	32 nm	25.93 fF	TF
DFC_4	65 nm	252.10 fF	TF
	32 nm	274.10 fF	TF
DFC_5	65 nm	21.69 fF	TF
	32 nm	10.70 fF	IRF

DFC_2 introduces an alteration of the parasitic capacitance associated to the metallization of $\overline{BL}$. This type of alteration induces an extra amount of charges in the bit line capacitance which is not completely discharged during the fault sensitizing operations (see Figure 2). This defect leads to a dynamic faulty behavior in the 32 nm cell, while in 65 nm memory the behavior is static.

Defect DFC_3 is connected to a capacitive coupling between the polysilicon word line and the substrate of the cell that produces a delay in the word line activation signals (i.e. MN3 and MN4). This defect always leads to a static fault both in 32 nm and 65 nm technology.

Finally DFC_4 and DFC_5 are coupling effects be-

tween the two bit lines, and between the bit line *BL* and the word line *WL*, respectively. It is interesting to note that in both cases the faulty behavior can be ascribed to the crosstalk effect between the two involved lines. In particular in case of DFC_5 there is a signal transfer between the word line and the bit line, even if the cell continues to store the correct logic value.

One interesting phenomena we observed during our experiments is that, by repeating the same experiments several times, we obtained small variations in the simulations results (especially when working with $32\,\mathrm{nm}$ technology). Figure 3 shows an example of this situation. The $32\,\mathrm{nm}$ based core cell continues to store the correct value even if the output signal shows two different behaviors. In the first case (i.e., the dark line), the output signal tries to drop down but after $0.2\,\mathrm{ns}$ it is forced again to an high value, while in the second case (i.e., the red line) the output signal reaches the $0\,\mathrm{V}$ value after $0.31\,\mathrm{ns}$. This confirms the high sensitivity to this type of defects.

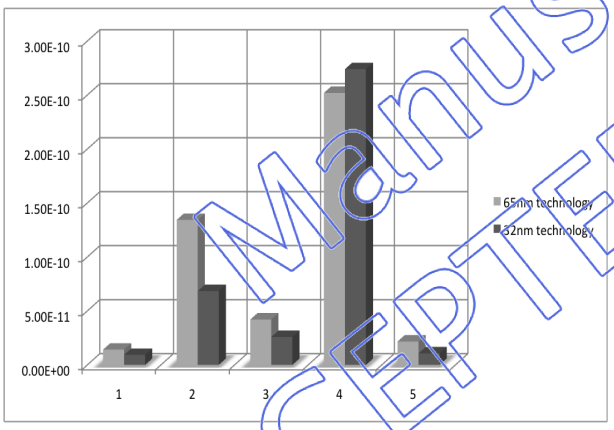

Figure 4. Graphic expression of the minimal capacitive value that produce a fault behavior

4. Conclusion

This paper proposed a preliminary analysis on the influence of parasitic capacitance variations on 6-transistors SRAM memory cells implemented using VDSM technologies. In particular, the paper proposes a comparative analysis among two memory technologies with feature sizes of $65\,\mathrm{nm}$ and $32\,\mathrm{nm}$ respectively. The analysis is performed by considering different defect locations, and defect sizes.

The experimental results show that for some defect locations the technology downscaling increases the probability of faulty behaviors connected to these physical defects. Moreover for some conditions these faulty behaviors can be classified as dynamic faults, thus requiring more complex test sequences to be detected.

A more complete and extensive analysis of the effects of these defects on different memory architecture is under development to better understand the test requirements of future memory technologies.

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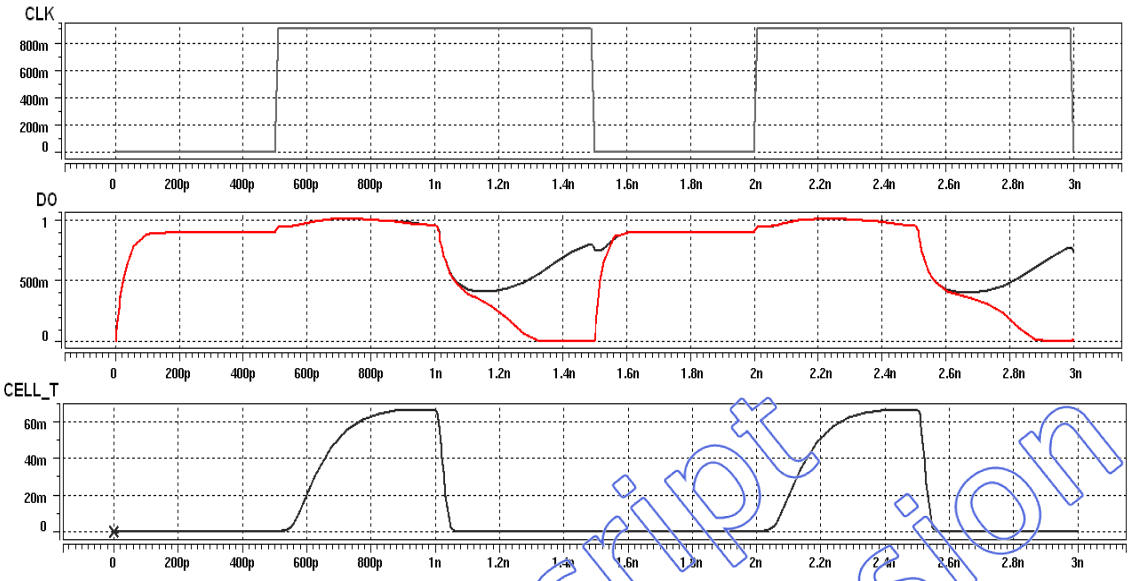

Figure 3. Simulation of the output signal in the 32 nm core cell based with the DFC_5 with two different behaviors

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