MOCHA, MOdelling and CHAracterization for SiP - Signal and Power Integrity Analysis

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Abstract

This paper describes the research activity that is being carried out in the MOCHA project, a cooperative R&D effort at the European scale. The aim of the project is to develop reliable modelling and simulation solutions for SiP design verification.

Introduction

In the last years, the complexity, speed, and packaging density of electronic systems have grown so fast that they created a completely new design scenario. In order to illustrate these issues, it is useful to consider the evolution of portable devices as an example. These consumer goods are integrating an increasing number of sophisticate and heterogeneous functions, such as GPS, video cameras and MP3. This evolution is driving the development of new 3D packages holding and connecting the subsystems for the digital and radiofrequency parts, new miniaturized ultra wideband interconnect and very large capacity memory modules. This application is evolving toward a System-in-Package (SiP) or a System-on-Package (SoP) configuration (See Fig.1) and is causing a revolution in the capabilities of electronic systems, as well as in the design needs.

The key features of this revolution are the increase of system complexity, the development of new dense 3D packaging structures and the increase of signalling rates. Complexity means that designers have to take a system simulation approach, in order to assure that the individual subsystems work properly and interact with each other as expected. Dense 3D packaging structures imply a package centric design approach. Till recently, package structures were simply providing the link between the integrated circuit (IC) and board domains, where designs were carried out independently. In the new scenario, the package strictly relates chips and boards, influencing the overall system operation. Faster signalling creates a bundle of new modelling problems, because it introduces new devices and increases the impact of parasitic effects on existing components.

Within this scenario it is strategic to analyze and detect potential signal and power integrity failures before the prototype phase. The key to success is a set of integrated EDA tools and modelling flows that combine the availability of accurate models with fast and reliable time-domain and system-level verification simulation methodologies. Current EDA tools hardly address these issues, as there is a large gap between the IC tools and the layout tools for packages and boards.

The aim of this project is to develop reliable modeling and simulation solutions for SiP design and verification through measurement analysis, thus validating the simulation results and making available characterization measurement platforms. At the end of the project it is expected that the flows for extracting accurate simulation models will be available, together with a performing integrated EDA platform and a viable signal integrity measurement methodology. The final targets of project include:

- a demonstration of the innovative IC simulation models developed and their related extraction flows by both simulation and measurement;
- the development of an innovative 3D EM field solver;
- the development of a performing SiP design and verification EDA platform;
- a demonstration of the developed signal integrity measurement techniques.

The current modeling solutions and EDA tools used for SiP design and verification have been derived from the board applications, as natural evolution due to the fact that a SiP is a sort of small board. Nevertheless, some technological differences, like SiP's 3D structures (wire bonds, solder balls, die bumps) and non-ideal reference planes, make useless or not accurate the classical IC buffers models and 2D interconnection models valid for board design and verification. As a result, the MOCHA research activity addresses the technical challenges covering all the issues from simulation models development (for IC buffers and power supply networks and for 3D physical structures) to SiP power and signal integrity verification methodologies by both simulation and measurement approaches.

Description of the Work

The MOCHA project work plan is organized into four major work packages (WP), which logically define the different fields that have to be addressed in order to achieve the expected technical goals. The WP sequence has been defined in such a way that the different activities are initially developed separately, interact with each other where needed, and are later merged together for the implementation of reliable simulation and measurement design verification platforms. A brief description of the work packages follows:

- IC power integrity model: Main objective is the identification of a suitable measurement methodology for modelling IC power supply distribution networks, overcoming the current limit of EDA tools to extract a reliable wide-frequency-range model. To this aim, both electromagnetic (EM) simulations and

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measurements will be carried out, allowing to generate accurate models that can be effectively used to study the trade-off between power rails topology, buffers configuration, pads distribution and accuracy [1].

- IC buffers' innovative modelling approach: Main objective is to explore an innovative approach for parametric modelling of IC buffers, which may be suitable for both simulation and measurement characterization. To this aim, a benchmarking between measurements and simulations will be continuously carried out to accomplish the target [2,3,4,5].
- SiP design and verification EDA platform: Main objective is the development of an EDA platform for carrying out reliable signal and power integrity analysis in the context of SiP design and verification, to enable a reduction of the overall design/manufacturing cycle. A new 3D EM field solver for 3D physical structures characterization will also be developed along with an interface that enables the interfacing between the 3D EM field solver and the EDA Platform [6].
- SiP signal integrity measurement platform: Main objective is to identify a viable technique for SiP signal integrity measurements, in order to observe and analyze the electrical behavior of internal package signals when SiP is working on a real application board. Within this work package, RF measurements will also be carried out for validating the simulation results of the 3D EM field solver [7,8].

Acknowledgments

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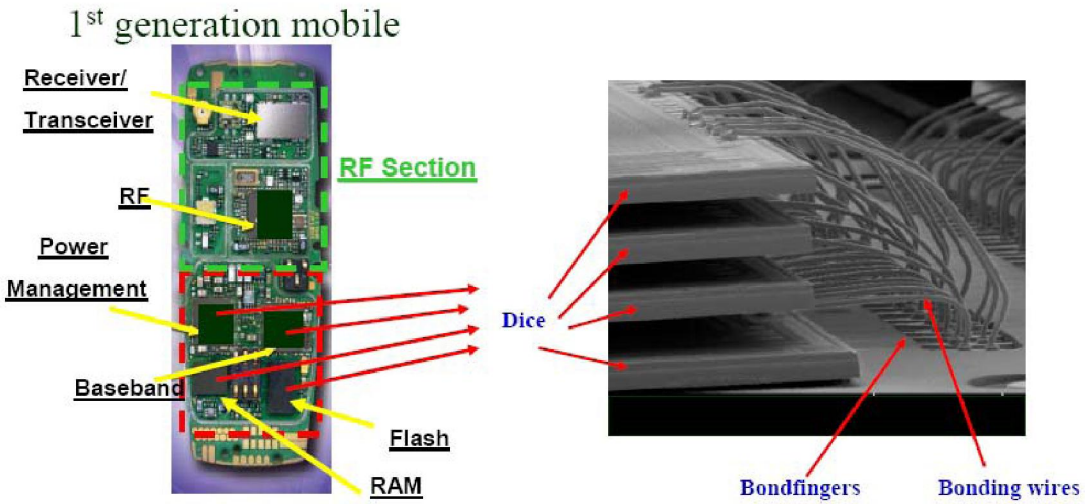

Fig. 1. The left panel shows a cellphone with the most relevant blocks as the ICs placed on the board. The right panel shows an example of the System-in-Package integration that allows the inclusion of four devices within the same package.