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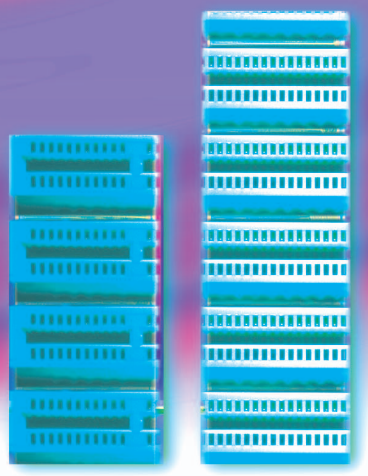
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15 November 2026

Multiport VNA Measurements

Thomas G. Ruttan, Brett Grossman, Andrea Ferrero, Valeria Teppati, and Jon Martens



It would have been difficult to predict, even 15–20 years ago, that microwave design and the personal computer (PC) would be as closely linked as they are today. In those days, PC manufacturers were excitedly claiming clock speeds of 16–33 MHz, while the microwave designer was routinely applying well-known design skills to problems into millimeter-wave frequencies. The proliferation of PC applications and Internet use in our everyday lives, along with complementary metal-oxide semiconductor (CMOS) technology keeping pace with Moore's law, have resulted in today's PC system having clock frequencies well into the GHz range and channel data rates measured in Gb/s.

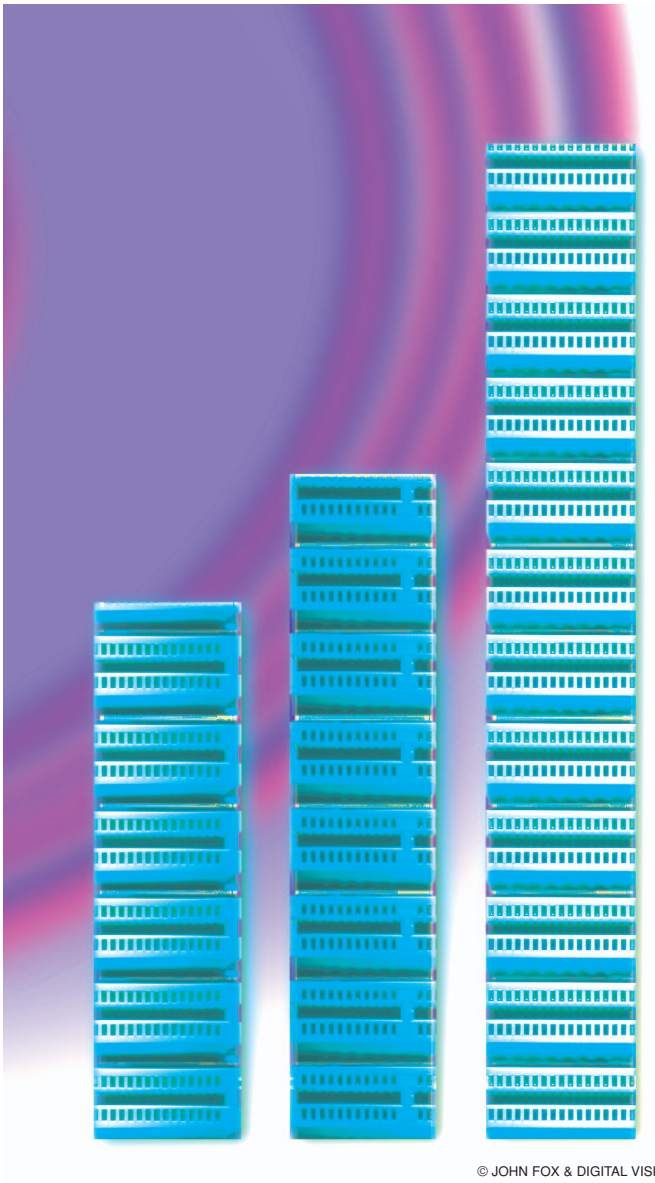
Keeping pace with these frequencies in the typical digital system presents significant design challenges. Preserving the signal integrity of a single, broadband signal through the packages, sockets, connectors, and PC board (PCB) traces typically found in today's computer systems, the system designer now borrows many tools from the microwave designer. However, to achieve the overall bandwidth required, the system architecture consists of tens to hundreds of parallel channels operating at these high data rates. This is not the typical challenge of the microwave designer! Power integrity—where the dc power is delivered cleanly to the CPU and other semiconductor devices—is also an important topic for the digital designer. Power integrity can have a significant impact on signal integrity due to ground bounce, bias ringing, and other effects, but we will save that discussion for another time.

A key element in the design process of these systems, whether it is to validate simulation models or to verify performance, is the ability to measure the performance of these systems at the operating frequency of interest. For

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this, the digital engineer again reaches into the microwave engineer's toolbox, and this time pulls out the vector network analyzer (VNA). Though the typical microwave engineer's VNA, with only two ports, doesn't lend itself to easily characterizing the groups of parallel signal channels the digital engineer faces, it can do so by making it a multiport instrument.

This article presents some of the most recent multiport VNA measurement methodologies used to characterize these high-speed digital networks for signal integrity. There will be a discussion of the trends and measurement challenges of high-speed digital systems, followed by a presentation of the multiport VNA measurement system details, calibration, and measurement techniques, as well as some examples of interconnect device measurements. The intent here is to present some general concepts and trends for multiport VNA measurements as applied to computer system board-level interconnect structures, and not to promote any particular brand or product.

Key Trends in High-Speed Digital Systems

In order to meet the challenges of the marketplace outlined above, the drivers for digital systems include achieving higher speeds, increasing the density of the signal channels, and moving to differential lines for the data bus. All three of these are primarily fulfilling the same objective—to increase the total system data bandwidth.

Figure 1 shows the industry's projected trends for maximum on-chip CPU operating frequency. It is very likely that all of the potential opportunity represented by this increasing chip performance will not be realized unless the system interconnect speeds also increase. Figure 2 illustrates how industry associations are proposing this will be implemented.

To meet this trend and support transmission data rates into the tens of Gb/s per channel will require minimal loss, reflection, and crosstalk well into the microwave frequency range of 5–20 GHz.

Signal density is increasing because of two factors—more signals and closer placement. In order to achieve the desired overall system bandwidths while keeping some control over the frequency of the signals, the number of signals in the typical system is growing. Figure 3 illustrates this with the trend to higher package pin count. While this metric includes pins used for both signal and power delivery, an estimate that 20–30% of these pins are dedicated to signal lines is not unreasonable. But in order to keep system physical dimensions from increasing at a similar rate, it is necessary that these signals be placed more closely together. More signals, placed closer together, leads to increasing density.

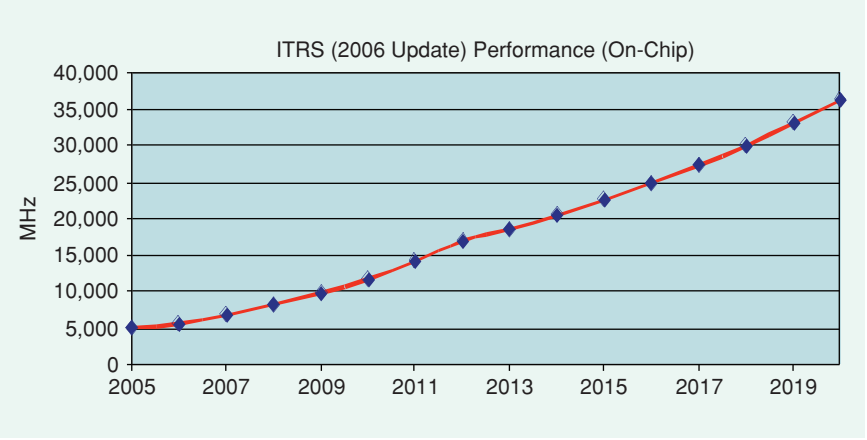


Figure 1. *Abstracted International Technology Roadmap for Semiconductors (ITRS) data for on-chip performance [1].*

Finally, the trend to differential lines for the signal path is also driven by the need for speed. Since the ground planes for typical board-level interconnect structures in computer systems have many routing clearance holes and plane discontinuities, it is difficult to create a well-defined reference ground plane for transmission lines. Differential (balanced) lines are used in many high-speed digital systems for board-level transmission lines. The reason for this is that differential lines will have improved high-frequency performance compared to single-ended (unbalanced) lines. To first order, this is due to the virtual ground between the pair of lines in a differential transmission line which reduces the requirement for a solid reference ground plane for acceptable high-frequency performance [3].

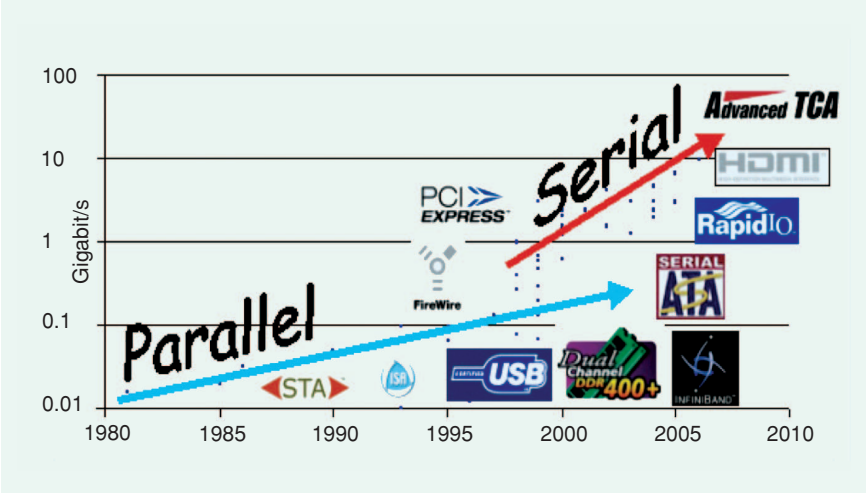


Figure 2. *Projected interface data rate trends [2].*

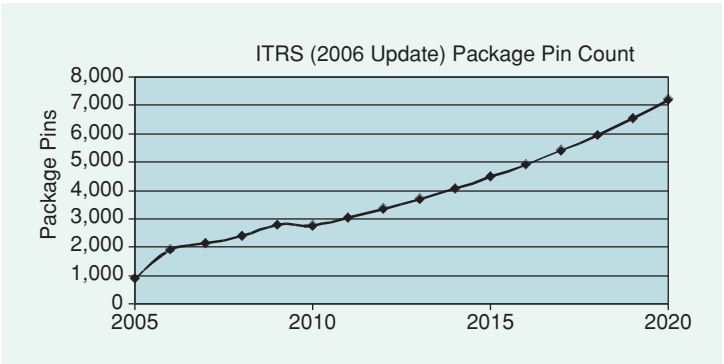


Figure 3. *Abstracted ITRS data on package pin count [1].*

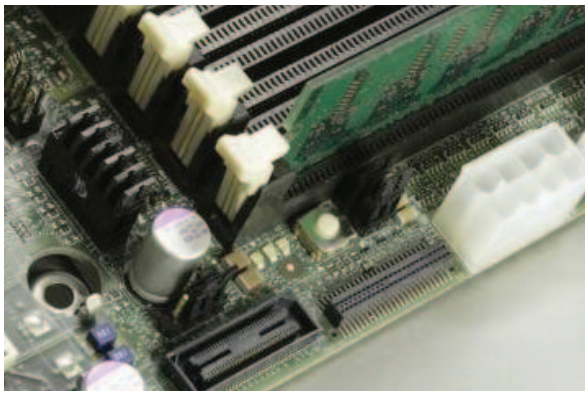


Figure 4. *Typical 3-D digital interconnect configuration.*

Challenges of Measuring Digital Interconnections in the Analog World

Since most of the digital interconnect structures are a combination of many parallel data lines and/or differential serial bus designs, the challenge of performing high-frequency measurements is quite different from the typical microwave device where there are only a few I/O lines to worry about. Additionally, PCBs are the circuit media of choice and will include both planar and three-dimensional (3-D) structures, as found in backplane server chassis and memory modules, illustrated in Figure 4.

So, the measurement problem is compounded by the need to connect many data lines, possibly in more than one plane, while making good, high-frequency connections from the PCB structures to the VNA instrumentation, which typically has coaxial test ports.

To provide a reliable test interface between the VNA and PCB test structures, the two choices are to either use coaxial to PCB launchers or probe directly to the PCB surface with microwave probes. Coaxial launchers are best suited to nonplanar, 3-D structures as shown in Figure 4, where probing on surfaces with more than one plane is difficult (though not impossible with proper probe station fixturing). Coaxial launches have the added advantage that the test ports for high I/O count devices can be physically spread out to ease the mechanical design of the test fixture at the expense of test board size. These coaxial launches need to be well designed and repeatable to provide a low-reflection, high-frequency transition if accurate calibration and measurement results are expected.

The use of microwave probes for the PCB test interface presents both an opportunity and a challenge. The opportunity lies in the fact that the probe launch interface will typically have an improved high-frequency transition to the board compared with coaxial launches. Thus, with a more electrically transparent test port transition, as well as a more repeatable connection, probing will generally provide improved calibration

and measurement accuracy. The challenge is that, for multiport devices, it is nearly impossible to fixture a probe station to mechanically place all the probes required if the traditional single-port probes are used. One solution is to use multiport probes on the same probe head, as shown in Figure 5. This method allows multiple ports to be tested simultaneously if the probe test patterns on the board are designed to match the probe head pattern, as shown in Figure 6.

The issue of VNA calibration for testing these board test structures must be carefully considered. While it is possible—for both the coaxial launch and probing cases—to perform a calibration at the VNA test ports and 1) include the test interface launch performance as part of the device under test (DUT) or 2) perform a separate de-embedding of the launches, it has been determined in previous work [4]–[6] that performing an on-board calibration places the reference plane on-board and thus provides accurate results.

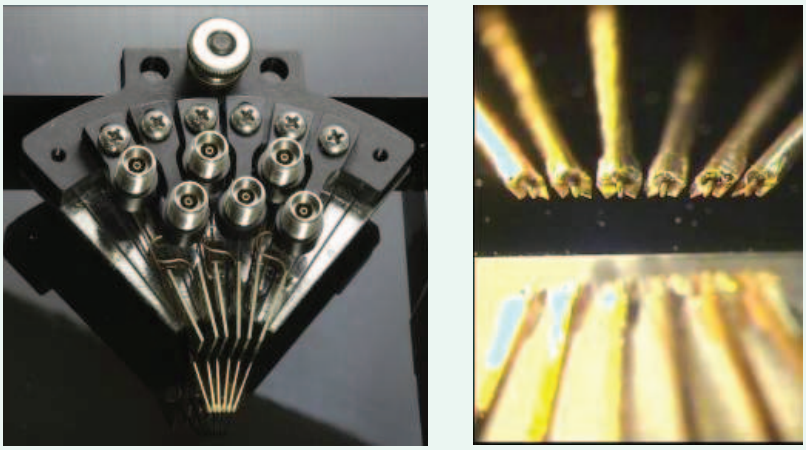


Figure 5. *Multiport ground-signal-ground (GSG) probe tips on the same probe head.*

Applying Microwave Measurement Techniques to the Problem—Multiport VNAs

VNAs having two ports are readily available in many microwave labs and, more recently, 4-, 8-, and even 12-port VNAs have become commercially available. These instruments with increased port quantities are utilized to characterize the many parallel channels of interconnect in digital systems, but why not simply utilize traditional two-port instruments?

The topic considered first is the condition of measuring n-port devices with m-port instruments when $m < n$. Frequently, in high-speed digital interconnects, this condition has presented itself when it is has been necessary to characterize coupling (crosstalk) in adjacent structures. Considering the crosstalk between two single-ended structures is an illustrative example.

In a single-ended interface, each interconnect structure is generally treated as a two-port device [Figure 7(a)]. As such, characterizing the crosstalk between one aggressor structure and one victim structure involves measurements between two two-port devices as shown in Figure 7(b).

Conceptually, it is useful to consider the structure of Figure 7(b) as a single four-port device ($n = 4$). If it were necessary to utilize a two-port VNA to characterize this device ($m = 2$), the condition of $m < n$ is realized. If two

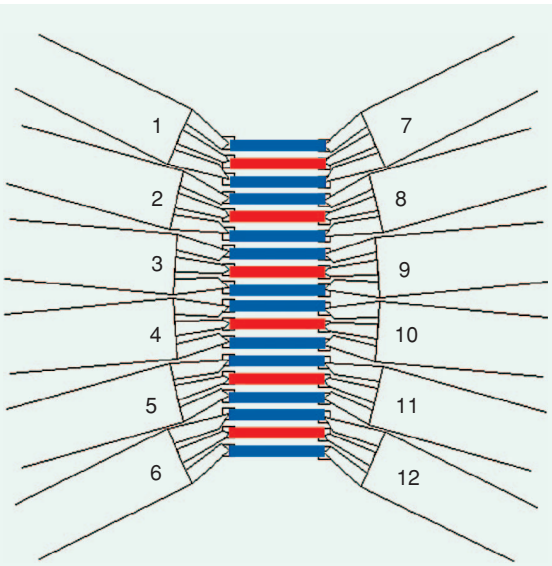


Figure 6. *Multiport probing pattern on a test board.*

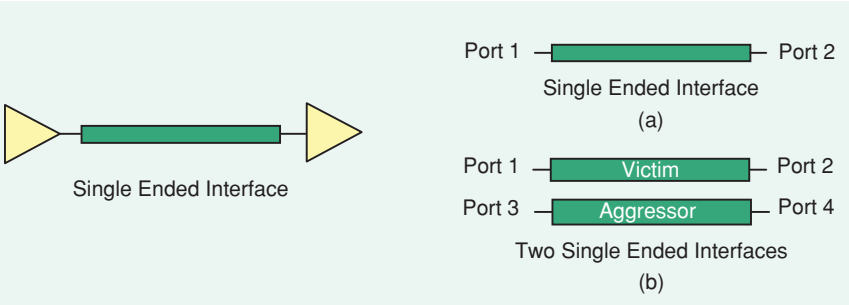


Figure 7. *Example of port numbering for (a) one single-ended interface and (b) two coupled, single-ended interfaces.*

aggressors and a single victim (i.e., three coupled structures) were of interest, it then follows that the number of device ports, $n = 6$, is still $> m = 2$, and so on.

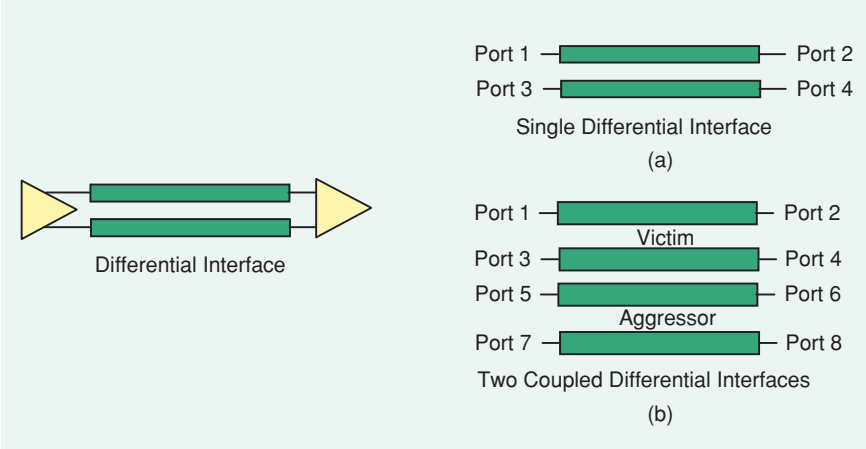


Figure 8. *Example of port numbering for (a) one differential interface and (b) two coupled differential interfaces.*

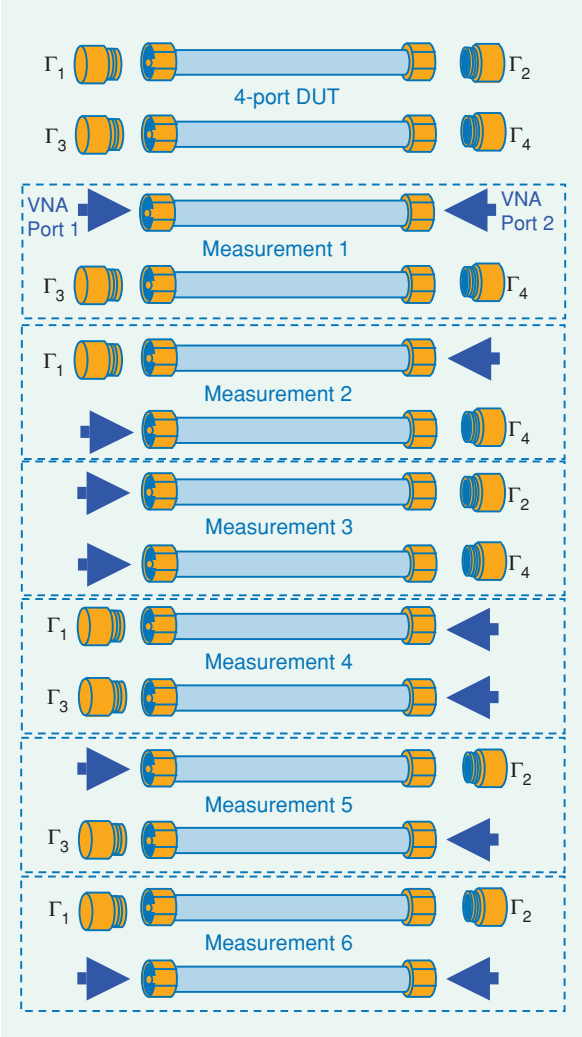


Figure 9. *Example of two-port measurements needed to characterize a four-port device. This illustrates the consistent application of terminations* (Γ_{1-4}) *to each port.*

If this discussion were expanded to include differential interfaces, then the simplest interface becomes a four-port structure [Figure 8(a)]. Similarly, measuring crosstalk between one aggressor structure and one victim structure now would be treated as an eight-port measurement as shown in Figure 8(b).

When measuring with a two-port VNA, the condition of $m < n$ exists with even the minimum differential structure ($2 < 4$). Currently, four-port VNAs ($m = 4$) to microwave frequencies are commonly available, and this provides for the condition $m = n$ ($4 = 4$) for the minimum differential structure. However, it is clear that when considering crosstalk between two or three coupled differential pairs ($n = 8$ and $n = 12$, respectively), the condition of $m < n$ exists.

In principal, this isn't a new challenge. In [7], Tippet and Speciale describe a procedure for measuring n-port devices with m-port instruments where $m < n$. Their procedure requires first having unique, known terminations ($\Gamma_1..n$) for each port. Next, multiple m-port measurements are made until all combinations of n-ports taken m at a time have been completed. An example of this procedure, where $m = 2$ and $n = 4$, is shown in Figure 9 and described in the following.

For the case where $m = 2$ and $n = 4$, $n(n-1)/2 = 6$ measurements are required to characterize the n-port device. Each of these six measurements produces a 2×2 S-parameter matrix which is a function of the terminations applied to the unmeasured ports. Once completed, all of these measurements must then be combined to produce the 4×4 S-parameter matrix of the DUT

$$\text{DUT} = \begin{pmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{pmatrix}$$

S-parameter matrix of a four-port DUT.

The submatrix collected from each measurement is illustrated in Figure 10.

From Figure 10, it is clear that the six measurements allow each of the off-diagonal S-parameters to be measured precisely one time. However, in achieving this, the on-diagonal S-parameters are each measured three times. If the terminations $\Gamma_{1..n}$ are not identical, then the repeated measurements of the on-diagonal S-parameters will not be identical.

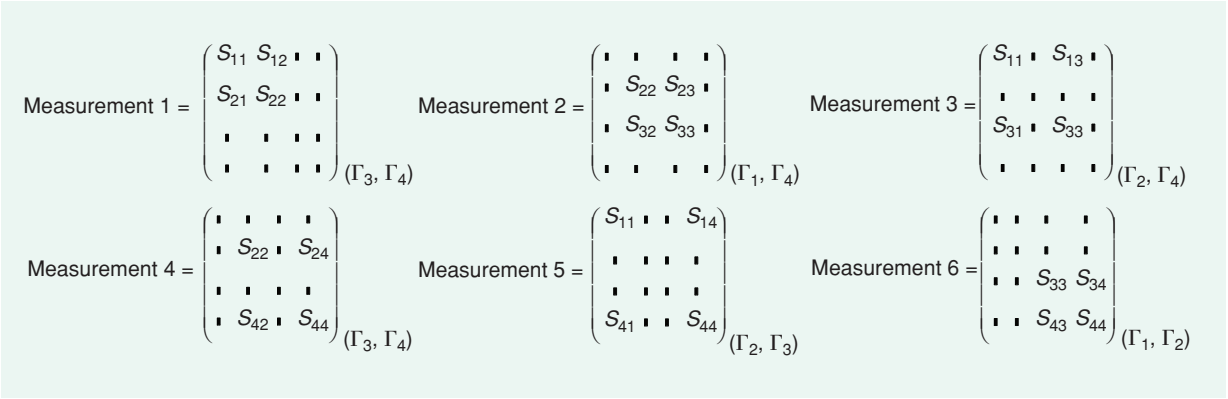


Figure 10. *Each of the six two-port measurements produces a* 2×2 *submatrix of the final* 4×4 *matrix which is a function of the terminations applied* (Γ_{1-4}).

Recall that it has been required that all of the terminations are known. Given this, it is possible to use the generalized scattering matrix renormalization to mathematically transform each *m*-port from the normalized port impedance of the measurement system to the normalized port impedance of the terminations [7].

Further study on this topic is captured in [8]–[11], and while each represents a slightly different approach to this problem, the required use of some quantity of known terminations still exists.

Practical Limitations

A practical limitation exists in many measurements when attempting to apply the techniques described above, and this occurs most notably when the interface to the DUT/fixture is made using microprobes rather than coaxial connectors.

With microprobe measurements, it is often the case that the terminations are either patterned or assembled onto the fixture. In these cases, it is then necessary to design multiple copies of the fixturing to accommodate all the various port/termination configurations that must be measured (Figure 11).

To be successful with this approach, it is first necessary to assume that the behavior of the multiple DUTs and fixturing is sufficiently repeatable. If this assumption is valid, then the resulting six measurements are shown in Figure 12.

As in the example of Figure 9, the off-diagonal elements of the 4×4 *S*-parameter matrix are each measured once, while the on-diagonal elements are measured multiple times. However, note there is not one unique termination for each port, but three different terminations on each port depending on the fixture (Figure 12). If the terminations are integrated with the DUT (i.e., as thin-film resistors), it is difficult to know their behavior independent of the DUT. If the terminations are assembled [i.e., as surface mount technology (SMT) components], the same characterization difficulty exists, as the assembly process contributes to the terminations' behavior. Therefore, for this approach to be successful, an additional assumption that the terminations are sufficiently repeatable is often necessary.

Benefits of Using n-Port Instruments for n-Port Devices

The previous section explained that while it is possible to measure *n*-port devices with $< n$-port instruments, some assumptions must be made. Regardless of the device, multiple measurements must be made, post-processed, and combined to produce the desired result. In the worst case, repeatable behavior across manufacturing and assembly variances must be assumed. For devices up to 12-ports ($n = 12$), Table 1 quantifies how these assumptions scale versus the number of available instrument ports.

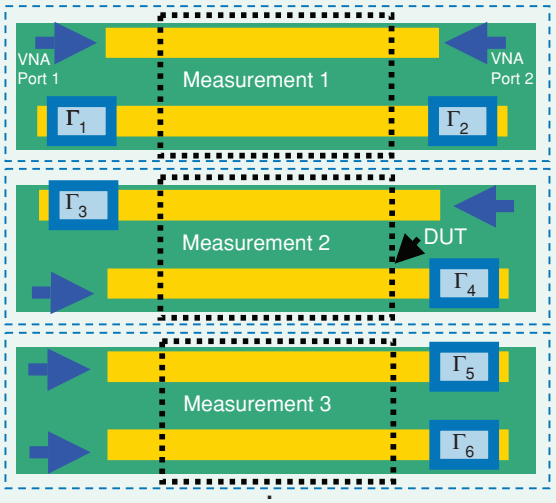


Figure 11. *Example of three of the two-port measurements necessary to fully characterize the four-port, illustrating the application of a unique termination* (Γ_{1-6}) *to each unmeasured port and the need for a unique DUT and fixturing for each measurement.*

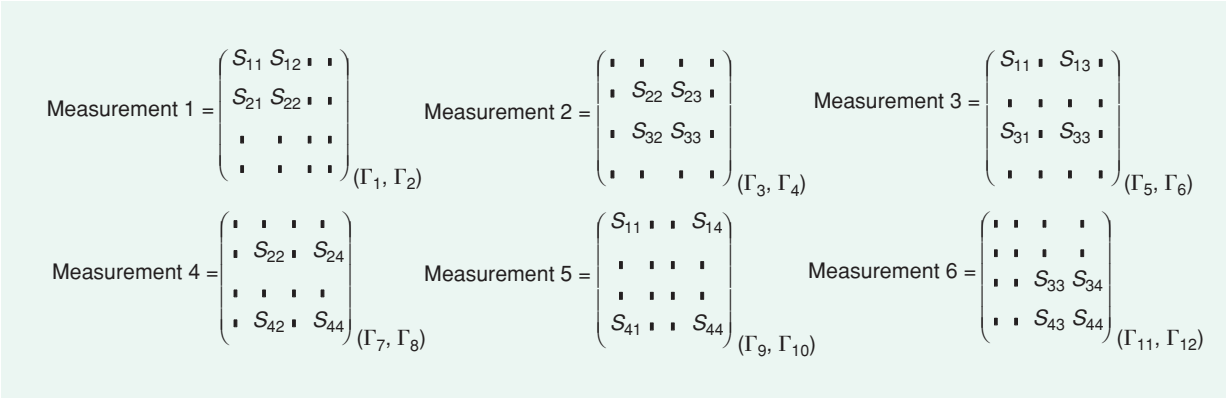


Figure 12. *Each of the six two-port measurements produces a* 2×2 *submatrix of the final* 4×4 *matrix, which is a function of the terminations applied* (Γ_{1-12}).

Table 1 is a worst-case illustration for the cases where $m < n$ and assumes no device symmetry. However, what should also be clear from Table 1 is that in the cases where $m = n$, the assumptions of symmetry and repeatability are no longer necessary. Significant benefits in terms of measurement time, postprocessing time, and fixture design complexity also result from requiring only a single measurement per DUT. Though there are multiple ways to implement these multiport VNAs, some choices create opportunities for additional efficiencies. Several of these choices will be discussed in the following sections, in the context of developing and utilizing a 12-port, 65-GHz VNA.

Multiport VNA Architectural Choices

In considering the architecture of an n-port VNA, we will focus on the macro questions of how the sources, receivers, and couplers should be configured. Somehow associated with every port must be a path to a source, to a reference and test coupler, and to a reference and test receiver. The basic questions that must be answered from this viewpoint include:

- How many sources? If less than one per port, how are they switched to the ports?
- How many couplers and where should they be?
- How many receivers? If less than two per port, how are they switched to the couplers?

Several possible configurations are shown in Figure 13. In some cases, additions are made to a two-port VNA [Figure 13(b) and (c)], while in another the construction is integral [Figure 13(a)].

To more clearly delineate why certain choices may be made, it might help to look more carefully at the constraints.

1) Because of the frequencies involved, extra sources and receivers will be very expensive. Extra couplers will be much less so.
2) Cable and connector losses are also very high due to the frequencies involved. It is particularly important to minimize losses after the test couplers as this will affect raw directivity and, hence, measurement stability. Stability is even more important as the port count increases since simplified calibrations will be desirable and tend to be more sensitive to stability.
3) Switch loss per unit isolation gets worse at higher frequencies. Thus, one should carefully consider isolation needs and minimize complexity of the switch fabric. This means that while all N^2 S-parameters must be measurable, it may not be necessary that every port be drivable by every source.
4) At higher frequencies, single-pole double-throw (SPDT) switches perform much better (in terms of loss per unit isolation) than single-pole triple-throw (SP3T) or single-pole quadruple-throw (SP4T) switches. Consider this in setting up the switch fabric.
5) Certain details of the measurement system may come into play. For example, if the measurement system is source-locking (i.e., using a coupled reference signal to lock the source), it may be desirable to keep a tighter control on how reference couplers are placed.

Table 1. DUT variations and terminations versus instrument ports.

No. of DUT Ports	No. of Instrument Ports	No. of DUT Variations	Total No. of Terminations
2	2	1	0
4	2	6	12
8	2	28	168
12	2	66	660
4	4	1	0
8	4	6	24
12	4	15	120
8	8	1	0
12	8	3	12
12	12	1	0

Shaded rows highlight cases where the number of DUT ports and instrument ports are equal (m=n).

6) For calibration simplicity, it would help if the load match presented by a port is independent of the driving port.

On the highest level, having one source and receiver per port is probably impractical at these higher frequencies per the configuration in Figure 13(a). The performance level of a switch matrix in front of a two-port (or M port, $M \ll N$) VNA will likely be unacceptable for stability reasons. This tends to argue for a coupler (or coupler set) per port, as in the configuration of Figure 13(c), as a more practical approach.

Much could be said about having a test and reference coupler per port versus having only a test coupler per port (in which case, the reference coupler back in the two-port VNA would be used). From the point of view of calibration simplicity, the former is preferable. As discussed later in this article, however, approaches have been found to allow all known calibration methods (and combinations thereof) to be used when there is limited reference coupler coverage. In this particular measurement scenario, it was desired to source lock the receiver and have a tighter control of reference signal levels. Since the calibrations would not be hampered, system sweep control would be simplified, and costs could be reduced, this led to a decision to use only one test coupler per port.

The above analysis leads to a structure like that in Figure 13(c). Due to the need to be close to the DUT (in a wafer probing environment), compartmentalizing the test couplers makes some sense so they can be positioned around the probing platform. The first layer of switches (nearest the DUT) is where the bulk of the isolation is needed, since that is where neighbor-to-neighbor potential coupling is unavoidable. From the performance advantages of SPDT switches, it then follows that the ports may want to be separated into pairs. This leads to the architecture shown in Figure 14, which also has the advantage of having the load match consistent. The load match is determined by the drive-side SPDT off-state impedance in almost all cases.

With a general architecture selected, one may then consider some of the implementation details. Many adequate couplers exist for this application, and so what about the switches? Mechanical switches were ruled out

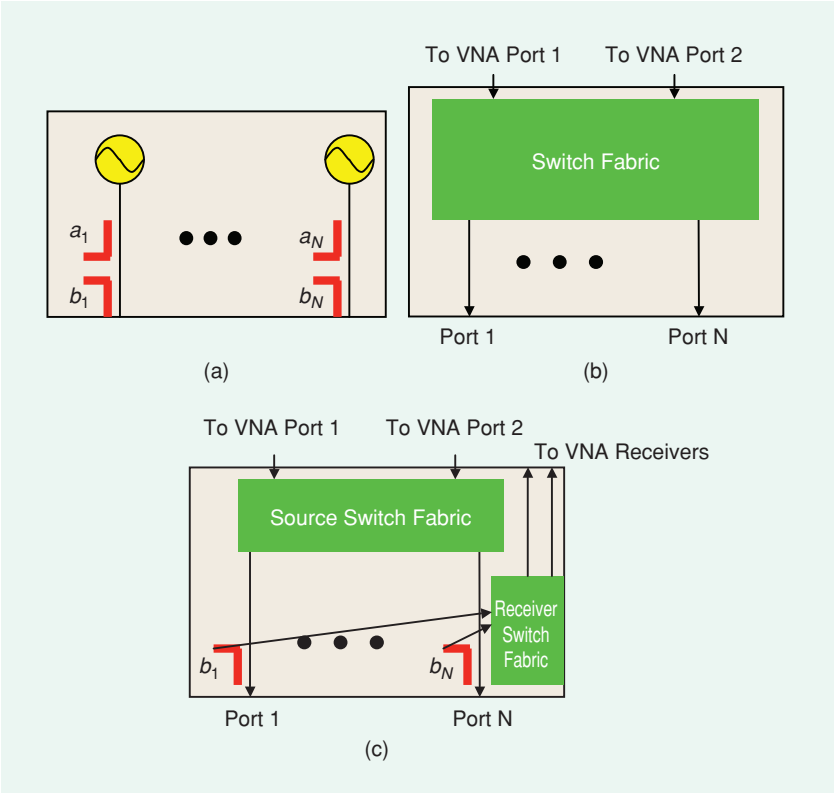


Figure 13. *Some possible extremes of architectures for a multiport VNA system using (a) a source and receiver per port, (b) only a two-port VNA as a base and relying entirely on a switch fabric to connect to N ports, or (c) a combination using independent test couplers but a base two-port VNA plus switch fabric to provide test signals.*

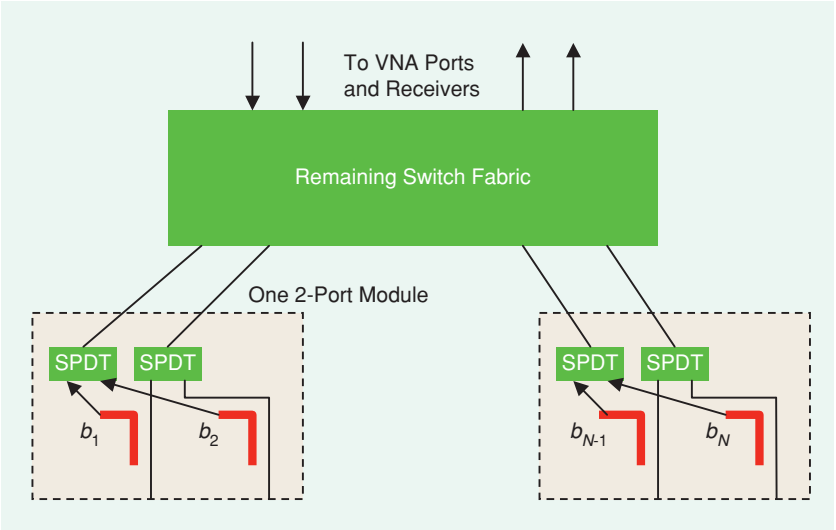


Figure 14. *A somewhat more optimal N-port architecture for wafer and board probing applications at high frequencies is shown here. Test ports are compartmentalized into pairs to improve stability and isolation.*

primarily for repeatability, match stability, and speed. While a variety of solid-state solutions are possible, some current diodes comprised of a P layer, an insulating layer, and an N layer, (PIN) offered relatively good insertion loss per unit isolation. The PIN-diode-based SPDT switches used here have a maximum insertion loss of about 7 dB to 65 GHz with an isolation of at least 110 dB to 65 GHz. This performance and the layer structure opens up the use of SP3T switches with modest insertion loss (~3 dB at 65 GHz) and > 50 dB of isolation on the upper level. A 12-port system uses a layer of four SP3T switches (two for source side and two for receive side) to form this remaining switch fabric section.

This resulting system had reasonable raw directivities (~10 dB or better to 65 GHz when configured in a wafer probing environment) and stability, as indicated by the line measurement in Figure 15 taken 42 h after calibration. The insertion loss drift observed is believed to be due to the cabling and temperature changes.

Calibration and Measurement Options for Multiport Measurements

We will now describe a general calibration approach for multiport systems, which has been applied and proved effective for the 12-port system just presented. In the following discussion, we will call the combination of the test and reference coupler a *reflectometer* or *complete reflectometer*. If the reference coupler is not present, the reflectometer will be called a *partial reflectometer*.

In the past, multiport VNA calibrations have been mainly developed for the complete reflectometer architecture; see an example for four ports in Figure 16(a) [12]–[14]. The well-established calibration techniques involve the use of either fixed standard sequences or automated electronic calibration devices. For the partial reflectometer architectures, as illustrated in the four-port example in Figure 16(b), some extensions of the ten-term error model have been proposed in the past [15].

In most cases, off-the-shelf calibration techniques for multiport systems suffer from the following drawbacks:

- The implementation is complex, and in many cases the formulation is not port-scalable.
- A rigid standard sequence must be followed.
- A significant number of standards and a very large number of connections are required.

Recently, a new calibration methodology for multiport VNAs with partial reflectometer architectures was introduced by the authors in [16]. It is based on the

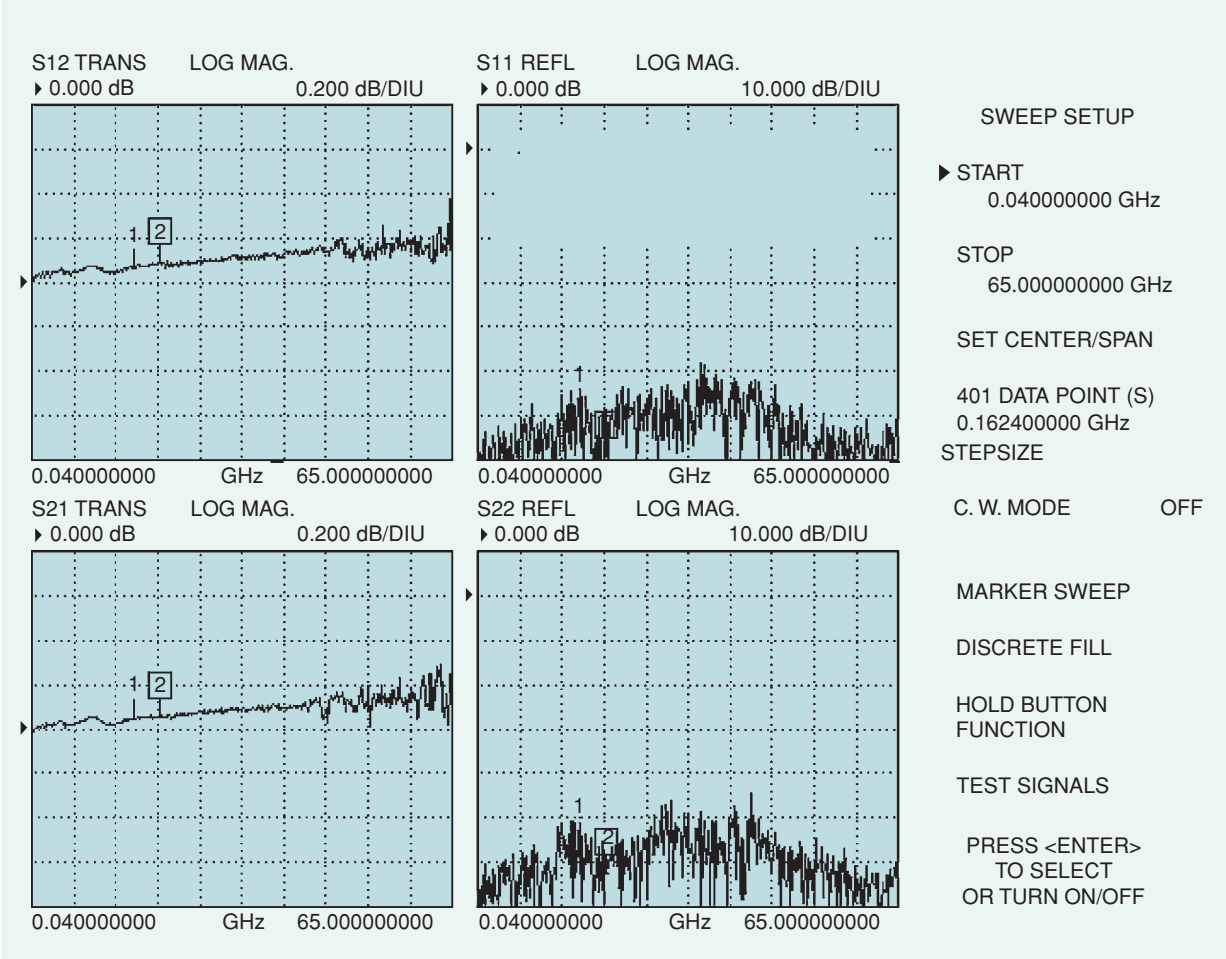


Figure 15. *The measurement of a coaxial delay line 42 h after calibration. There was some insertion loss drift due to cables and temperature changes.*

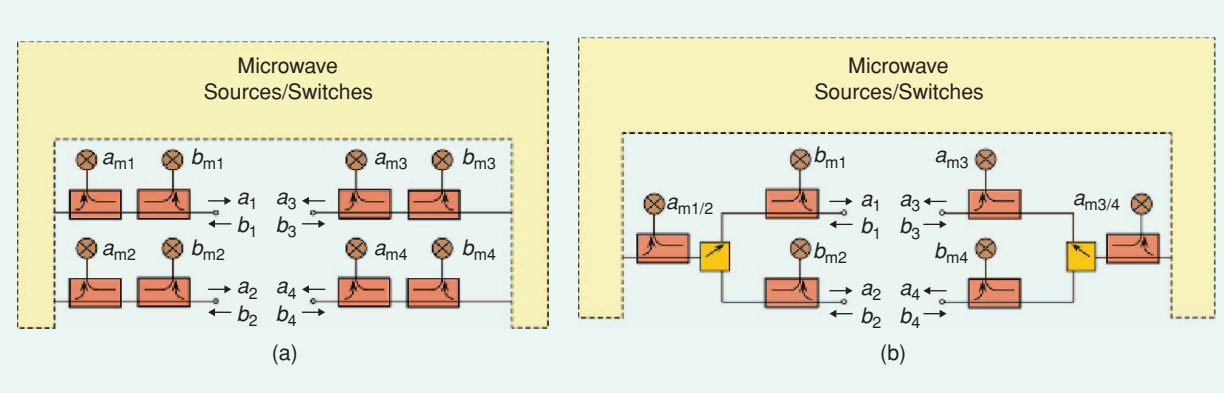


Figure 16. *(a) Complete reflectometer multiport architecture and (b) an example of a partial reflectometer architecture.*

assumption that each port has two possible states, as shown in Figure 17: state A [Figure 17(a)], where a complete reflectometer is connected, and state B [Figure 17(b)], where only the reflected wave (test) coupler is available.

The new calibration approach introduces:

- simple, compact, and easily scalable math, useful for both complete and partial reflectometer architecture
- flexible standard sequence
- reduced number of standards and connections.

The new error model generalizes the ten terms of the well-known two-port error model to a multiport error model and allows the combination of measurements at different ports of different standards in a single linear system with $6 \cdot n - 1$ error terms. The generalized equation, for error-coefficient computation or deembedding, is the following:

$$-\boldsymbol{S}\boldsymbol{G}\hat{\boldsymbol{B}}_m + \boldsymbol{F}\hat{\boldsymbol{B}}_m - \boldsymbol{S}\boldsymbol{L}\tilde{\boldsymbol{B}}_m + \boldsymbol{K}\tilde{\boldsymbol{B}}_m + \boldsymbol{S}\boldsymbol{H}\tilde{\boldsymbol{A}}_m - \boldsymbol{M}\tilde{\boldsymbol{A}}_m = \boldsymbol{0}, \quad (1)$$

where $\boldsymbol{S}$ is the DUT or standard scattering matrix; $\boldsymbol{H}, \boldsymbol{K}, \boldsymbol{L}, \boldsymbol{M}, \boldsymbol{F}, \boldsymbol{G}$ are diagonal $n \times n$ matrices containing error coefficients; and $\tilde{\boldsymbol{A}}_m, \tilde{\boldsymbol{B}}_m, \hat{\boldsymbol{B}}_m$ are matrices containing the measured incident and reflected waves (see [16] for details).

Now we will briefly revisit the dynamic calibration concept, originally introduced only for a complete reflectometer VNA and recently extended to partial reflectometer architectures. More information can be found in [13] and [17]. The dynamic calibration technique was originally developed on a graph-theory-based algorithm, which dynamically computes the standard sequence, with the following assumptions:

- Only a set of available one- and two-port standards is required, and thus no multiport standards are needed to accomplish the calibration.
- The user can define the connectivity properties among the different VNA ports; i.e., the user specifies which ports can be connected with fully defined two-port standards as thrus or partially defined standards (e.g., reciprocal devices).
- The user may also integrate one or more two-port traditional calibrations on specific port pairs to increase the accuracy.

The dynamic calibration is particularly useful for measurements in the digital world. In this scope, it is common to have mixed environments, such as on-wafer and coaxial ports, gender connectivity problems, or mechanical dimension problems where ports are separated too far to be easily connected. Dynamic calibration, allowing the user to decide where to connect thrus or unknown thrus, is crucial in these cases. Moreover, as the number of ports increases, a reduced standard sequence means there is less probability for mistakes due to loose connectors or bad probe contacts. Reduced calibration time is another important benefit both in R&D and production test applications.

A software program [17] has been developed that incorporates these measurement and calibration methodologies, providing the capability to compute an optimized standard sequence which reduces the number of connections and the corresponding measurement complexity.

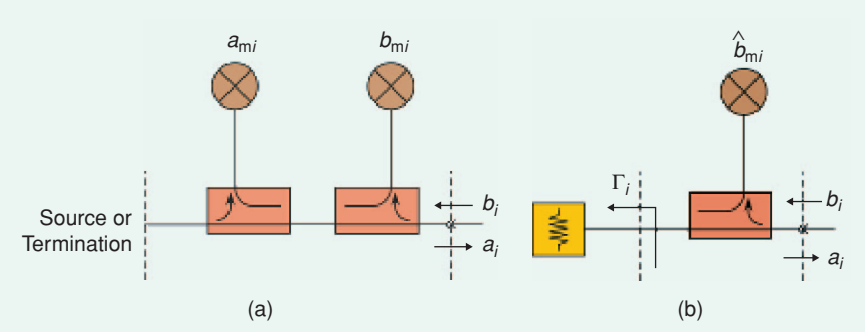


Figure 17. *(a) State A and (b) state B configurations.*

For example, let us consider a directional coupler with two APC7 and two female SMA ports (see Figure 18). This is a typical case where the connector gender and types cause some problems. Indeed, a thru connection is possible only between Ports 1 and 2. All other ports can be connected only through the use of adapters. These issues typically require time-consuming adapter removal techniques, losing measurement accuracy and introducing more standards connections. The new software instead allows for building a calibration (Figures 19 and 20), which fits the types of connectors and restrictions imposed by the DUT. To determine the standard sequence, the software splits the ports into different groups according to the user specification (see Figure 19). Then, it merges the groups as much as possible into fully known two-port devices or unknown two-port devices—in this case one unknown thru—and computes the final sequence, as shown in Figure 20. In this way, no adapter removals are needed and a high level of accuracy is achieved.

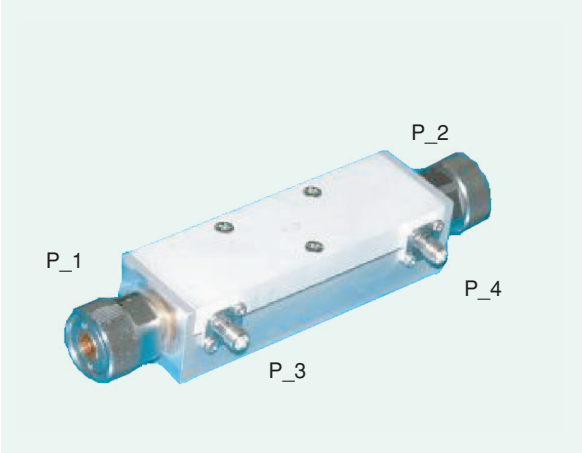


Figure 18. *An example of a DUT: a directional coupler with two SMA and two APC7 ports.*

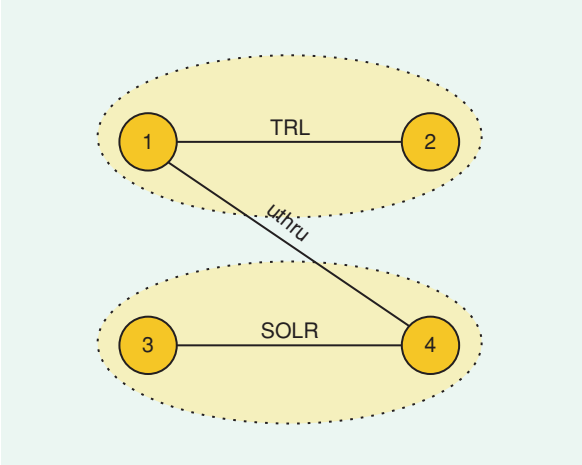


Figure 19. *An example of dynamic calibration for a four-port system.*

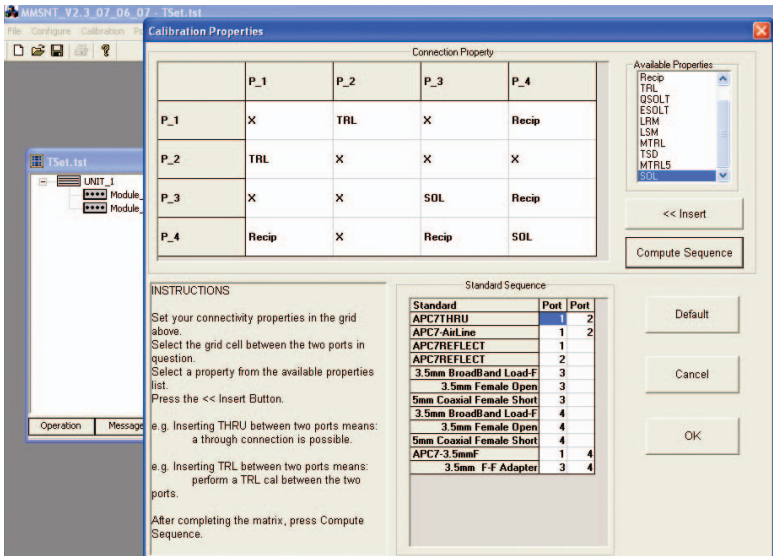


Figure 20. *Dynamic calibration: connection matrix and standard sequence.*

Examples of Interconnect Device Measurements

The previous sections described the VNA hardware and calibrations required to support multiport measurements. But there are additional capabilities that a multiport VNA must support in order to make these types of multiport measurements feasible on a regular basis.

During the VNA calibration process, it is possible for several deterministic variances to occur which can affect the quality of the calibration. Several well-known examples of these are cable movement, temperature drift, and probe or connector repeatability. Typically, if something does occur that causes a calibration to be unacceptable, an attempt is made to identify and address the problem and then the entire calibration is repeated. In a one- or two-port calibration, the penalty—in terms of time—for repeating the entire calibration may be acceptable. However, as was illustrated in [6], the penalty with increasing port counts can grow dramatically (up to ~2.5 h for a 12-port calibration) depending on the calibration approach chosen.

Furthermore, simply repeating the calibration doesn't ensure that new errors are not introduced. Again, in a one- or two-port calibration, it can be a challenge to ensure repeatable conditions for the standard measurements on each port (whether probed or coaxial standards). As the number of ports increases, so too does the number of standard connections. Consider that for a typical two-port short, open, load, thru (SOLT) calibration, the number of repeatable port connections required is eight, whereas for a reasonably equivalent 12-port SOLT calibration this number of connections jumps to 58 (Figure 21).

Taking maximum advantage of the calibration methods described previously would reduce this 12-port SOLT calibration to 25 port connections [6]. However, even making 25 port connections repeatable presents challenges.

Figure 22 illustrates a 12-port microstrip PCB structure where contact is made through replaceable 2.4-mm coaxial connectors. This structure was measured after the completion of a reduced 12-port thru, reflect, line (TRL) calibration which had required 28 port connections, with the results shown in Figure 23.

As seen from the measurements in Figure 23, five of the six microstrip structures demonstrated the expected behavior. However, the microstrip structure placed between Ports 2 and 8 was clearly different. Upon further investigation, it was determined that the connector on Port 2 did not have the proper torque applied during the calibration. Correcting the connector torque during a complete recalibration would again require 28 connections to be made. However, if the only standards that contacted Port 2 could be remeasured, and the error coefficients recalculated, this would reduce the number of connections that need to be made to four (in this example). Figure 24 illustrates the result of performing only these four measurements and updating the existing calibration.

This type of capability may be a convenience with one- or two-port measurements. But it is essential for measurements with increasing port quantities, and it is just one example of a needed capability beyond the fundamental VNA hardware and calibration algorithms.

Now that we have seen an example of a calibration process and its data, we will discuss an example of the multiport characterization of a digital interconnect device placed on a test structure, shown in Figure 25. This is a characterization test board for a CPU socket, using on-board calibration elements and de-embedding structures with 12-port microwave probes for the test interface with the 12-port VNA. CPU sockets are used in many computers to provide a removable connection between the CPU package and the system motherboard, so this is a good example of a digital

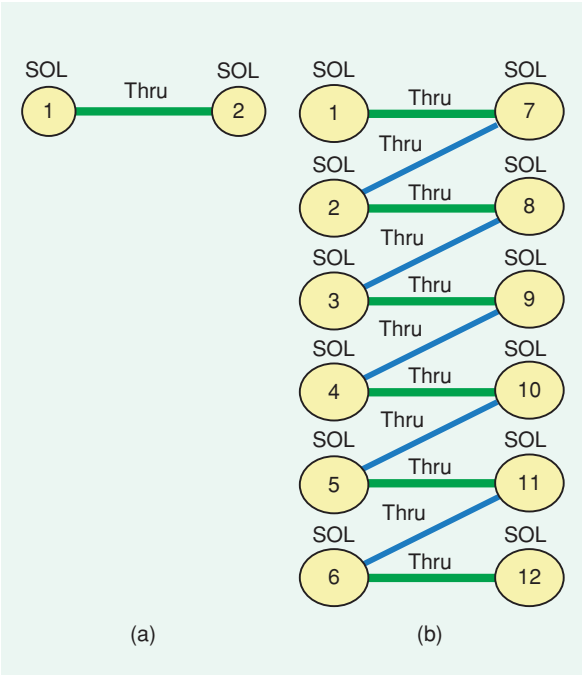


Figure 21. *Ball diagrams for SOLT calibrations: (a) Two-port requiring eight-port connections and (b) 12-port requiring 58 connections.*

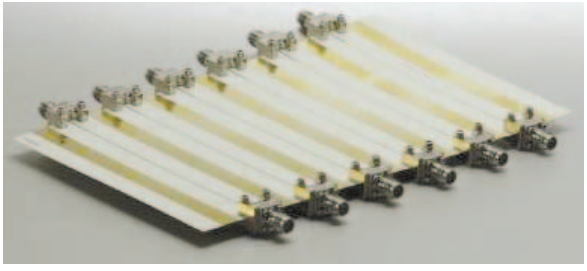


Figure 22. *12-port, coax, microstrip structure.*

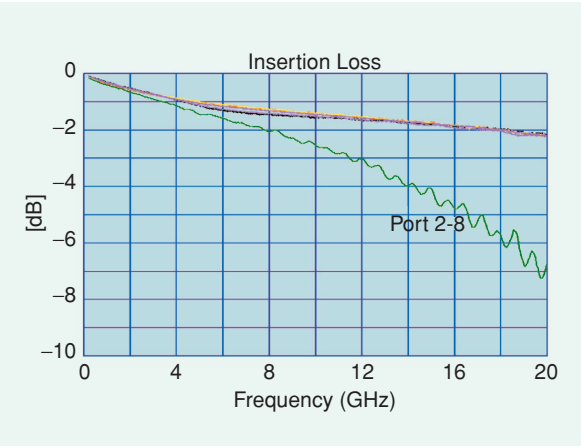


Figure 23. *Microstrip measurement after initial TRL calibration.*

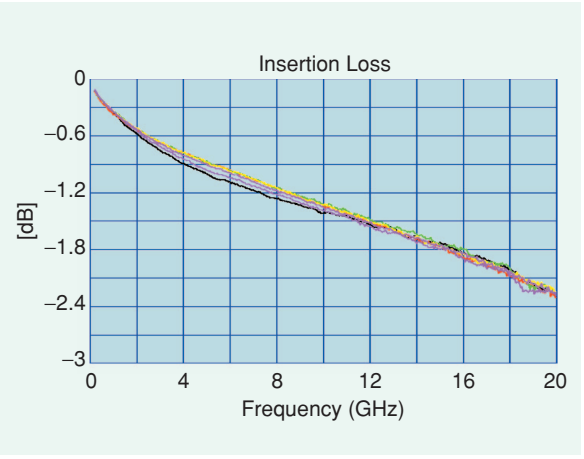


Figure 24. *Microstrip measurement after updated TRL calibration.*

interconnect device that requires multiport high-frequency characterization. The test board contains on-board 12-port multiline TRL calibration elements, test line de-embedding structures, and an SMT-mounted socket to be characterized. Using the 12-port VNA, the differential response of the socket can be obtained through the single-ended measurements and postprocessing of the data using the integrated capabilities in the test software. This will give the differential response of one victim line and the crosstalk from two adjacent aggressor lines from this 12-port measurement.

The layout of the test board in Figure 25 shows the land grid array (LGA) socket soldered to the board in the lower-left side with a test package and retention (clamping)

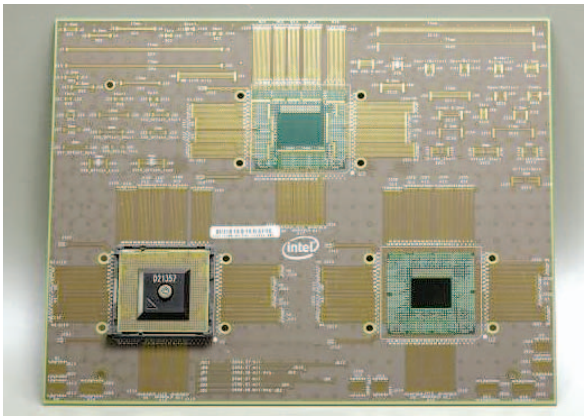


Figure 25. *CPU socket multiport test board with socket and test package.*

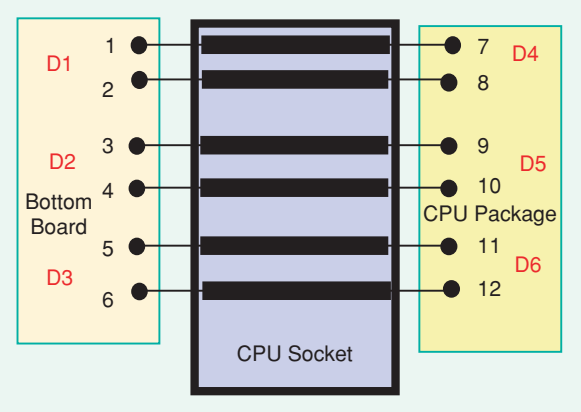


Figure 26. *Port assignment for 12-port measurements of the CPU socket.*

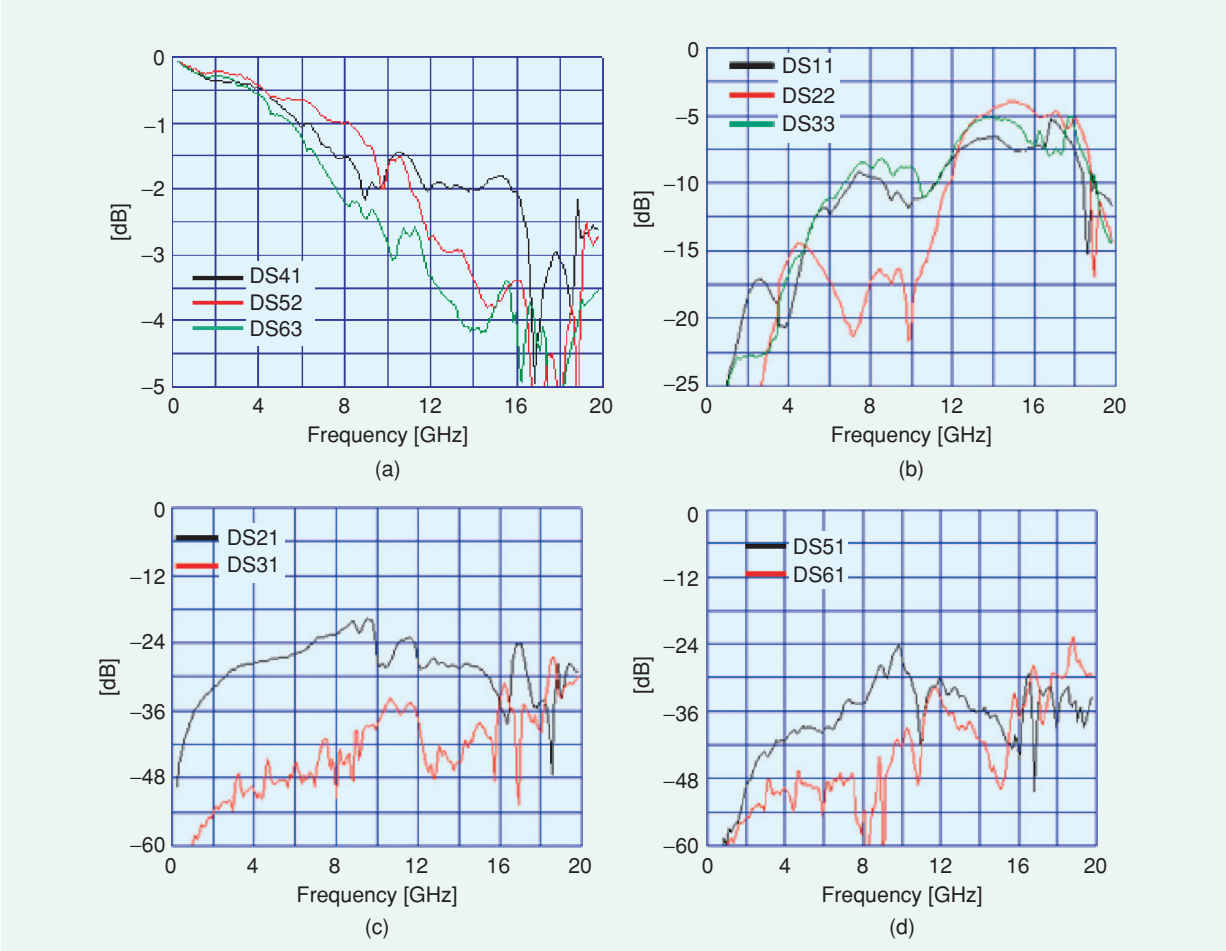


Figure 27. *Typical socket differential, de-embedded multiport data: (a) Differential insertion loss, (b) differential return loss, (c) differential NEXT, and (d) differential FEXT.*

structure to compress the package into the socket to provide the LGA socket contacts and the test package pads. An additional socket mounting site is shown at the lower-right section of the board with the test line deembedding structures placed in the upper-center region. All of the various calibration and verification structures are placed in the upper-left and upper-right regions. The measurement port assignment and configuration is shown in Figure 26.

Figure 27 displays the postprocessed, differential *S*-parameter data of the socket. It should be noted that this data has all the board and package test lines deembedded so that this is only the response of the socket, plus the solder balls, pads, and 1-mm microstrip line length on the bottom of the socket as well as the package LGA pad, a short (0.79mm) package via, and 1-mm microstrip line length at the top of the socket. This illustrates the differential response for this socket, including differential insertion and return loss, near-end crosstalk (NEXT), and far-end crosstalk (FEXT) for three contact pairs in the grid array. Within this three-pair configuration, one of the pairs is the victim (quiet signal channel where the unwanted noise is imposed by neighboring signal channels), and the two remaining contact pairs (aggressor channels) placed adjacent to the victim channel impart the unwanted, or crosstalk, noise.

If we look at this data from the perspective of a microwave designer, it might be surprising that this response looks relatively clean (that is, free from many resonances and discontinuities) through 8–10 GHz. Given the physical structure of these sockets, with many densely packed contacts in a grid array and the contact design driven more by the mechanical requirements rather than an optimized electrical impedance transition, the expectation might be that we would not see useable performance anywhere in the microwave frequency range. Additionally, this data points out that, due to these measurement capabilities, it is possible to design and model digital interface connections for optimized high-frequency performance and validate these designs and models with accurate real-world measurements.

Conclusions

We have seen that characterizing digital interconnect devices and structures in the high-speed microwave arena presents a variety of difficult challenges. The large number of signal lines with high density placed on a less than ideal circuit board media requires careful thought and design of the test structures, measurement and calibration methodology, and test equipment in order to accurately measure these interconnect devices and systems. The physical configuration of these board-level structures, running the range from planar to 3-D, drives the test interface to more complex forms to insure proper testability. Application of a well-known microwave tool—the VNA—to these testing challenges leads us to expanding the VNA to multiple ports and rethinking the approach to calibration and testing so that it becomes practical to extract the single-ended and differential *S*-parameter performance data from these structures. This article has shown that a 12-port VNA designed with these measurement challenges in mind, coupled with test software that incorporates new methodologies to enable multiple signal line devices to be tested accurately and efficiently and a test interface that is tailored to the specific configuration of the digital interconnect device, will result in useful, accurate measurement data to validate designs and models of digital interconnects.

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